Abstract
In recent years, the demand for system topologies incorporating high power IGBT modules in parallel has outstripped the innovation in the techniques for driving these modules. Current systems are therefore sub-optimal, compromise on efficiency, and reliability, and over-specified the modules in use increasing system costs. They also need matched IGBT Modules from suppliers, thus reducing supply chain and maintenance flexibility, and increase inventory.

1 Introduction
Amantys are introducing a new gate drive technology for applications employing direct parallel connection of the power IGBT modules. Paralleled applications are increasingly popular and are driven by a number of factors:

- Desire to have a modular solution where power output can be scaled around a common platform.
- New packages that both enhance performance through lowered parasitics in a given topology and are lower in cost. Primepack and Econopack are two specific examples here. The required output power is then achieved through multiple parallel modules.
- Very high power output systems (particularly at 4500V and above) that can only achieve the required power through multiple modules.

1.1 Why is paralleling a problem?
In theory, if all the IGBTs had the same characteristics and the gate drivers had identical time delays then parallel operation would not be an issue. In practice, however, there are a number of variables that result in a big shift from this ideal scenario. The imbalance in sharing can be split into 2 categories; the static (during the on period) and dynamic (during the switching transitions) current sharing. Static sharing will self-balance to a large extent during the on-period with modern IGBTs because of their inherent characteristics that forces them to share but large imbalances can still occur during the switching transitions.
Figure 1 shows a complete switching waveform of 3 parallel devices with zoomed in detail of the turn-on and turn-off transitions. The convergence of the current during the on-period can be observed as can the effects of one device turning on only very slightly later in time. In this case the blue trace shows the effect of just 100ns of misalignment. This misalignment is caused by parameter variation in the IGBT module, not timing variation in the gate drive or transmission system, which is assumed to be well matched.

Fundamentally the two key factors that will affect the dynamic performance of the current sharing are the turn-on synchronisation due to differences in drive timing and IGBT threshold voltage and the collector current slope ($\frac{dI_C}{dt}$). The factors that affect the current slope for a resistor based drive are highlighted in the following IGBT equations:

**Turn On:**
$$\frac{dI_C}{dt} = \frac{V_G - \left( V_{th} - \frac{I_P}{2g_m} \right)}{\frac{R_GC_{GS}}{g_m} + L_p}$$  (1)

**Turn Off:**
$$\frac{dI_C}{dt} = \frac{V_{th} + \frac{I_L}{2g_m} - V_G}{\frac{R_GC_{GS}}{g_m} + L_p}$$  (2)

Where: $V_G$ is the gate drive voltage (gate supply voltage), $V_{th}$ is the IGBT threshold voltage which also has temperature dependence, $R_G$ is the gate driver resistance, $C_{GS}$ is the IGBT gate-source capacitance, $I_L$ is the load current at turn-off, $I_P$ is the peak current at turn-on, $g_m$ is the IGBT transconductance and $L_p$ is the parasitic inductance of the particular branch of the power circuit.

It is important to understand these variable parameters in more detail and the following table highlights some of the variables and their impact on both static and dynamic current sharing:
### 1.1.1 IGBT tolerances

IGBT threshold voltage may typically have a tolerance of 1V and parallel modules will turn on at different times as this $V_{th}$ is reached. Turning on is defined as the point where this voltage is reached and the IGBT conducts current. Turning off is defined as the opposite when this threshold is passed through in a negative going direction and the IGBT is considered to be off. The IGBT input capacitance will vary from module to module resulting in additional varying time when this threshold is reached.

Both these characteristics as well as transconductance will impact the rate of change of current at turn on and off ($\frac{dI}{dt}$). The $\frac{dI}{dt}$ directly impacts the balancing of current sharing even with perfectly synchronised switching timing.

To alleviate these problems, power stack manufacturers often try and use modules from the same production batch of silicon which are more likely to have closer characteristics. In addition, selection and matching is also adopted. Both approaches cost time and money and result in decreased flexibility and potential future problems if IGBTs need to be replaced. In addition this is not a cure-all solution as other system variations still impact the current sharing.

If switching timings are not aligned then IGBTs will have to momentarily support large currents under normal switching and short circuit conditions.

### 1.1.2 Gate driver characteristics

There are a number of parameters on the gate driver that will affect the switching characteristics and therefore the parallel sharing. Even when a single gate driver is used with multiple gate connections to paralleled modules, variations in the internal gate resistance will cause differing currents and timing in the switching characteristics. For situations involving multiple gate drivers the variations in their resistors will further impact the switching timing between IGBTS and in addition other parameter differences between drivers will also cause imbalance:

- Differing power supply voltages effect gate charge/discharge timing and are also directly linked to $\frac{dI}{dt}$ (equation 1).
- Variations in each drivers propagation delay (latency). This is the time between receiving a command pulse and the gate drive circuitry changing state.

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### Table 1 - Static and dynamic dependencies of current mismatching in parallel connection

<table>
<thead>
<tr>
<th>Static current symmetry</th>
<th>Dynamic current symmetry</th>
</tr>
</thead>
<tbody>
<tr>
<td>DC-bus stray inductance</td>
<td>0</td>
</tr>
<tr>
<td>AC output inductance</td>
<td>+</td>
</tr>
<tr>
<td>Temperature difference between IGBT modules</td>
<td>++</td>
</tr>
<tr>
<td>IGBT Saturation voltage $V_{CEsat}$</td>
<td>++</td>
</tr>
<tr>
<td>Diode Forward voltage $VF$</td>
<td>++</td>
</tr>
<tr>
<td>Gate-emitter threshold voltage (VGE)</td>
<td>0</td>
</tr>
<tr>
<td>AC output resistance</td>
<td>++</td>
</tr>
<tr>
<td>DC-link resistance</td>
<td>++</td>
</tr>
<tr>
<td>Gate drive voltage</td>
<td>+</td>
</tr>
<tr>
<td>Gate turn-on and turn-off delay time</td>
<td>0</td>
</tr>
<tr>
<td>Gate loop resistance</td>
<td>0</td>
</tr>
<tr>
<td>Gate loop induction</td>
<td>0</td>
</tr>
<tr>
<td>Magnetic field influence</td>
<td>0</td>
</tr>
</tbody>
</table>

Key: 0: no impact; +: some impact; ++: significant impact on sharing
• Any jitter on these propagation delays. Where systems have glitch filters with sampled PWM this can become more of an issue when master clocks between modules are unsynchronised.

1.1.3 Power circuit parasitic inductances
It is very difficult to achieve identical inductance in all parallel power paths and this directly affects the \( \frac{dI}{dt} \) and therefore the current balancing. Therefore, the system designer will always strive to make these power connections as symmetrical as is possible.

2 Existing Approaches to Parallel Solutions
There are a number of techniques currently used to provide acceptable performance in systems with paralleled modules. A short summary of the 2 main approaches is useful in considering areas where the performance can be enhanced:

2.1 Multiple IGBT modules driven by a single gate driver
In this solution there is no special provision for parallel operation beyond each power module being fitted with its own gate drive resistors and active clamp. Although this approach eliminates the variables of multiple gate drives, there are still a number of problems:

• The IGBT modules still require selection for threshold voltage and the outlined problems.
• The length of gate drive wires needs to be balanced, and the wires themselves add inductance which makes control of the IGBT under fault conditions problematic.
• Gate driver resistors and active clamp TVS devices still need to be fitted locally on each individual module.
• The more large modules that are added in parallel, the lower the potential switching frequency supported results. This is because the gate drive PSU will only be capable of driving a given capacitance at a given frequency. As IGBTs are added in parallel the capacitances add together. If the driver is scaled to have lots of excess power capability to do this then it will be a long way from optimal cost when driving a single module.
• There is no opportunity in a fault reporting system to know which IGBT has an issue. The unit behaves as if it were driving one large IGBT.

The main advantage of this approach is that it requires no cost in the gate drive module design. Because there is only a single driver when controlling multiple modules it will appear cheap on first sight but as a result of previously outlined shortcomings this saving can easily be lost through using more modules than required. Bearing in mind that a single extra 190x140mm module is equivalent to at least 4 gate drivers, this can easily be false economy!

2.2 Traditional Master/slave gate driver architecture
Another paralleling approach is that of master/slave configured gate driver cards. In this system the master receives the incoming PWM and passes it on to slaves through a consistent latency data link. On first sight, this has the advantage that slaves will be significantly lower cost but when you take into account the actual implementation and some of the resulting problems, this system still has compromises:

• All the IGBT variables still manifest themselves in the current balancing performance.
• Gate resistor and power supply tolerances will be exhibited.
• The data link between the master and the slave requires isolation of at least 100V. Although the IGBTs are directly connected in parallel, there are still significant voltage shifts between them as large currents move around with high speed transitions. In fact the worse the balancing, the more pronounced this problem becomes.
Fault and acknowledge signals are fed back to the master so faults can be determined but there is no possibility of indicating which IGBT is at fault.

2.3 Directly paralleled gate driver architecture
The final examined approach is that of directly paralleled gate driver cards. In this system each power module has its own gate driver and the incoming PWM signal is fed directly to all the inputs. The approach relies upon low and consistent propagation delays between the drivers with low jitter. An examination of performance can be summarised as follows:

- All the IGBT variables still manifest themselves in the current balancing performance.
- Gate resistor and power supply tolerances will be exhibited.
- The data link and PSU on each driver already has the full IGBT isolation voltage so there are no issues with isolation.
- Because of the tight tolerance required in timing only an electrical interface can be employed as fibre is both variable in timing and presents issues in coupling the send and return signals together. Therefore, a fibre input system would need an adaptor board to convert the fibre interface to multiple electrical ones.
- Each gate driver has its own PSU so the system scales well although does incur additional cost as multiple PSUs will cost more than a single higher power one to achieve a given power rating.
- Fault and acknowledge signals are fed back to the master as a combined signal, so although faults can be determined, there is no possibility of indicating which IGBT is at fault. Again the parallel combination behaves as a single large IGBT.

3 Amantys Proposed Solution
After examining a number of potential approaches to paralleling that could both improve upon the limitations of existing solutions as well as be integral in the on-going standard product range, Amantys have developed a technology based around true alignment of the IGBT switching transitions that is being called Amantys Adaptive Parallel. By synchronising the current edges at turn-on and turn-off, and assuming a consistent dI/dt, the IGBTs will share the load current much more effectively in a parallel application. This approach will overcome many of the previously outlined shortcomings. In addition to tight control of the timing of switching transitions the system incorporates a mechanism to allow Power Insight data and configuration to be accessible at an individual IGBT level.

The resulting solution incorporates circuitry on the gate drive that controls the IGBT turn-on and off transitions so that they occur at a defined point in time. Each gate driver monitors the point where it is switching and adapts the timing to force switching events to occur at a defined time and thereby result in tight alignment. Because the actual time of these events is aligned in a way that is independent of the IGBT or gate drive parameters, the following variables in the system are addressed:

- IGBT parameters. Variations in threshold voltage and/or gate charge are compensated for in the alignment making IGBT matching unnecessary. As parameters change with temperature, the system adapts and also compensates for any differences as well as any aging effects.
- Gate driver variables including gate resistor tolerance and PSU accuracy are compensated for.
- Gate driver propagation delays are inherently synchronised and therefore tightly matched in the system.
It should be noted that the first generation of the Amantys parallel control is targeted at optimizing the dynamic switching imbalance that exists today and there is not a specific mechanism employed to balance the conduction currents. However, because of the self-balancing effect of the conduction current characteristics, and the fact that the turn-on events are aligned, very good current balancing is observed. In addition, although the Amantys system does not specifically adjust the \( \frac{dI}{dt} \) actively, system variables that also have an effect on the slope of the current outlined previously result in minimum impact on the imbalance because of the way that current slopes are synchronised.

In order for the gate drives to provide the tight alignment of the switching transitions it is important that the PWM drive signal reaches them at the same time and that drivers are synchronised together. As a result of this, and the requirement of maintaining Power Insight operation on each IGBT module, a separate parallel control bus is implemented between the paralleled gate drivers.

The advantages of using this system architecture as follows:

1. In a system with fibre inputs on the master it ensures that the PWM is transferred to the slaves with the minimum of latency. In addition the gate drivers are synchronized together.
2. Power Insight operation is provided at an individual IGBT level. Each IGBT can be addressed and configured in isolation and any data and fault codes will come from an individual IGBT/driver combination.
3. The interface between the master and slaves is differential and therefore provides flexibility in the locations of the system components in a noisy environment.
4. A single fibre optic or electrical interface will control all the parallel IGBTs. For fibre systems the master handles the system I/O and passes it across on the parallel bus to the slaves. For electrical isolation systems master and slave drives are the same physical hardware that intercommunicate through the bus where the driver with the system PWM input assumes the role of a master in controlling operation on this bus.

Figure 2 shows the same setup as the 3 parallel devices from figure 1 with the Amantys parallel control system enabled. It can clearly be observed that the dynamic current balancing has significantly improved and as a result of this the initial imbalance during the turn-on period is also significantly reduced.

The system will continuously adapt to changes in temperature and any aging of IGBT and system characteristics, ensuring that the same level of synchronous balance is maintained.
Table 2 compares the effectiveness of the different parallel approaches examined with the Amantys system. It can be seen that the Amantys adaptive parallel system addresses both the variations in driver parameters and, more importantly, the variations in the IGBT module characteristics.
<table>
<thead>
<tr>
<th>Parameter</th>
<th>One gate drive to multiple IGBTs</th>
<th>Multiple gate drives – Master/Slave</th>
<th>Multiple gate drives – Direct Parallel</th>
<th>Amantys Adaptive Parallel</th>
</tr>
</thead>
<tbody>
<tr>
<td>Temperature difference between IGBT modules</td>
<td>✗</td>
<td>✗</td>
<td>✗</td>
<td>✓ ✓</td>
</tr>
<tr>
<td>IGBT Gate-emitter threshold voltage ($V_{GE}$)</td>
<td>✗</td>
<td>✗</td>
<td>✗</td>
<td>✓ ✓</td>
</tr>
<tr>
<td>IGBT Gate Charge ($Q_G$)</td>
<td>✗</td>
<td>✗</td>
<td>✗</td>
<td>✓ ✓</td>
</tr>
<tr>
<td>Gate drive resistor variations</td>
<td>✗</td>
<td>✗</td>
<td>✗</td>
<td>✓ ✓</td>
</tr>
<tr>
<td>Gate driver supply voltages</td>
<td>N/A</td>
<td>✗</td>
<td>✗</td>
<td>✓ ✓</td>
</tr>
<tr>
<td>Gate driver propagation delays</td>
<td>N/A</td>
<td>✓</td>
<td>✓</td>
<td>✓ ✓</td>
</tr>
<tr>
<td>IGBT Saturation voltage $V_{CEsat}$ – static sharing.</td>
<td>✗ - Self-balancing as in Fig.1</td>
<td>✗ - Self-balancing as in Fig.1</td>
<td>✗ - Self-balancing as in Fig.1</td>
<td>✓ - Improved self-balancing as in Fig. 3</td>
</tr>
</tbody>
</table>

- ✓ - Some improvement, ✓ ✓ - Significant improvement
- ✗ - Does not address, N/A – Not applicable

Table 2 – Comparison of parallel imbalance mechanisms with system architecture.