
CHT-CG50LP DATASHEET

Version: 1.6

**High-Temperature , Low-Power, Versatile
Clock Generator**

General Description

The CHT-CG50LP is a versatile, low-power high-temperature crystal clock generator with low pin count. Compared to CISSOID' industry standard CHT-CG50, the CHT-CG50LP has been optimized for lower power consumption, smaller die size while offering extra features such as built-in frequency division.

The chip features a programmable crystal oscillator driver with an enable/disable control signal, an external clock input and a frequency divider selectable from 1 to 512. Using an external crystal, it is intended to provide reliable precision performance throughout the -55 to +225°C temperature range for supply voltages between 3.3V and 5V.

The CHT-CG50LP can operate with crystals from 1MHz to 50MHz. It can also be used with 32.758kHz crystal for real time clock needs.

The output frequency can be selected by means of a programmable divider, providing division factors of 1, 2, 4, 8, 16, 32, 256 and 512. The programmability of the crystal driver allows working with a wide range of crystals. An output enable pin (OEB) is also included to put the output in high impedance mode. In applications requiring only a precision divider chain - where an external clock source is already present - the crystal driver may be bypassed via the input EXTCLK_IN.

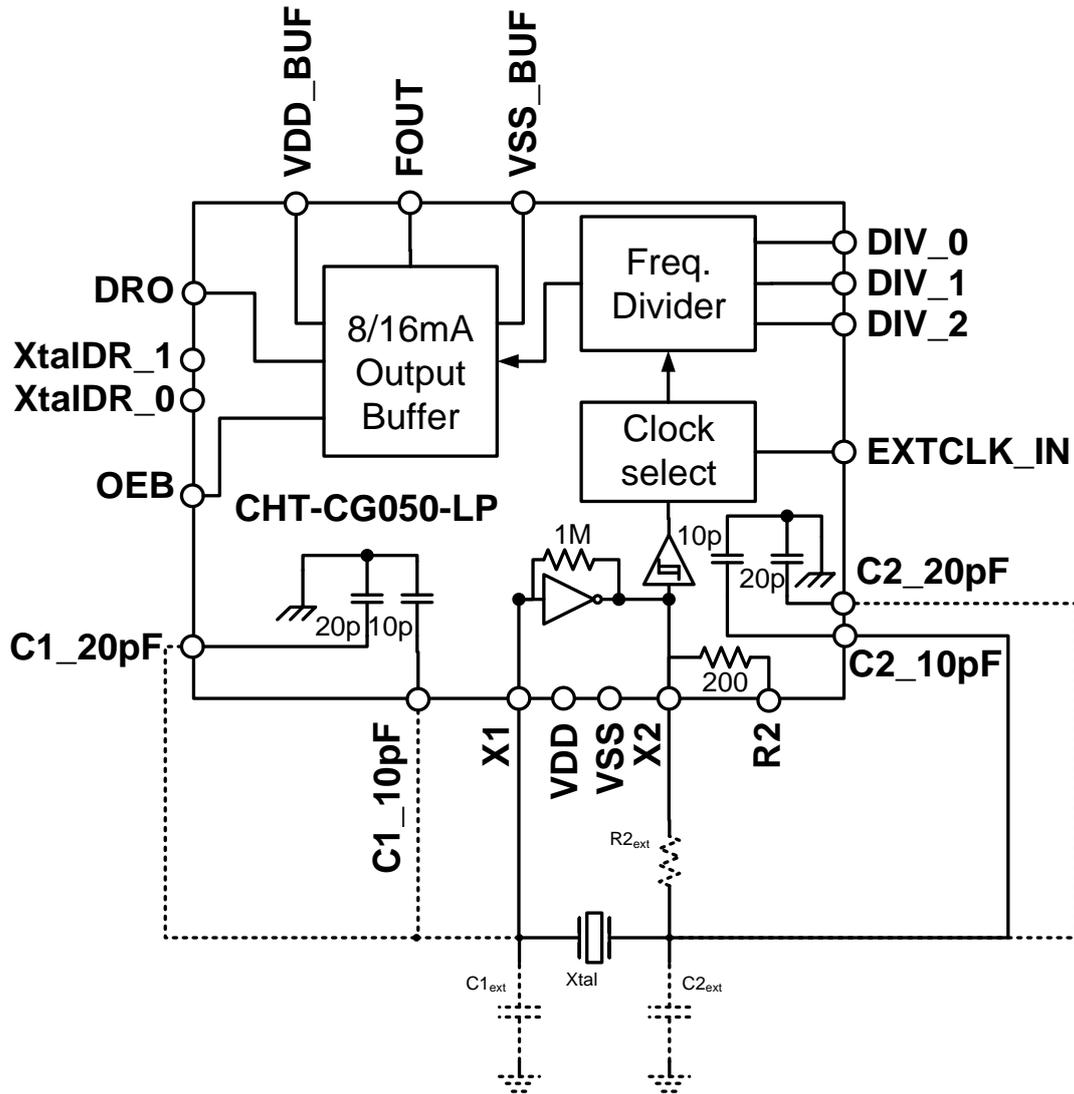
Features

- Power supply:
 - 5V +/-10% (1MHZ – 50MHZ)
 - 3.3V +/-10% (1MHZ – 30MHZ)
- Qualified from -55 to +225°C (Tj)
- Two input sources: crystal (1 to 50 MHz), external clock (DC to 50MHz)
- Operates with 32.768kHz crystals
- Programmable frequency divider: F_{in} , $F_{in}/2$, $F_{in}/4$, $F_{in}/8$, $F_{in}/16$, $F_{in}/32$, $F_{in}/256$ and $F_{in}/512$
- Programmable output driver:
 - High impedance
 - 8mA/16mA drive capability
- Programmable crystal drive
- Built-in capacitors (10pF and/or 20pF)
- Available in bare die and in hermetically sealed Ceramic TDFP16 package
- Validated at 225°C for 1000 hours (and still on-going)

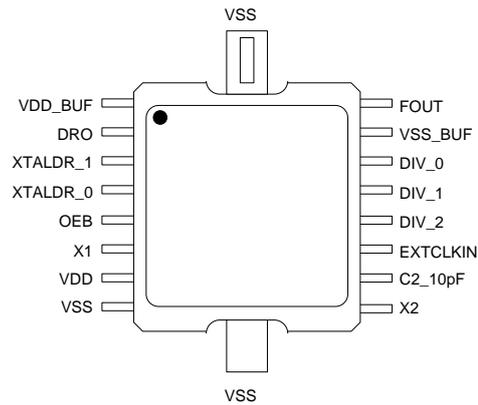
Applications

- Clock buffer & clock generation in down-hole tools, aerospace, defense and HiRel applications

Functional Block Diagram



Package and Pin Description



| Pin # (TDFP16) | Pin Name | Description |
|-------------------|-----------|--|
| 1 | VDD_BUF | Output buffer power supply terminal. ¹ |
| 2 | DRO | Selection digital input pin for the output buffer strength: DRO=0 → 16mA buffer; DRO=1 → 8mA buffer. Features a built-in pull-down resistor (50kΩ Typ.) |
| 3 | XTALDR_1 | Selection digital input pin for the crystal drive circuitry (including the selection between internal and external clock). Refer to the text and truth table for use. Features an internal pull-down resistor (50kΩ Typ.). |
| 4 | XTALDR_0 | Selection digital input pin for the crystal drive circuitry (including the selection between internal and external clock). Refer to the text and truth table for use. Features an internal pull-up resistor (50kΩ Typ.). |
| 5 | OEB | Output Enable digital input: When driven LOW, output is enabled, When driven HIGH, output is at high impedance. Features a built-in pull-down resistor (50kΩ Typ.) |
| 6 | X1 | Input of crystal driver. <u>Built-in 10pF capacitor (C1_10pF) hard-wired connected to this pin.</u> |
| 7 | VDD | Circuit core power supply terminal ¹ . |
| 8 | VSS | Circuit core ground terminal ¹ . |
| 9 | X2 | Output of crystal driver |
| 10 | C2_10pF | Optional built-in 10pF capacitor with a common terminal connected to VSS. |
| 11 | EXTCLK_IN | Input for an external clock source. Features an internal pull-down resistor (50kΩ Typ.). |
| 12 | DIV_2 | Selection bit of the frequency division factor - digital input - MSB |
| 13 | DIV_1 | Selection bit of the frequency division factor - digital input. |
| 14 | DIV_0 | Selection bit of the frequency division factor - digital input - LSB Note: Each DIV_n input pin features a built-in pull-down resistor (50kΩ Typ.) setting the frequency division rate to Fin:1 by default when DIV_n pins are left unconnected |
| 15 | VSS_BUF | Output buffer ground terminal ¹ . |
| 16 | FOUT | Output signal. |
| NA | R2 | Optional built-in 200 ohms resistance with a common terminal connected to X2. <u>Not available in TDFP16.</u> |
| NA | C2_20pF | Optional built-in 20pF capacitor with a common terminal connected to VSS. <u>Not available in TDFP16.</u> |
| NA | C1_20pF | Optional built-in 20pF capacitor with a common terminal connected to VSS. <u>Not available in TDFP16.</u> |
| NA | C1_10pF | Optional built-in 10pF capacitor with a common terminal connected to VSS. <u>Connected to X1 pin in TDFP16.</u> |

¹ VDD_BUF and VDD are internally connected; VSS_BUF and VSS are internally connected. Vertical large package leads and package heatsink (exposed pad) are internally connected to VSS

Configuration Examples & Minimum Connections

| Pin Name | Minimum configuration: 16mA Buffer; div rate=1; crystal mode with Ron=400Ω | Ext Clock configuration | 8 mA Buffer with 512 div. rate configuration crystal mode with Ron=400Ω |
|-----------------------------|--|-----------------------------|--|
| VDD_BUF | Connected to positive power supply | | |
| VSS_BUF | Connected to negative power supply | | |
| VDD | Connected to positive power supply | | |
| VSS | Connected to negative power supply | | |
| X1 | Connected to crystal | | |
| X2 | Connected to crystal | | |
| FOUT | Clock output | | |
| C2_10pF | Connected to crystal | | |
| DIV_0 | Left unconnected: Division rate = 1 | | Connected to power supply |
| DIV_1 | | | |
| DIV_2 | | | |
| DRO | Left unconnected: Buffer strength = 16mA | | Connected to power supply |
| XTALDR_0 | Left unconnected: Crystal mode enabled with min crystal driver strength ² | Connected to ground | Left unconnected: Crystal mode enabled with min crystal driver strength ² |
| XTALDR_1 | | Left unconnected | |
| OEB | Left unconnected: Output enabled | | |
| EXTCLK_IN | Left unconnected | Connected to external clock | Left unconnected |
| Total nbr of connected pins | 8 | 10 | 12 |

² Add 1 or 2 more connections if a different crystal drive is required

Absolute Maximum Ratings

Supply Voltage V_{DD} to GND -0.5 to 6.0V
Voltage on any Pin to GND -0.5 to $V_{DD}+0.3V$

Operating Conditions

Supply Voltage V_{DD} to GND 3.3V to 5V
Junction temperature -55°C to +225°C

ESD Rating

Human Body Model CLASS 2 (>2KV)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Frequent or extended exposure to absolute maximum rating conditions or above may affect device reliability.

DC Electrical Characteristics

 Unless otherwise stated: $V_{DD}=5V$, $T_j=25^\circ C$. **Bold underlined** values indicate values over the whole temperature range ($-55^\circ C < T_j < +225^\circ C$).

| Parameter | Condition | Min | Typ | Max | Units |
|---|--|--------------------|-------|--------------------|---------------|
| Supply voltage V_{DD} | | <u>2.97</u> | | <u>5.5</u> | V |
| Current consumption I_{dd} (XTALDR_0=1, XTALDR_1=0) | $V_{DD}= 3.3V$, $F_{IN} = 10MHz$, $C_L = 0pF$ OEB = LOW, DRO = LOW | | | <u>0.82</u> | mA |
| | $V_{DD}= 3.3V$, $F_{IN} = 16MHz$, $C_L = 0pF$ OEB = LOW, DRO = LOW | | | <u>1.25</u> | |
| | $V_{DD}= 3.3V$, $F_{IN} = 20MHz$, $C_L = 0pF$ OEB = LOW, DRO = LOW | | | <u>1.51</u> | |
| | $V_{DD}= 3.3V$, $F_{IN} = 20MHz$, $C_L = 22pF$ OEB = LOW, DRO = LOW | | | <u>3.47</u> | |
| | $F_{IN} = 16MHz$, $C_L = 0pF$ OEB = LOW, DRO = LOW | | | <u>2.2</u> | |
| | $F_{IN} = 27MHz$, $C_L = 0pF$ OEB = LOW, DRO = LOW | | | <u>3.51</u> | |
| | $F_{IN} = 40MHz$, $C_L = 0pF$ OEB = LOW, DRO = LOW | | | <u>5.04</u> | |
| | $F_{IN} = 40MHz$, $C_L = 22pF$ OEB = LOW, DRO = LOW | | | <u>9.5</u> | |
| | $F_{IN} = 27MHz$, OEB = HIGH | | | <u>0.67</u> | |
| Minimum HIGH level output voltage V_{OH} | I _{source} =16mA | <u>4.67</u> | | | V |
| Maximum LOW level output voltage V_{OL} | I _{sink} =16mA | | | <u>0.30</u> | V |
| Minimum HIGH level input voltage V_{IH} (EXTCLK_IN pin) | | <u>3.15</u> | | | V |
| Maximum LOW level input voltage V_{IL} (EXTCLK_IN pin) | | | | <u>1.35</u> | V |
| Xtal driver On-Resistance | XTALDR_0=1, XTALDR_1=0 | | 740 | | Ω |
| | XTALDR_0=0, XTALDR_1=1 | | 380 | | Ω |
| | XTALDR_0=1, XTALDR_1=1 | | 200 | | Ω |
| Internal capacitors | | | | | |
| Initial accuracy | | | 17 | | % |
| Temperature drift | $\Delta T = 225^\circ C - 25^\circ C$ | | 0.6 | | % |
| TC1 | $C(T) = C(T_0) [1+TC1.(T-T_0)+$ | | 0.023 | | $10^{-3}/K$ |
| TC2 | $TC2.(T-T_0)^2]$ | | 0.013 | | $10^{-6}/K^2$ |

AC Electrical Characteristics

Unless otherwise stated: $V_{DD}=5V$, $T_j=25^{\circ}C$. **Bold underlined> values indicate values over the whole temperature range ($-55^{\circ}C < T_j < +225^{\circ}C$).**

| Parameter | Condition | Min | Typ | Max | Units |
|---|--|------------------------------|-----------|------------------|-------|
| Frequency range F_{IN} | $V_{DD} = 5V$ | <u>1</u> ³ | | <u>50</u> | MHz |
| | $V_{DD} = 3.3V$ | <u>1</u> ³ | | <u>30</u> | |
| Duty cycle @ 50% V_{DD} DC^4_5 | $F_{IN}=1MHz, V_{DD} = 5V$ | | 50/50 | | % |
| | $F_{IN}=27MHz, V_{DD} = 5V$ | | 51.7/48.3 | | |
| | $F_{IN}=35MHz, V_{DD} = 5V$ | | 52/48 | | |
| Output rise time ⁶ 10% to 90% V_{DD} t_r | $DRO=0, Z_{LOAD} = 1M\Omega // 22pF$ | | 2.3 | | ns |
| | $DRO=0, Z_{LOAD} = 600\Omega // 15pF$ | | 1.9 | | |
| Output fall time ⁶ 10% to 90% V_{DD} t_f | $DRO=0, Z_{LOAD} = 1M\Omega // 22pF$ | | 2.2 | | ns |
| | $DRO=0, Z_{LOAD} = 600\Omega // 15pF$ | | 1.8 | | |
| Oscillation established after V_{DD} goes high ⁷ $t_{power-on}$ | V_{DD} from 0 to 5V | | 1.9 | | ms |
| Oscillation established after XTALDR_n goes HIGH ⁷ $t_{start-up}$ | $V_{DD} = 5V$ XTALDR_n from LOW to HIGH | | 0.4 | | ms |
| Equivalent capacitance at driver input (X1) ⁸ C_{X1} | Freq= 1MHz | | 0.72 | | pF |
| Equivalent capacitance at driver output (X2) ⁸ C_{X2} | Freq= 1MHz | | 0.71 | | pF |
| Equivalent capacitance at limiting resistor (R2) ⁸ C_{R2} | Freq= 1MHz | | 0.6 | | pF |

³ CG50LP also supports 32.768kHz crystal operation; refer to Circuit Functionality section for info about crystal network

⁴ Duty cycle is measured with a unitary division factor and $Z_{LOAD} = 1050\Omega // 22pF$.

⁵ Depends on crystal characteristics and on $R2_{EXT}$ value.

⁶ Depends on load conditions and **DRO** setting.

⁷ Depends on used crystal and **XTALDR_0**, **XTALDR_1** settings.

⁸ Valid for die version

Typical Performance Characteristics

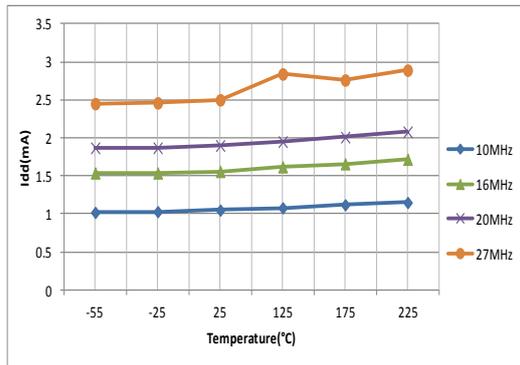


Figure 1: Current consumption ($V_{DD} = 5V$, $OEB = LOW$, $C_L = 0pF$, $XTALDR_0=1$, $XTALDR_1=0$)

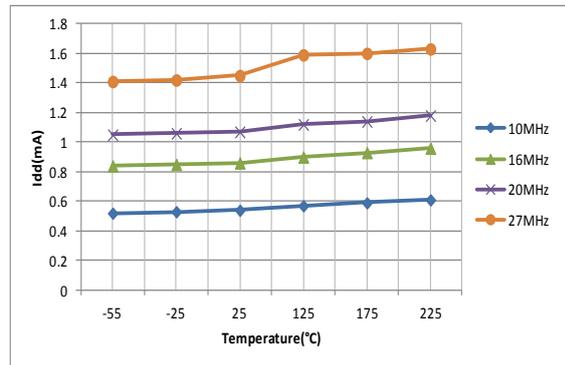


Figure 2: Current consumption ($V_{DD} = 3.3V$, $OEB = LOW$, $C_L = 0pF$, $XTALDR_0=1$, $XTALDR_1=0$)

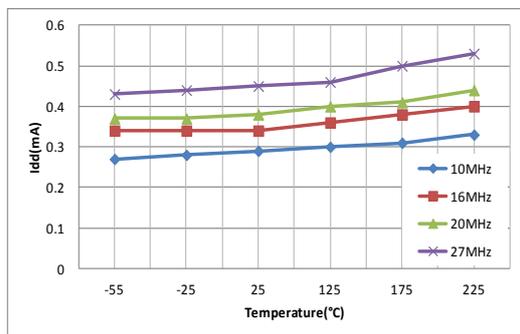


Figure 3: Current consumption ($V_{DD} = 5V$, $OEB = HIGH$, $XTALDR_0=1$, $XTALDR_1=0$)

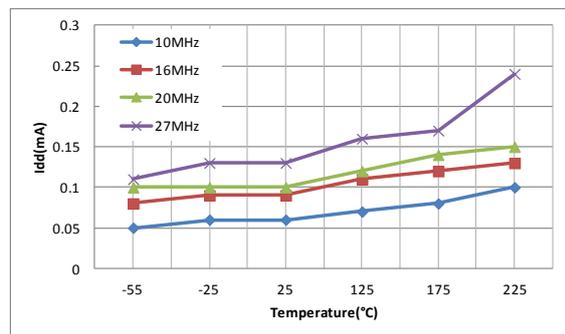


Figure 4: Current consumption ($V_{DD} = 3.3V$, $OEB = HIGH$, $XTALDR_0=1$, $XTALDR_1=0$)

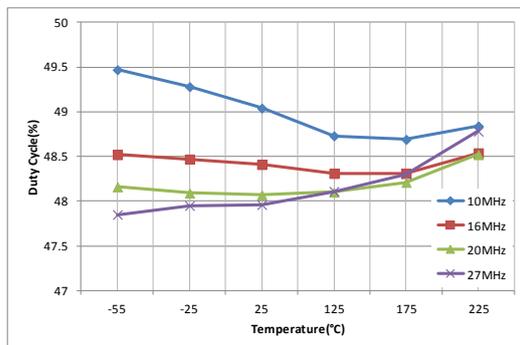


Figure 5: Duty cycle ($V_{DD}=5V$)

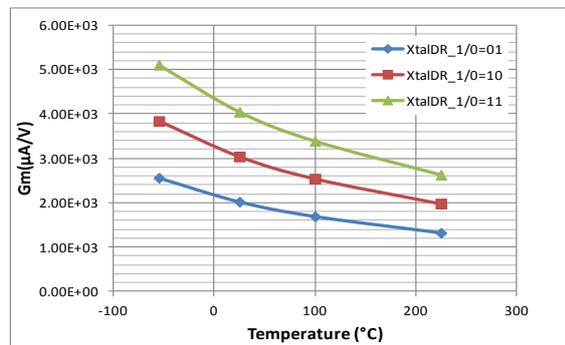


Figure 6: Crystal driver transconductance ($V_{DD}=5V$)

Circuit Functionality

Operating conditions

The CHT-CG-50LP is qualified for supply voltages ranging from 3.0V up to 5.5V.

The operating temperature range extends from -55°C to +225°C.

Crystal driver

The pins **XTALDR_0** and **XTALDR_1** allow to set-up the crystal driver strength or to select the external input clock

| XTALDR_0 | XTALDR_1 | Internal State |
|----------------------|----------------------|---|
| 0 | 0 | Crystal driver disabled. External clock used. |
| 1 (standard mode) | 0 (standard mode) | Min crystal drive (Ron ≅ 740Ω) |
| 0 | 1 | Medium crystal drive (Ron ≅ 380Ω) |
| 1 | 1 | Max crystal drive (Ron ≅ 200Ω) |

XTALDR_0 is internally pulled up (50kΩ Typ.) and XTALDR_1 internally pulled down (50kΩ Typ.).

Reducing the drive strength of the crystal driver will help reducing the current consumption of the device

Frequency divider

Eight division factors (1, 2, 4, 8, 16, 32, 256 and 512) can be selected through the digital control lines **DIV_0**, **DIV_1** and **DIV_2**.

| DIV_0 | DIV_1 | DIV_2 | Division rate |
|-------|-------|-------|---------------|
| 0 | 0 | 0 | 1 |
| 1 | 0 | 0 | 2 |
| 0 | 1 | 0 | 4 |
| 1 | 1 | 0 | 8 |
| 0 | 0 | 1 | 16 |
| 1 | 0 | 1 | 32 |
| 0 | 1 | 1 | 256 |
| 1 | 1 | 1 | 512 |

The 3 digital inputs pins are internally pulled down, enabling a frequency division rate of 1 by default when the pins are left unconnected (internally pulled down (50kΩ Typ.).

Output buffer

The output buffer has dedicated power supply terminals, allowing the system designer to properly decouple them

The output buffer features 2 fixed output strengths of 8mA and 16mA which can be selected from the digital input pin DRO. This enables the CHT-CG-50-LP to optimize the output signal integrity depending on the type of output load. The default output strength is 16mA when DRO is left unconnected (internally pulled down, 50kΩ Typ.). When HIGH (connected to VDD), the output strength is 8mA.

The output buffer can be set in high-impedance by setting OEB pin to HIGH.

32 KHz operation

The figure below illustrates the recommended configuration for CG50LP operation with a 32KHz crystal

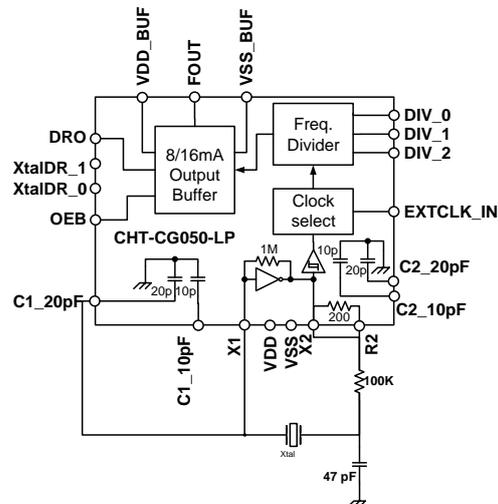
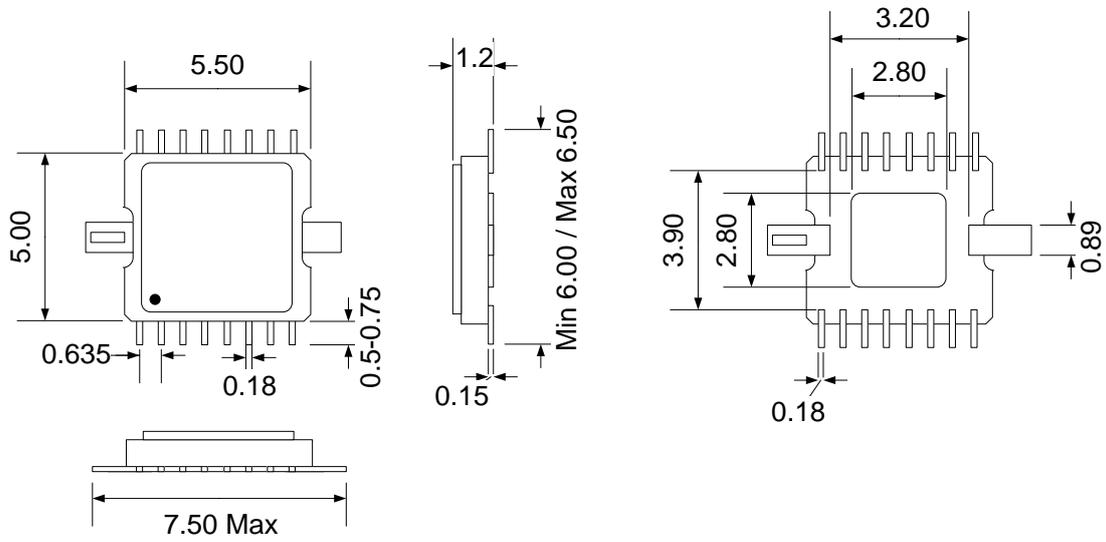


Figure 7. Configuration for 32KHz operation

Typical application

The CHT-CG-50LP offers the final user several possible configurations depending upon the characteristics of the target application.

Package Dimensions (TDFP16)


Physical dimensions (mm +/- 10%)

Ordering Information

| Product Name | Ordering Reference | Package | Marking |
|--------------|-----------------------|---------|--------------|
| CHT-CG50LP | CHT-PUL9560A-TDFP16-T | TDFP16 | CHT-PUL9560A |

Contact

| | |
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