# SFP 1.25G Transceiver MSFP-1.25G-T

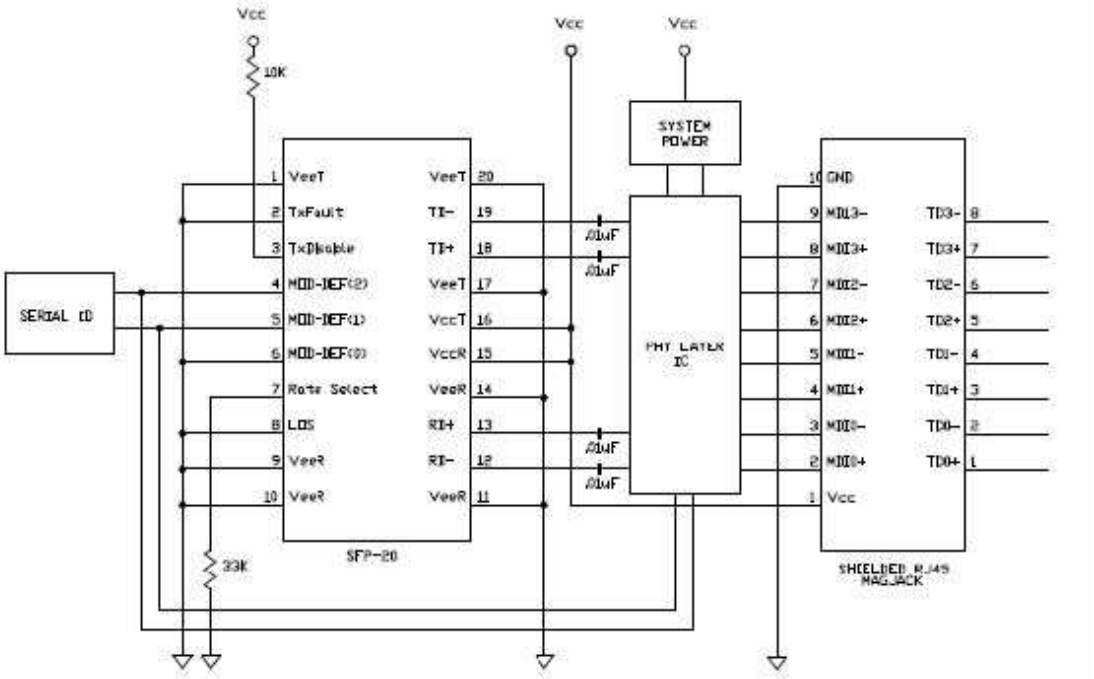
## Features

- Compliant with MSA SFP specification
- Die cast metal housing
- Single +3.3V power supply
- Serial ID functionality
- Bail latch style ejector mechanism
- TDR functionality support
- Auto MDI/MDIX crossover
- Shunt Auto Transformer
- Compatible with CAT 5 cable in excess of 100M in length
- 10/100/1000 BASE-T Auto-Negotiation in host systems with SGMII interface
- Compliant with the Gigabit Ethernet and 1000-BASE-T standards as specified in IEEE 802.3-2002 and IEEE 802.3ab
- Compatible with IEEE 802.3u and IEEE 802.3z

## Operate condition

| PARAMETER | SYMBOL | MIN | NOM | MAX | UNIT | CONDITION |
|---|---|---|---|---|---|---|
| Operating Voltage | VccT, VccR | 3.1 | 3.3 | 3.5 | V | |
| Current | I | 300 | | 400 | mA | Steady State |
| Surge Current | Isurge | | | 30 | mA | Hot Plug |
| Power Consumption | P | | | 1 | W | |
| Storage Temperature | T | -40 | | 85 | C | |
| Operating Temperature | T | 0 | | 70 | C | |
| Relative Humidity | RH | 5 | | 95 | % | |

## BLOCK DIAGRAM




The RJ45 Gigabit Ethernet pluggable transceiver module is a high performance integrated duplex data link for bi-directional communication over CAT 5 unshielded twisted pair copper cable. It is compliant with the MSA Small Form Factor Pluggable (SFP) specification. The RJ45 transceiver is specifically designed for high speed Gigabit Ethernet data links at 1.25 Gbaud. The transceiver is hot pluggable and operates at +3.3V.

### Host Board Interface

The table below shows the host interface signals and their functions.

**Pin Function Definitions.**

| PIN NO. | NAME | FUNCTION | SEQ. | NOTES |
|---|---|---|---|---|
| PIN 1 | VeeT | Transmitter Ground | 1 | VeeT and VeeR are connected in SFP. |
| PIN 2 | TX_FAULT | Transmitter Fault Indication | 3 | Not Implemented. Tied to VeeT in SFP. |

| | | | | |
|---|---|---|---|---|
| PIN 3 | TX_DISABLE | Transmitter Disable | 3 | See TX Disable. |
| PIN 4 | MOD DEF (2) | Module Definition 2 | 3 | Data Line for Serial ID and Bidirectional Data Transfer bus. |
| PIN 5 | MOD DEF (1) | Module Definition 1 | 3 | Clock Line for Serial ID and Bidirectional Data Transfer bus. |
| PIN 6 | MOD DEF (0) | Module Definition 0 | 3 | Tied to Vee in SFP. |
| PIN 7 | RATE SELECT | Not Implemented | 3 | Not implemented. 33K pulldown to Vee in SFP. |
| PIN 8 | LOS | Loss of Signal | 3 | See LOS option. |
| PIN 9 | VeeR | Receiver Ground | 1 | VeeT and VeeR are connected in SFP. |
| PIN 10 | VeeR | Receiver Ground | 1 | VeeT and VeeR are connected in SFP. |
| PIN 11 | VeeR | Receiver Ground | 1 | VeeT and VeeR are connected in SFP. |
| PIN 12 | RD- | Inverted Received Data out | 3 | AC coupled 100 ohm differential high speed data lines. |
| PIN 13 | RD+ | Non-Inverted Received Data out | 3 | AC coupled 100 ohm differential high speed data lines. |
| PIN 14 | VeeR | Receiver Ground | 1 | VeeT and VeeR are connected in SFP. |
| PIN 15 | VccR | Receiver Power | 2 | VccR and VccT are connected in SFP. |
| PIN 16 | VccT | Transmitter Power | 2 | VccR and VccT are connected in SFP. |
| PIN 17 | VeeT | Transmitter Ground | 1 | VeeT and VeeR are connected in SFP. |
| PIN 18 | TD+ | Non-inverted Data In | 3 | AC coupled 100 ohm differential high speed data lines. |
| PIN 19 | TD- | Inverted Data In | 3 | AC coupled 100 ohm differential high speed data lines. |

| | | | | |
|---|---|---|---|---|
| PIN 20 | VeeT | Transmitter Ground | 1 | VeeT and VeeR are connected in SFP. |

### TX Disable

Pulled up to Vcc with 10K ohm resistor in SFP. For normal operation the Host must hold the TX Disable input low. An open or high input to the SFP holds the PHY in reset. The reset condition is removed 175ms after TX Disable goes low.

### LOS Option

The SFP MSA specification defines a pin called LOS to indicate loss of signal to the motherboard. This is an output of the SFP module and an input to the motherboard. Eflow's 1000Base-T copper SFP Transceiver normally comes with the LOS signal connected to ground. The transceiver can be ordered with this signal connected to the LED_Link1000 output of the PHY to indicate a good link

### Bi-directional Data Transfer Bus

The Eflow 1000 Base-T Copper SFP Transceiver supports a bi-directional data transfer bus (BDT) to communicate with the PHY. The BDT operates with the same serial data line (SDA -MOD_DEF[2]) and serial clock line (SCL MOD_DEF[1]) that are used for serial identification. The device address for the PHY is 1010110X binary. The SDA is a bi-directional line while the SCL line is not. Both of the bus interface lines are high when the bus is inactive. The PHY operates as the Slave port of the bus interface and all references to Slave refer to the PHY.

The PHY BDT features are

7 bit device addresses / 8 bit data transfers

100 Kbps mode

400 Kbps mode

### Termination Circuits

Inputs to the transceiver are AC coupled and internally terminated through 50 ohms. These modules can operate with PECL or ECL logic levels. The input signal must have at least a 325mV peak-to-peak (single ended) signal swing. Output from the receiver section of the module is also AC coupled and is expected to drive a 50 ohm load. Different termination strategies may be required depending on the particular Serializer/Deserializer chip set used. The transceiver is designed with AC coupled data inputs and outputs to

provide the following advantages:

Close positioning of SERDES with respect to transceiver; allows for shorter line lengths and at Gigabit speeds reduces EMI.

Minimum number of external components. Internal termination reduces the potential for unterminated stubs which would otherwise increase jitter and reduce transmission margin.

Subsequently, this affords the customer the ability to optimally locate the SERDES as close to the transceiver as possible and save valuable real estate. At Gigabit rates this can provide a significant advantage resulting in better transmission performance and accordingly better signal integrity.

## Power Coupling

A suggested layout for power and ground connections is given in *Figure 1* below. Connections are made via separate voltage and ground planes. The mounting posts are at case ground and should not be connected to circuit ground. The ferrite bead should provide a real impedance of 50 to 100 ohms at 100 to 1000 MHz. Bypass capacitors should be placed as close to the 20 pin connector as possible.

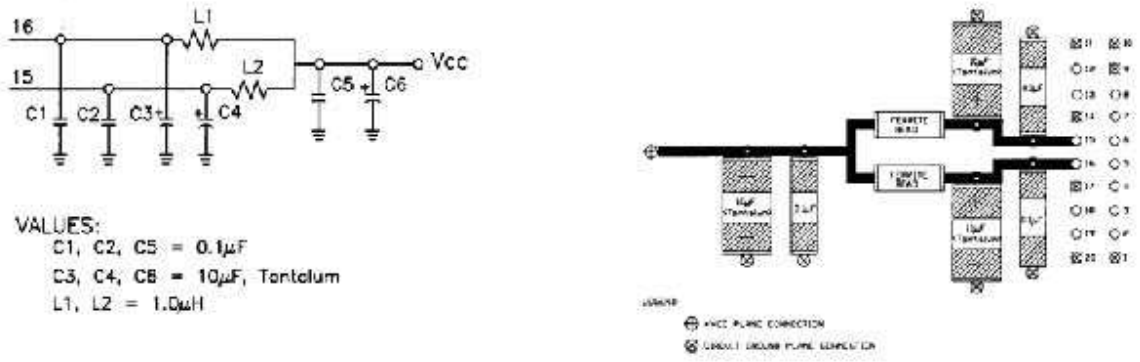



**Figure 1: Suggested Power Coupling**

## Mechanical Description

The transceiver shall be compliant with common SFP mechanical outline

### 1000Base-T SFP Transceiver Dimensions

Figure 2 Illustrates the Mechanical Dimensions of the Transceiver

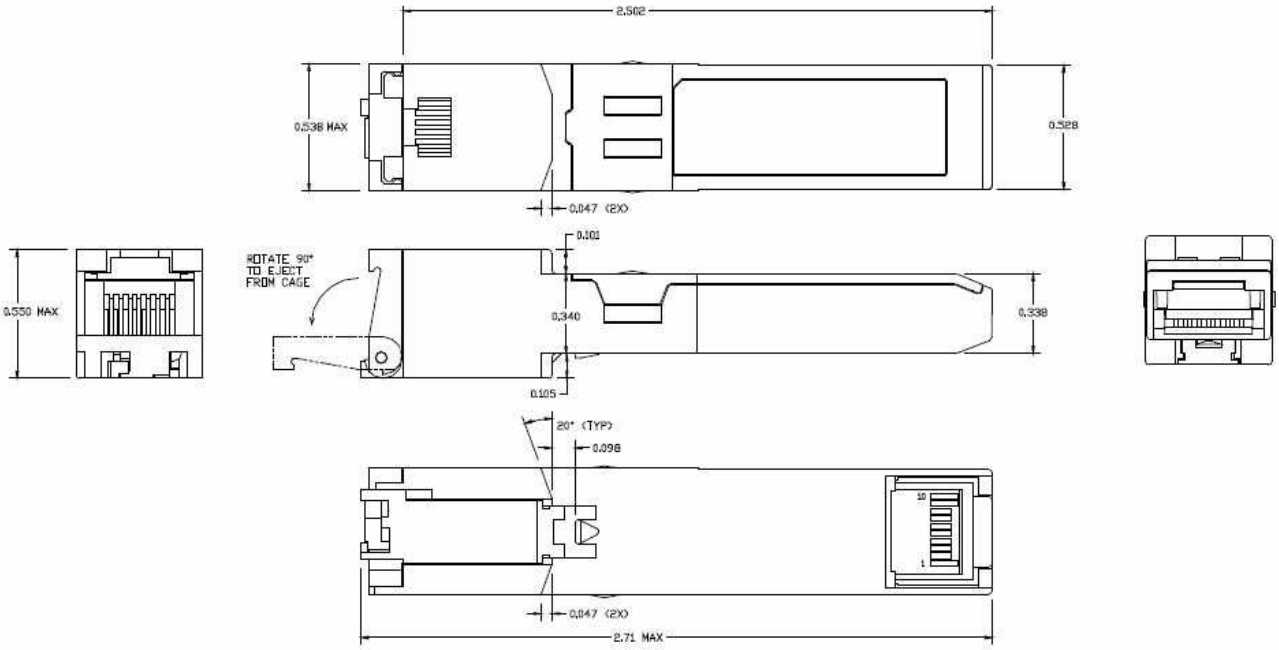



**Figure 2 Mechanical Dimensions of Transceiver**

## Mating of SFP Transceiver to SFP Host Board Connector

The pads on the PCB of the SFP transceiver shall be designed for a sequenced mating as follows:

First mate: Ground contacts Second mate: Power contactsThird mate: Signal contacts

The SFP MSA specification for a typical contact pad plating for the PCB is 0.38 micrometers minimum hard gold over 1.27 micrometers minimum thick nickel. To ensure the long term reliability performance after a minimum of 50 insertion removal cycles, the contact plating of the transceiver is 0.762 micron (30 microinches) over 3.81 micron (150 microinches) of Ni on Cu contact pads.

## RJ45 Connector

RJ45 connector shall support shielded and unshielded cables. Also, the connector is mechanically robust enough and designed to prevent loss of link, when the cable is positioned or moves in different angles. The connector shall pass the “wiggle” RJ45 connector operational stress test. During the test, after the cable is plugged in, the cable is moved in circle to cover all 360 deg in the vertical plane, while the data traffic is on. There shall be no link or data loss.