Document No: AX6800x/V1.02/05/28/2015

Features

- Single chip microcontroller with 2-port (AX68002) /4-Port (AX68004) USB KVM Switch

- **CPU for Application**
  - 8-bit pipelined RISC, single cycle per instruction operating up to 96MHz and 100% software compatible with standard 8051/80390
  - Supports power management unit with deep sleep mode, programmable watchdog timer, three 16-bit timer/counters, and millisecond timer
  - Supports CPU Debugger for connecting to In-Circuit Emulation (ICE) adaptor
  - Supports DMA Controller (7 DMA channels) and memory arbiter for fast data movement during network protocol stack processing and peripheral communications
  - 1 external interrupt sources with 2 priority levels

- **Program/Data and Flash Memory**
  - On-chip 8KB SRAM for CPU program code mirroring
  - Supports In-System Programming (ISP) for initial Flash memory programming via UART or ICE adaptor
  - Supports reprogrammable boot code and In-Application Programming (IAP) to update boot code or run-time firmware through USB or UART interface
  - On-chip 32KB data memory for CPU and packet buffering
  - On-chip 128KB Flash memory for CPU program code
  - On-chip 1KB Flash Information Page for Hardware Configuration
  - Supports Page architecture for flash erase
  - Minimum 100,000 flash program/erase cycles
  - Minimum 10 years flash data retention under maximum 20 times pre-cycles

- **USB Interfaces**
  - Supports 2/4 multi-addressable Device Controllers and compliant with USB Spec 2.0 Full speed
  - Build-in one USB host controller and one USB root hub that supports four downstream ports and each compliant with USB2.0 Full/Low speed
  - Supports Control, Bulk, Interrupt, and Isochronous transfer types.
  - Support controllable D+ pull-up resistance for upstream ports
  - Support controllable D+/- pull-down resistance for downstream ports
  - Support Burst mode transfer for BULK data transfer in Device Controller
  - Supports the downstream SOF synchronization with selected upstream port for ISO data transfer automatically

- **Peripheral Communication Interfaces**
  - 2 UART interface (1 supporting DMA mode, Modem control, remote wake-up and up to 921.6Kbps baud)
  - 2 High Speed SPI interface with DMA mode (1 master and 1 slave mode)
  - I^2C interface with DMA mode (1 master with EDID Console and 4 slave mode with EDID Slave)
  - 2 PS/2 Host interfaces
  - Up to 4 GPIO ports of 8 bits each (Supports 2 GPIO ports with de-bounce and interrupt function)
  - Programmable Buzzer function

- **Supports KVM switch functions in software**
  - Controls 2/4 computers from a single console
  - Supports PS/2 keyboard/mouse and USB keyboard/mouse
  - Supports keyboard and mouse emulation for error-free booting
  - USB device in console is transparent to computers that support most gaming/multimedia keyboards and multifunction mouse
  - Mouse sample rate on both of downstream and upstream ports is the same
  - Supports DDC (Display Data Channel) emulation and stores the console monitor's EDID (Extended Display Identification Data)
  - Two or four computers can share two or four USB downstream ports in console
  - Support maximum 7 USB devices in console, including HID, HUB, MSC and Audio Class
  - Supports touch screen, writing pad, and touch pad devices
  - Supports "push buttons" and "hot keys" switching
  - Support auto-scan mode for monitoring PC operation
- Integrates on-chip oscillator and 96MHz PLL to operate with external 12MHz crystal
- Integrates on-chip power-on reset circuit
- 64-pin QFN (AX68002)/100-pin LQFP (AX68004) RoHS compliant package
- Operating temperature range: 0 to +70 ° C

ASIX ELECTRONICS CORPORATION
4F, NO.8, Hsin Ann Rd., HsinChu Science Park, Hsin-Chu City, Taiwan, R.O.C.
TEL: 886-3-579-9500
FAX: 886-3-579-9558
http://www.asix.com.tw

Release Date: 05/28/2015

Product Description

AX6800x, Single Chip Micro-controller with USB Host and Device controller, is a System-on-Chip (SoC) solution which offers high performance CPU architecture with on-chip 128KB Flash memory as Program Memory, on-chip 32KB Data Memory for CPU, built in one Root Hub and 2/4 ports Host Controller compliant with USB2.0 Full/Low Speed Standard, 2/4 ports Device Controller compliant with USB2.0 Full Speed Standard, and rich peripheral interfaces for wide varieties of application which need bridge to the USB interface.

The CPU architecture of AX6800x utilizes the USB protocols maintenance for those upstream and downstream ports to the external USB Host and Device and performs packet translation between upstream and downstream ports. The Root Hub provided all the transactions scheduling and management with CPU to maintain to the all adapted USB devices. The Host and Device controller with DMA engine provide the data transmission between the USB bus from/to on-chip 32KB SRAM.

In addition to stand-alone application, AX6800x with USB protocol suite running on-chip and various serial host interfaces supported, High Speed UART or High Speed SPI, can be used as a data bridge from/to USB interface in an embedded system.

A 12 MHz crystal is needed for internal 96 MHz PLL to provide the 48 and 12 MHz for USB related and the typical operating frequency of AX6800x is 48 or 96MHz. AX6800x also integrates power-on reset circuit on-chip that can simplify external reset circuit on PCB and prevent the program code corrupt in Flash memory.

AX6800x is available in 100-pin LQFP or 64-pin QFN RoHS compliant package and the recommended operating temperature range is 0 to 70℃.

AX6800x provides cost effective solution to enable simple, easy, and low cost integration capability for KVM applications. It could also provide highly programmable flexibility and compatibility.

Target Applications

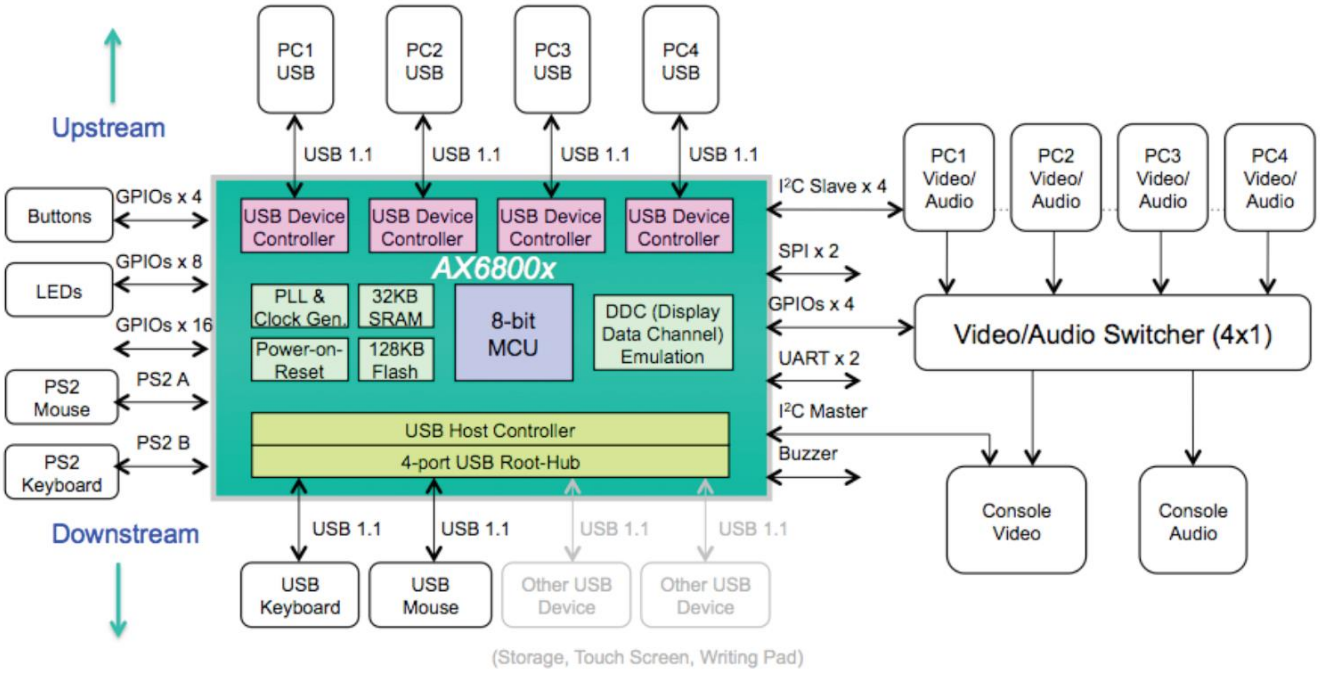


Figure 0-1: Target Application Diagram

Typical System Block Diagrams

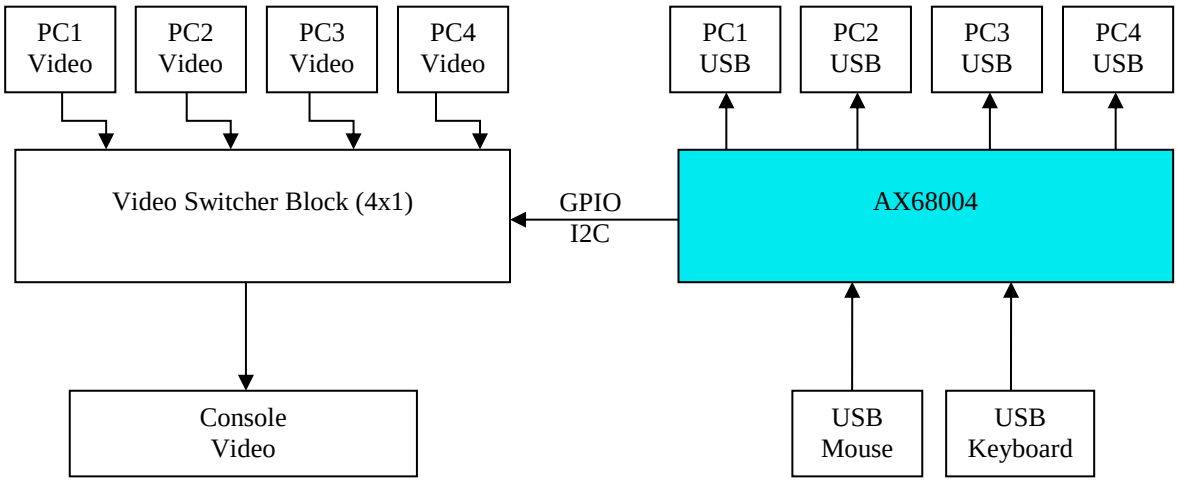


Figure 0-2: USB KVM

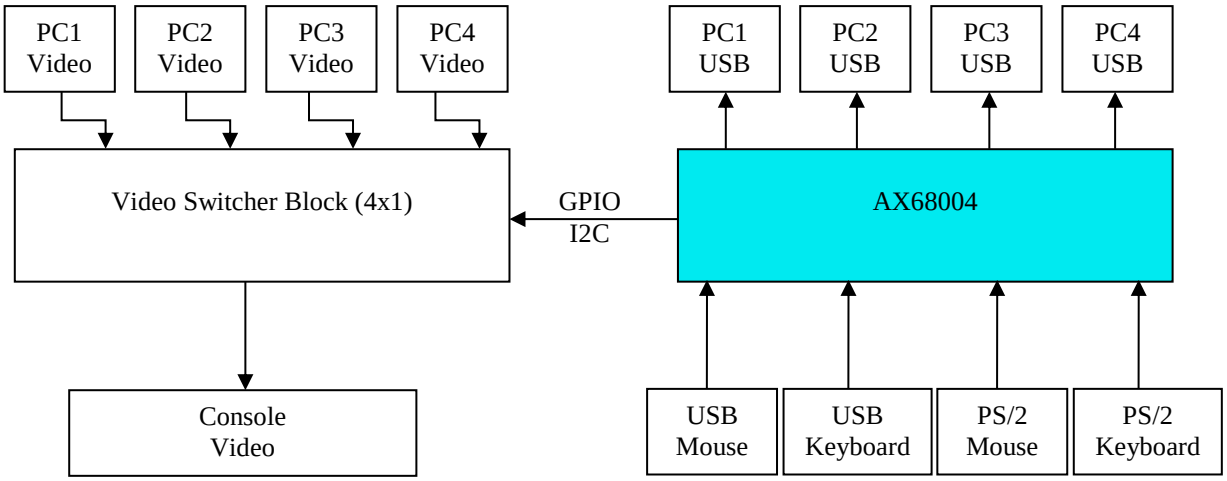


Figure 0-3: Combo KVM

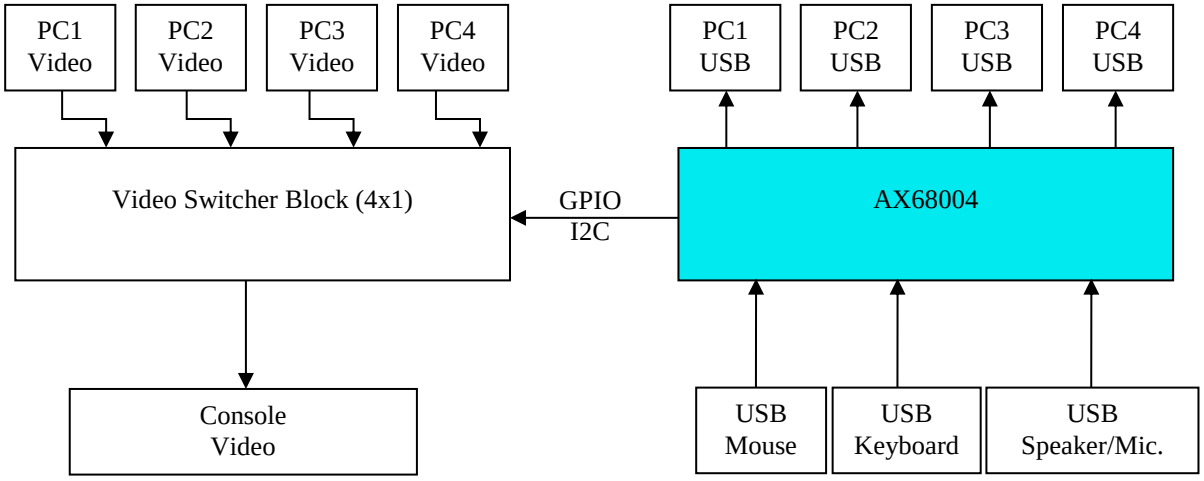


Figure 0-4: Audio USB KVM

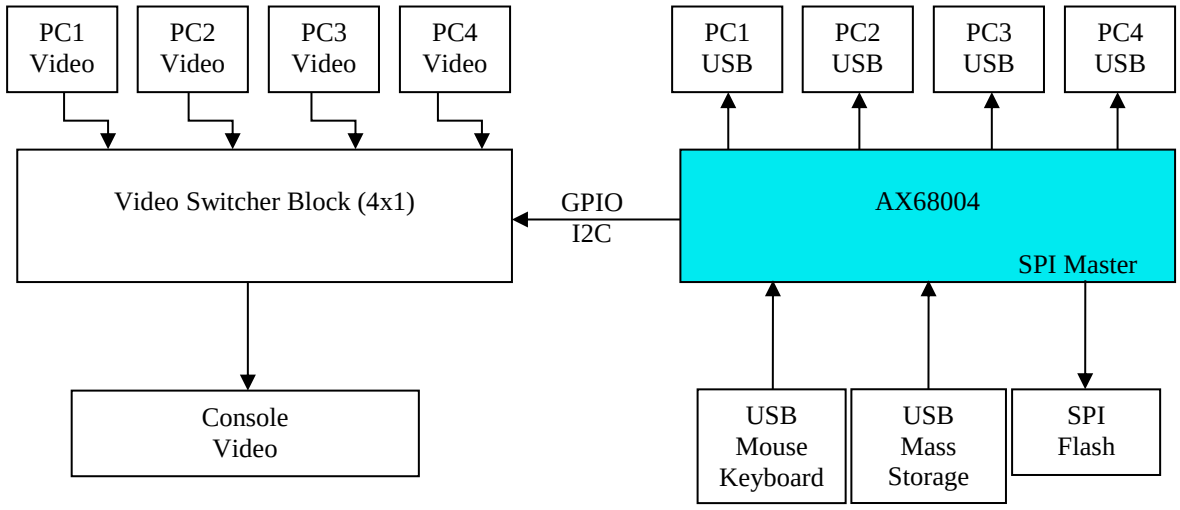


Figure 0-5: KVM with Storage

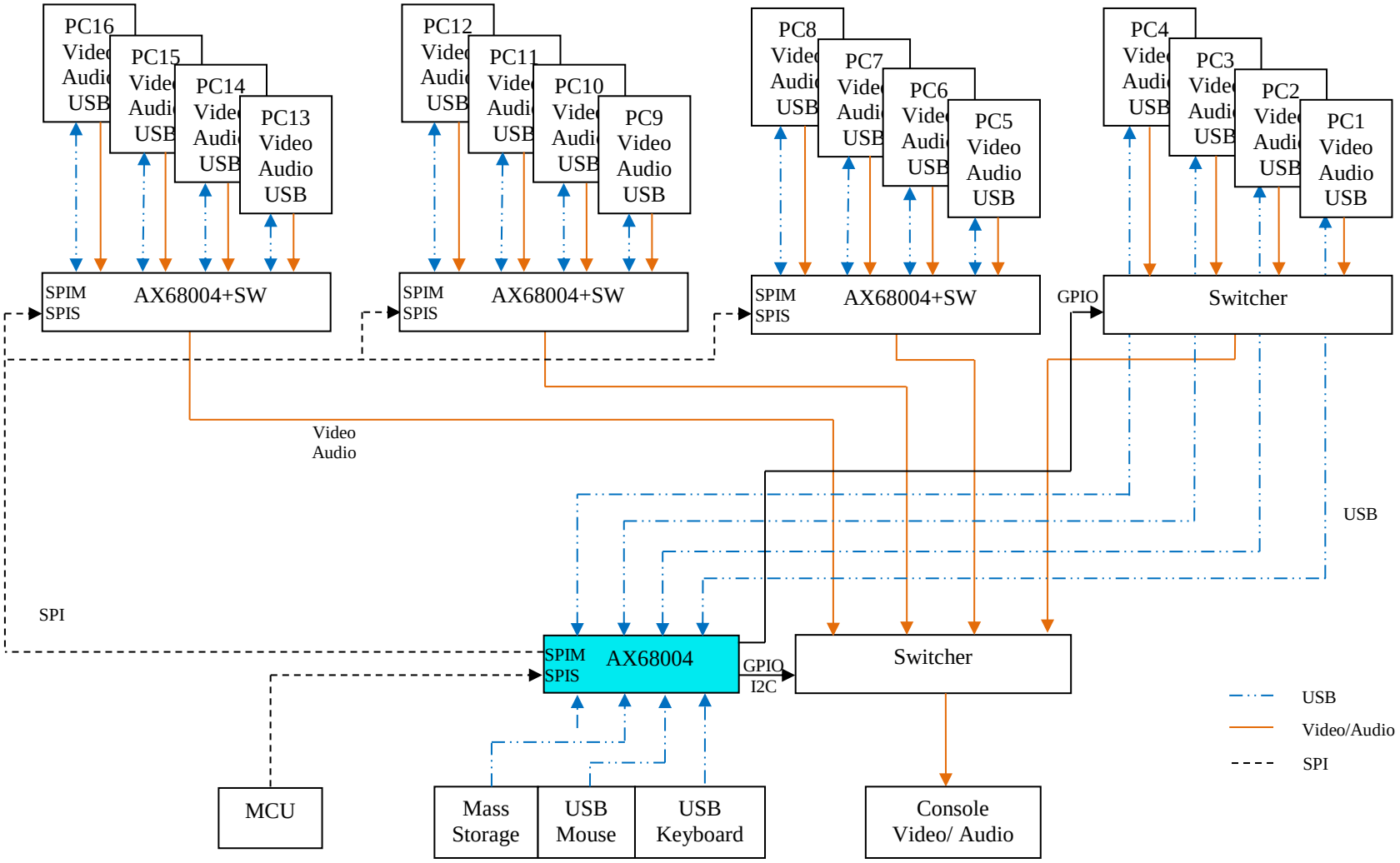
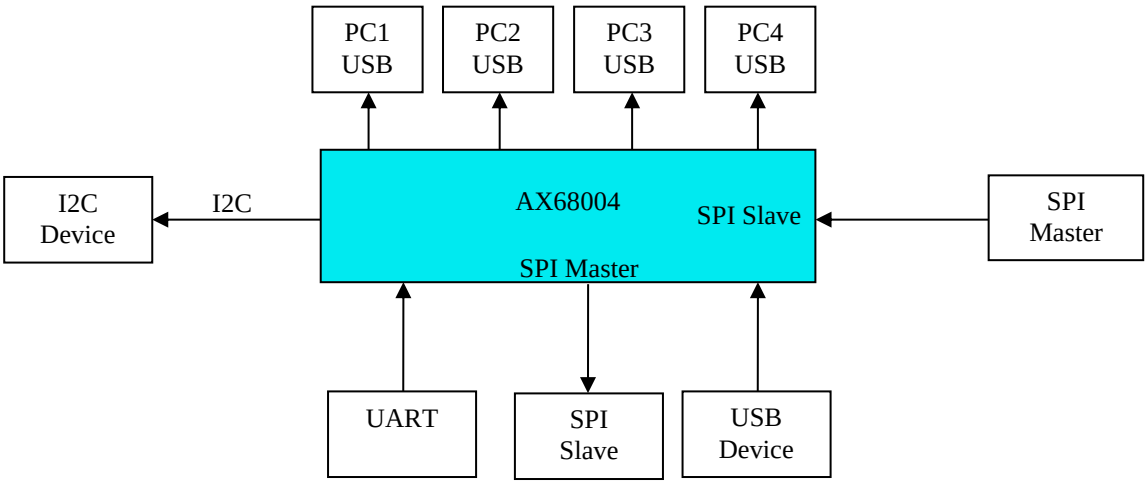


Figure 0-6: Cascade USB KVM



Note 1: USB Host to USB Host Bridging
Note 2: USB Host to USB Device Bridging
Note 3: I2C to USB Bridging
Note 4: SPI to USB Bridging
Note 5: UART to USB Bridging

Figure 0-7: USB Bridging

DISCLAIMER

No part of this document may be reproduced or transmitted in any form or by any means, electronic or mechanical, including photocopying and recording, for any purpose, without the express written permission of ASIX. ASIX may make changes to the product specifications and descriptions in this document at any time, without notice.

ASIX provides this document "as is" without warranty of any kind, either expressed or implied, including without limitation warranties of merchantability, fitness for a particular purpose, and non-infringement.

Designers must not rely on the absence or characteristics of any features or registers marked "reserved", "undefined" or "NC". ASIX reserves these for future definition and shall have no responsibility whatsoever for conflicts or incompatibilities arising from future changes to them. Always contact ASIX to get the latest document before starting a design of ASIX products.

TRADEMARKS

ASIX, the ASIX logo are registered trademarks of ASIX Electronics Corporation. All other trademarks are the property of their respective owners.

Table of Contents

1.0 INTRODUCTION 12

1.1 GENERAL DESCRIPTION 12
1.2 PRODUCT SELECTION GUIDE 12
1.3 AX6800X BLOCK DIAGRAM 13
1.4 AX6800X PINOUT DIAGRAM 14
1.5 SIGNAL DESCRIPTION 16

2.0 FUNCTION DESCRIPTION 23

2.1 CLOCK GENERATION 23
2.2 RESET GENERATION 23
2.3 CPU CORE AND DEBUGGER 24
2.3.1 CPU Core 24
2.3.2 Debugger 24
2.4 FLASH CONTROLLER AND ON-CHIP FLASH MEMORY 25
2.4.1 Program Loader 25
2.4.2 Flash Controller and In-Application Programming 25
2.4.3 In-System Programming 25
2.4.4 On-Chip Flash Memory 25
2.5 MEMORY CONTROLLER AND ON-CHIP DATA MEMORY 26
2.6 DMA CONTROLLER 26
2.7 INTERRUPT CONTROLLER 26
2.8 WATCHDOG TIMER 26
2.9 POWER MANAGEMENT UNIT 27
2.10 TIMERS AND COUNTERS 27
2.11 UARTS 27
2.12 GPIOS 28
2.13 BUZZER CONTROLLER 28
2.14 I2C CONTROLLER 28
2.15 HIGH SPEED SPI CONTROLLER 28
2.16 PS/2 CONTROLLER 29
2.17 USB ROOT HUB AND HOST CONTROLLER 29
2.18 USB DEVICE CONTROLLER 29

3.0 MEMORY MAP DESCRIPTION 30

3.1 HARDWARE CONFIGURATION WITH FLASH INFORMATION MEMORY MAP 30
3.1.1 Flag (0x00) 31
3.1.2 Multi-function Pin Setting (0x03 ~ 0x01) 31
3.1.3 Programmable USB Pull Disable (0x04) 36
3.1.4 Reserved (0x05) 36
3.2 PROGRAM MEMORY MAP 37
3.3 EXTERNAL DATA (XDATA) MEMORY MAP 37
3.4 INTERNAL DATA MEMORY AND SFR REGISTER MAP 38

4.0 ELECTRICAL SPECIFICATION 39

4.1 DC CHARACTERISTICS 39
4.1.1 Absolute Maximum Ratings 39
4.1.2 Recommended Operating Condition 39
4.1.3 Leakage Current and Capacitance 39
4.1.4 DC Characteristics of 3.3V with 5V Tolerant I/O Pins 40
4.1.5 USB Transceivers Specification 41
4.2 POWER CONSUMPTION 42
4.3 POWER-ON-RESET (POR) SPECIFICATION 43
4.4 POWER-UP/-DOWN SEQUENCE 44
4.5 AC TIMING CHARACTERISTICS 46
4.5.1 Clock Input Timing Specification 46

4.5.2 Timer 0/1/2 Interface Timing *46*
4.5.3 High Speed UART *47*
4.5.4 I2C Interface Timing *48*
4.5.5 High Speed SPI Interface Timing *49*
4.5.6 PS/2 Interface Timing *51*
4.5.7 Buzzer Interface Timing *52*

5.0 PACKAGE INFORMATION **53**

5.1 64-PIN QFN PACKAGE 53
5.2 100-PIN LQFP PACKAGE 54

6.0 ORDERING INFORMATION **56**

7.0 REVISION HISTORY **56**

List of Figures

FIGURE 0-1: TARGET APPLICATION DIAGRAM 2
FIGURE 0-2: USB KVM 3
FIGURE 0-3: COMBO KVM 3
FIGURE 0-4: AUDIO USB KVM 4
FIGURE 0-5: KVM WITH STORAGE 4
FIGURE 0-6: CASCADE USB KVM 5
FIGURE 0-7: USB BRIDGING 6
FIGURE 1-1: AX6800X BLOCK DIAGRAM 13
FIGURE 1-2: AX68002 PINOUT DIAGRAM 14
FIGURE 1-3: AX68004 PINOUT DIAGRAM 15
FIGURE 3-1: THE PROGRAM MEMORY MAP OF CPU 37
FIGURE 3-2: THE INTERNAL MEMORY MAP OF CPU 38
FIGURE 4-1: POWER-UP SEQUENCE TIMING DIAGRAM AND TABLE 44
FIGURE 4-2: POWER-DOWN SEQUENCE TIMING DIAGRAM AND TABLE 45
FIGURE 4-3: TM_CK[2:0] TIMING DIAGRAM AND TABLE 46
FIGURE 4-4: TM_GT[2:0] TIMING DIAGRAM AND TABLE 46
FIGURE 4-5: TXD1 AND RXD1 TIMING DIAGRAM 47
FIGURE 4-6: HIGH SPEED SPI MASTER CONTROLLER TIMING DIAGRAM AND TABLE 49
FIGURE 4-7: HIGH SPEED SPI SLAVE CONTROLLER TIMING DIAGRAM AND TABLE 50
FIGURE 4-8: PS2 HOST RECEIVING DATA TIMING DIAGRAM AND TABLE 51
FIGURE 4-9: PS2 HOST SENDING DATA TIMING DIAGRAM AND TABLE 51
FIGURE 4-10: BUZZER OUTPUT TIMING DIAGRAM AND TABLE 52

List of Tables

TABLE 1-1: CHIP CLOCK AND RESET PIN DESCRIPTION 16
TABLE 1-2: CHIP CONFIGURATION PIN DESCRIPTION 17
TABLE 1-3: USB TRANSCEIVER PIN DESCRIPTION 17
TABLE 1-4: USB UPSTREAM (DEVICE CONTROLLER) VBUS PIN DESCRIPTION 17
TABLE 1-5: USB DOWNSTREAM (HOST CONTROLLER) VBUS CONTROL PIN DESCRIPTION 18
TABLE 1-6: I2C PIN DESCRIPTION 18
TABLE 1-7: UART 0 & BUZZER PIN DESCRIPTION 19
TABLE 1-8: GPIO PIN DESCRIPTION 19
TABLE 1-9: INTERRUPT PIN DESCRIPTION 19
TABLE 1-10: TIMERS PIN DESCRIPTION 20
TABLE 1-11: CPU DEBUGGER PIN DESCRIPTION 20
TABLE 1-12: HIGH SPEED UART 1 PIN DESCRIPTION 20
TABLE 1-13: HIGH SPEED SPI PIN DESCRIPTION 21
TABLE 1-14: PS2 PIN DESCRIPTION 22
TABLE 1-15: POWER, GROUND PIN DESCRIPTION 22
TABLE 2-1: THREE POWER MANAGEMENT OPERATION MODES OF AX6800X 27
TABLE 3-1: HARDWARE CONFIGURATION FLASH INFORMATION MEMORY MAP 30
TABLE 3-2: THE CPU SFR REGISTER MAP 38
TABLE 4-1: I2C MASTER CONTROLLER TIMING TABLE 48
TABLE 4-2: I2C SLAVE CONTROLLER TIMING TABLE 48

1.0 Introduction

1.1 General Description

AX6800x, Single Chip Micro-controller with USB Host and Multiple Addressed Device Controller, is a System-on-Chip (SoC) solution which offers high performance CPU architecture with on-chip 128KB Flash memory as Program Memory, on-chip 32KB Data Memory for CPU, built in one USB host controller and one USB root hub that supports four downstream ports compliant with USB2.0 Full/Low Speed Standard, 4 Device Controllers compliant with USB2.0 Full Speed Standard, and rich peripheral interfaces for wide varieties of application which need bridge to the USB interface.

The CPU architecture of AX6800x utilizes the USB protocols maintenance for those upstream and downstream ports to the external USB Host and Device and performs packet translation between upstream and downstream ports. The Root Hub provided all the transactions scheduling and management with CPU to maintain to the all adapted USB devices. The Host and Device controller with DMA engine provide the data transmission between the USB bus from/to on-chip 32KB SRAM.

In addition to stand-alone application, AX6800x with USB protocol suite running on-chip and various serial host interfaces supported, High Speed UART or High Speed SPI, can be used as a data bridge from/to USB interface in an embedded system.

A 12 MHz crystal is needed for internal 96 MHz PLL to provide the 48 and 12 MHz for USB related and the typical operating frequency of AX6800x is 48 or 96MHz. AX6800x also integrates power-on reset circuit on-chip that can simplify external reset circuit on PCB and prevent the program code corrupt in Flash memory.

AX6800x is available in 100-pin LQFP or 64-pin QFN RoHS compliant package and the recommended operating temperature range is 0 to 70℃.

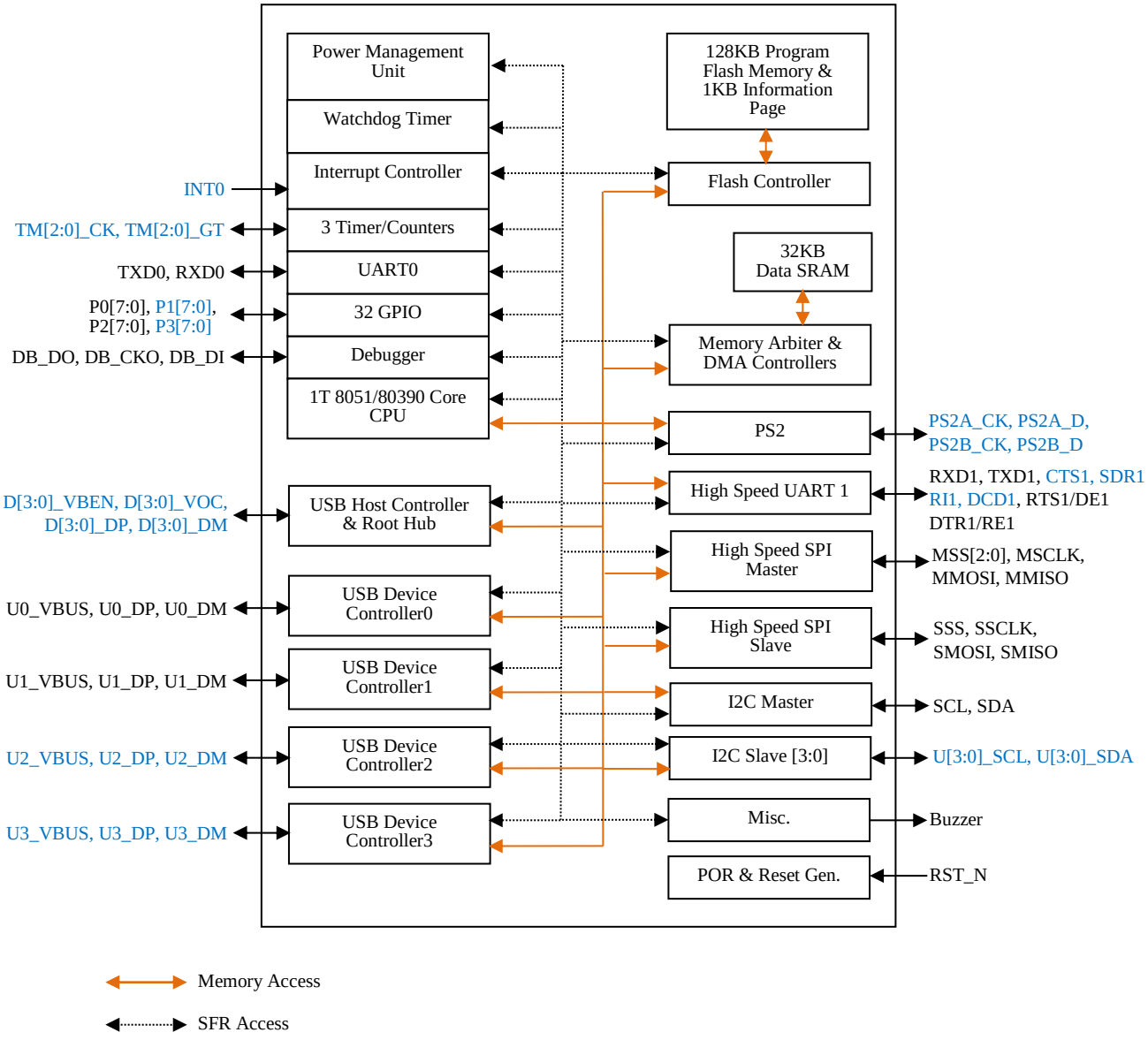
AX6800x provides cost effective solution to enable simple, easy, and low cost integration capability for KVM applications. It could also provide highly programmable flexibility and compatibility.

1.2 Product Selection Guide

Below table shows the major differences among the 2 available part numbers.

Part Number	Flash Program Memory (bytes)	CPU SRAM Data Memory (bytes)	USB Host/Device Ports	GPIO	Package	Operating Temperature
AX68002 QF	128K	32K	2+2	16	64-pin QFN	0 to 70°C
AX68004 LF	128K	32K	4+4	32	100-pin LQFP	0 to 70°C

1.3 AX6800x Block Diagram



Note: U[3:2]_SCL, U[3:2]_SDA, TM[2:0]_CK, TM[2:0]_GT, INT0, PS2A_CK, PS2A_D, PS2B_CK, PS2B_D, CTS1, SDR1 RI1, DCD1, P1[7:0], P3[7:0], U2_VBUS, U2_DP, U2_DM, D[3:2]_VBEN, D[3:2]_VOC, D[3:2]_DP, D[3:2]_DM are for AX68004 only.

Figure 1-1: AX6800x Block Diagram

1.4 AX6800x Pinout Diagram

AX68002 is housed in a 64-pin QFN package.

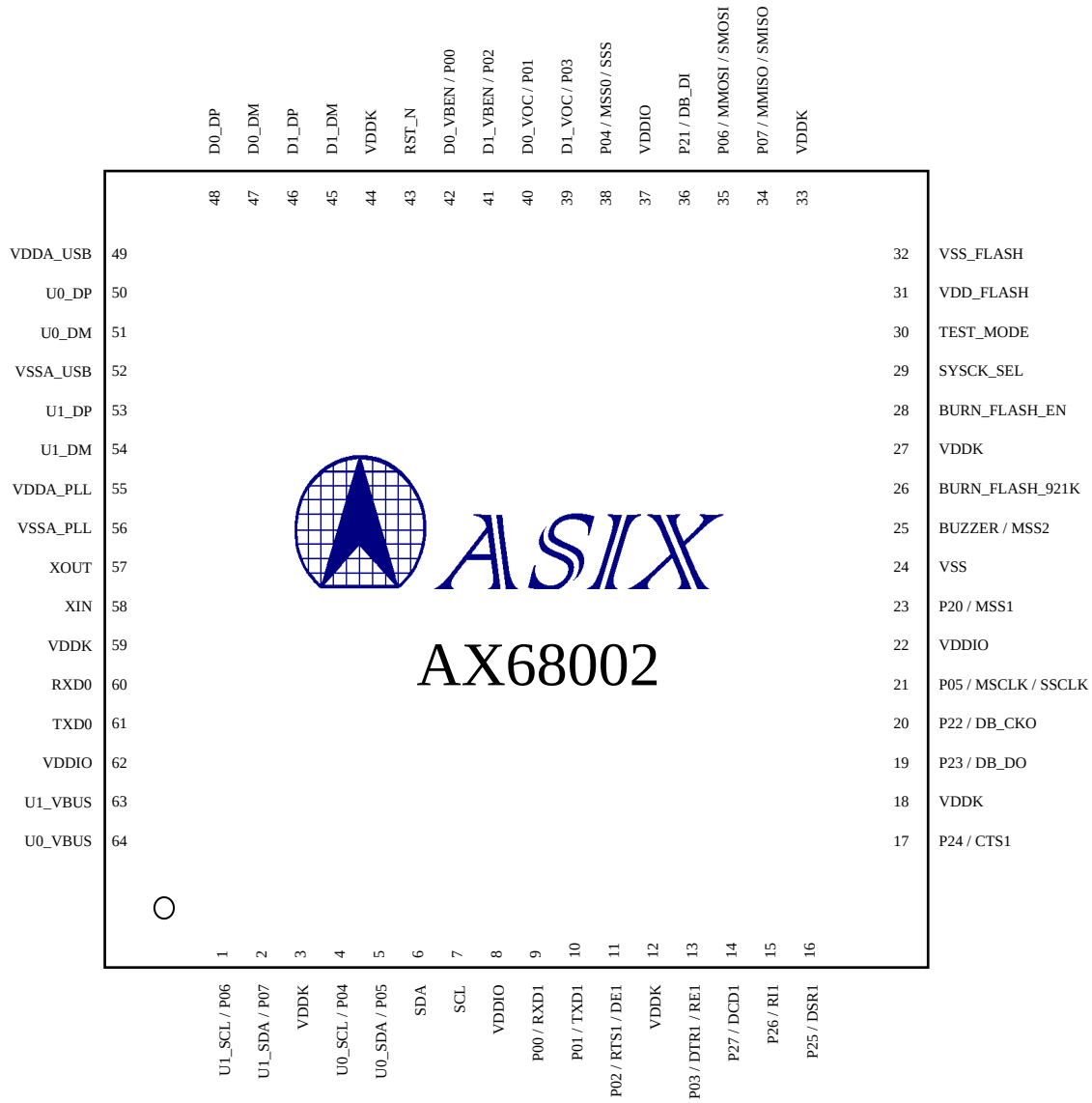


Figure 1-2: AX68002 Pinout Diagram

AX68004 is housed in a 100-pin LQFP package.

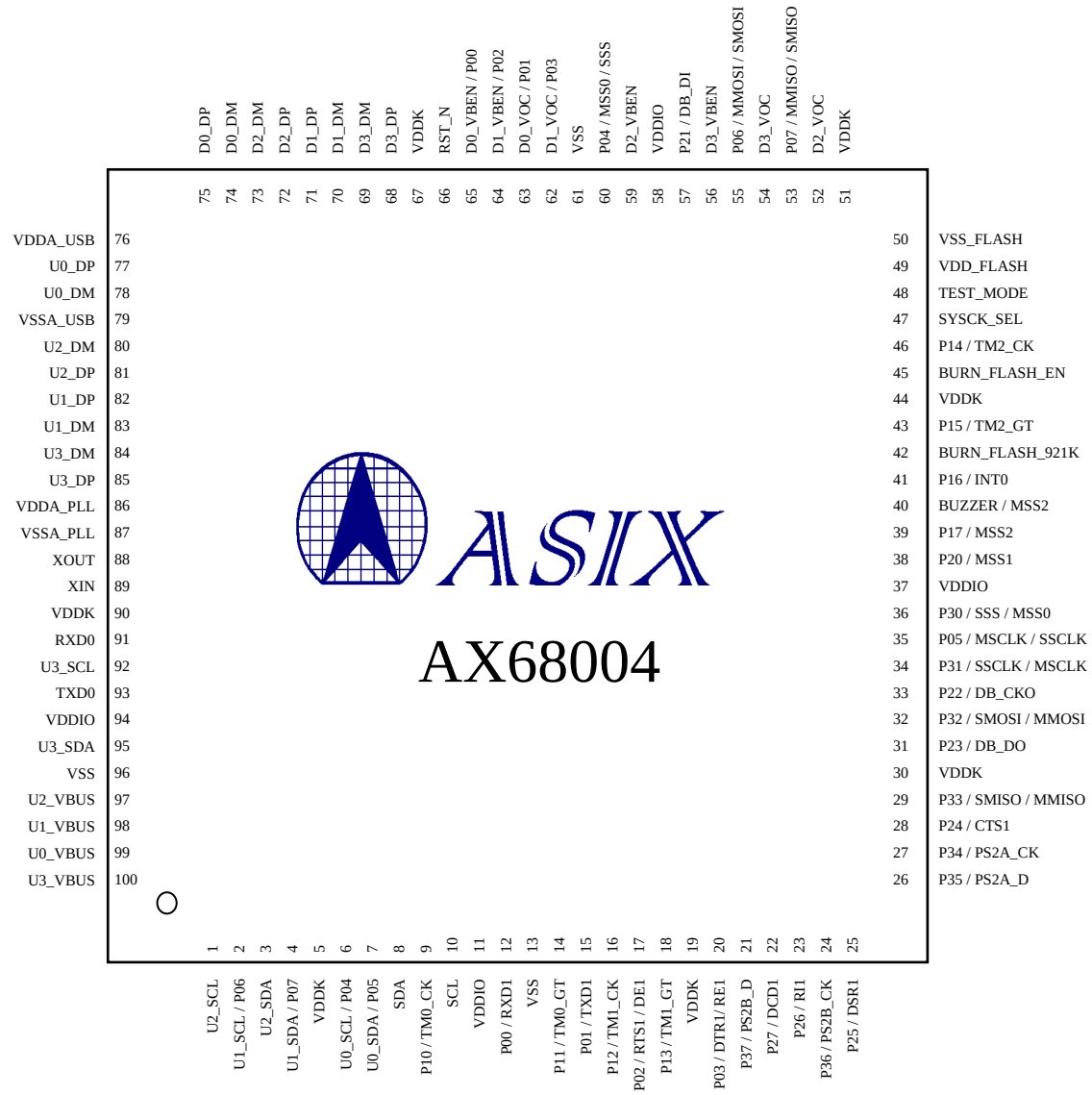


Figure 1-3: AX68004 Pinout Diagram

1.5 Signal Description

Following abbreviations are used in "Type" column of following pin description tables. Note that some I/O pins with multiple signal definitions on the same pin may have different attribute in "Type" column for different signal definition.

AB	Analog Bi-directional I/O	**O5**	Output, 3.3V with 5V tolerant
AI	Analog Input	**PU**	Internal Pull-Up (75K)
AO	Analog Output	**PD**	Internal Pull-Down (75K)
B3	Bi-directional I/O, 3.3V	**P**	Power and ground pin
B5	Bi-directional I/O, 3.3V with 5V tolerant	**S**	Schmitt Trigger
I3	Input, 3.3V	**T**	Tri-state
I5	Input, 3.3V with 5V tolerant	**4m**	4mA driving strength
O3	Output, 3.3V	**8m**	8mA driving strength

For example, pin 12 in AX68004 package can be P00 or RXD0. If P00 is selected, its Type is B5/4m/PU; if RXD1 is selected, its Type is I5. In other words, the PU (internal pull-up) only takes effect in P00 signal mode while RXD1 signal mode doesn't. User should refer to the table specific to desired function for exact pin type definition.

The multi-function pin settings are configured by Hardware Configuration (**HWCFG**) in Flash Information Page Memory. The following abbreviations are used in pin description tables.

Table 1-1: Chip Clock and Reset Pin Description

Chip Clock and Reset				
Pin Name	**Type**	**Pin No**		**Pin Description**
		64	**100**	
XIN	AI	58	89	12MHz crystal input or oscillator clock input. This clock is always required for the USB functions and, in most cases, used as clock reference to the internal 96MHz PLL which generates 96MHz as main operating system clock. The recommended reference frequency is 12MHz +/-50ppm, 45 ~ 55% clock duty cycle. Note that this input pin is 3.3V tolerant.
XOUT	AB	57	88	12MHz crystal output.
RST_N	I5/PU/S	43	66	Chip Reset input, active low. RST_N is the hardware reset input used to reset this chip. This input is AND with internal Power-On-Reset (POR) circuit, which generates the main system reset for this chip.
SYSCK_SEL	I5/PU	29	47	Operating SYStem ClocK frequency SELection input: 0: Select 48MHz operating system clock, please tie to logic low. 1: Select 96MHz operating system clock, please tie to logic high or NC.
TEST_MODE	I5/PD	30	48	Test Mode enable. For normal operation, please always tie to logic low or NC.
VDDA_PLL	P	55	86	Analog Power for internal 96MHz PLL, 1.8V.
VSSA_PLL	P	56	87	Analog Ground for internal 96MHz PLL.

Table 1-2: Chip Configuration Pin Description

Chip Configuration Pins				
Pin Name	Type	Pin No		Pin Description
		64	100	
BURN_FLASH_EN	I5/PD	28	45	Please NC or pull down with 10Kohm to allow the CPU to proceed with normal boot after power-on reset and to disable In-System-Programming (ISP) mode via UART 0. Please pull up with 4.7Kohm to temporarily enable ISP mode for initial Flash memory programming via UART 0. This puts the CPU in reset state during the ISP mode.
BURN_FLASH_921K	I5/PU	26	42	When ISP mode is enabled (BURN_FLASH_EN = pull-up), please NC or pull up with 10Kohm to enable higher speed of 921.6Kbps baud rate at UART 0. Please pull down with 4.7Kohm to enable normal speed of 115.2Kbps baud rate at UART 0 during ISP mode. When the ISP mode is disabled (BURN_FLASH_EN = pull-down), this pin has no effect.

Table 1-3: USB Transceiver Pin Description

USB Transceiver Pins				
Pin Name	Type	Pin No		Pin Description
		64	100	
U0_DP	AB	50	77	Upstream USB Port 0 D+.
U0_DM	AB	51	78	Upstream USB Port 0 D-.
U1_DP	AB	53	82	Upstream USB Port 1 D+.
U1_DM	AB	54	83	Upstream USB Port 1 D-.
U2_DP	AB	-	81	Upstream USB Port 2 D+.
U2_DM	AB	-	80	Upstream USB Port 2 D-.
U3_DP	AB	-	85	Upstream USB Port 3 D+.
U3_DM	AB	-	84	Upstream USB Port 3 D-.
D0_DP	AB	48	75	Downstream USB Port0 D+.
D0_DM	AB	47	74	Downstream USB Port0 D-.
D1_DP	AB	46	71	Downstream USB Port1 D+.
D1_DM	AB	45	70	Downstream USB Port1 D-.
D2_DP	AB	-	72	Downstream USB Port2 D+.
D2_DM	AB	-	73	Downstream USB Port2 D-.
D3_DP	AB	-	68	Downstream USB Port3 D+.
D3_DM	AB	-	69	Downstream USB Port3 D-.
VDDA_USB	P	49	76	Power for USB Transceivers, 3.3V.
VSSA_USB	P	52	79	Ground for USB Transceivers.

Table 1-4: USB Upstream (Device Controller) VBUS Pin Description

USB Upstream VBUS Pins				
Pin Name	Type	Pin No		Pin Description
		64	100	
U0_VBUS	I5, PD	64	99	Upstream Port 0 VBUS. Used to detect the VBUS status for Upstream Port 0
U1_VBUS	I5, PD	63	98	Upstream Port 1 VBUS. Used to detect the VBUS status for Upstream Port 1
U2_VBUS	I5, PD	-	97	Upstream Port 2 VBUS. Used to detect the VBUS status for Upstream Port 2
U3_VBUS	I5, PD	-	100	Upstream Port 3 VBUS. Used to detect the VBUS status for Upstream Port 3

Table 1-5: USB Downstream (Host Controller) VBUS Control Pin Description

USB Downstream VBUS control Pins				
Pin Name	Type	Pin No		Pin Description
		64	100	
D0_VBEN	O5	42	65	Downstream Port 0 VBUS Enable [(1)].
D0_VOC	I5,PU	40	63	Downstream Port 0 VBUS Over Current detection [(1)].
D1_VBEN	O5	41	64	Downstream Port 1 VBUS Enable [(2)].
D1_VOC	I5,PU	39	62	Downstream Port 1 VBUS Over Current detection [(2)].
D2_VBEN	O5	-	59	Downstream Port 2 VBUS Enable.
D2_VOC	I5,PU	-	52	Downstream Port 2 VBUS Over Current detection.
D3_VBEN	O5	-	56	Downstream Port 3 VBUS Enable.
D3_VOC	I5,PU	-	54	Downstream Port 3 VBUS Over Current detection.

Note 1: To enable these multi-function pins, please set USB_D0_PSEL = 0 in HWCFG offset 0x003 or USB_D0_PSEL = 1 but MP0_10_PSEL = 0 in HWCFG offset 0x001.

Note 2: To enable these multi-function pins, please set USB_D1_PSEL = 0 in HWCFG offset 0x003 or USB_D1_PSEL = 1 but MP0_32_PSEL = 0 in HWCFG offset 0x001.

Table 1-6: I2C Pin Description

I2C Interface				
Pin Name	Type	Pin No		Pin Description
		64	100	
SCL	O5/T/4m	7	10	I2C Serial Clock line for I2C master controller. SCL is a tri-stateable output, which requires an external pull-up resistor.
SDA	B5/T/4m	6	8	I2C Serial Data line for I2C master controller. SDA is a tri-stateable output, which require an external pull-up resistor.
U0_SCL	I5/4m	4	6	I2C Upstream (slave) controller 0 Serial Clock line [(3)]. U0_SCL requires an external pull-up resistor.
U0_SDA	B5/T/4m	5	7	I2C Upstream (slave) controller 0 Serial Data line [(3)]. U0_SDA is a tri-stateable output, which requires an external pull-up resistor.
U1_SCL	I5/4m	1	2	I2C Upstream (slave) controller 1 Serial Clock line [(4)]. U1_SCL requires an external pull-up resistor.
U1_SDA	B5/T/4m	2	4	I2C Upstream (slave) controller 1 Serial Data line [(4)]. U1_SDA is a tri-stateable output, which requires an external pull-up resistor.
U2_SCL	I5/4m	-	1	I2C Upstream (slave) controller 2 Serial Clock line. U2_SCL requires an external pull-up resistor.
U2_SDA	B5/T/4m	-	3	I2C Upstream (slave) controller 2 Serial Data line. U2_SDA is a tri-stateable output, which requires an external pull-up resistor.
U3_SCL	I5/4m	-	92	I2C Upstream (slave) controller 3 Serial Clock line. U3_SCL requires an external pull-up resistor.
U3_SDA	B5/T/4m	-	95	I2C Upstream (slave) controller 3 Serial Data line. U3_SDA is a tri-stateable output, which requires an external pull-up resistor.

Note 3: To enable these multi-function pins, please set I2C_U0_PSEL = 0 in HWCFG offset 0x002 or I2C_U0_PSEL = 1 but MP0_74_PSEL = 0 in HWCFG offset 0x001.

Note 4: To enable these multi-function pins, please set I2C_U1_PSEL = 0 in HWCFG offset 0x002 or I2C_U1_PSEL = 1 but MP0_74_PSEL = 0 in HWCFG offset 0x001.

Table 1-7: UART 0 & Buzzer Pin Description

UART 0 Interface				
Pin Name	Type	Pin No		Pin Description
		64	100	
RXD0	B5/4m/PU	60	91	UART 0 serial Receive Data.
TXD0	O5/4m	61	93	UART 0 serial Transmit Data.
BUZZER	O5/4m	25	40	Buzzer [5].

Note 5: To enable these multi-function pins, please set BUZZER_PSEL = 0 in HWCFG offset 0x003 or BUZZER_PSEL = 1 but MP1_7_PSEL = 1 in HWCFG offset 0x001.

Table 1-8: GPIO Pin Description

GPIO Interface				
Pin Name	Type	Pin No		Pin Description
		64	100	
P0[7:0]	B5/4m/PU	34, 35, 21, 38, 13, 11, 10, 9 (2, 1, 5, 4, 39, 41, 40, 42)	53, 55, 35, 60, 20, 17, 15, 12 (4, 2, 7, 6, 62, 64, 63, 65)	General Purpose Input/ Output Pins Port 0 [6]. To enable these multi-function pins, please set MP0_10/32/74_PSEL = 0 in HWCFG offset 0x001. P0 has two pinout options and the parenthesis indicates the 2nd option, enabled by setting MP0_10/32/74_PSEL = 1, USB_D0/D1_PSEL = 1 and, I2C_U0/U1_PSEL = 1.
P1[7:0]	B5/4m/PU	-	39, 41, 43, 46, 18, 16, 14, 9	General Purpose Input/ Output Pins Port 1 [6]. To enable these multi-function pins, please set MP1_10/32/54/6/7_PSEL = 0 in HWCFG offset 0x001.
P2[7:0]	B5/4m/PU	14, 15, 16, 17, 19, 20, 36, 23	22, 23, 25, 28, 31, 33, 57, 38	General Purpose Input/ Output Pins Port 2 [6]. To enable these multi-function pins, please set MP2_0/31/54/76_PSEL = 0 in HWCFG offset 0x002.
P3[7:0]	B5/4m/PU	-	21, 24, 26, 27, 29, 32, 34, 36	General Purpose Input/ Output Pins Port 3 [6]. To enable these multi-function pins, please set MP3_30/74_PSEL = 0 in HWCFGS offset 0x002.

Note 6: Due to internal weak pull-up, user may add stronger external pull-up resistors for these GPIO pins, if necessary.

Table 1-9: Interrupt Pin Description

Interrupt Interface				
Pin Name	Type	Pin No		Pin Description
		64	100	
INT0	I5/PU	-	41	CPU INTerrupt 0 inputs, active low or falling edge trigger [7].

Note 7: To enable these multi-function pins, please set MP1_6_PSEL = 1 in HWCFG offset 0x001.

Table 1-10: Timers Pin Description

Timers Interface				
Pin Name	Type	Pin No		Pin Description
		64	100	
TM[2:0]_CK	I5	-	46, 16, 9	TiMer 2, 1, 0 external Clock input [8].
TM[2:0]_GT	I5	-	43, 18, 14	TiMer 2, 1, 0 external GaTe control input [8].

Note 8: To enable these multi-function pins, please set MP1_10/32/54_PSEL = 1 in HWCFG offset 0x001.

Table 1-11: CPU Debugger Pin Description

CPU Debugger Interface				
Pin Name	Type	Pin No		Pin Description
		64	100	
DB_DI	I5/PU	36	57	CPU DeBugger Data Input [9].
DB_CKO	O5/4m	20	33	CPU DeBugger Clock Output [9].
DB_DO	O5/4m	19	31	CPU DeBugger Data Output [9].

Note 9: To enable these multi-function pins, please set MP2_31_PSEL = 1 in HWCFG offset 0x002.

Table 1-12: High Speed UART 1 Pin Description

High Speed UART 1 Interface				
Pin Name	Type	Pin No		Pin Description
		64	100	
RXD1	I5	9	12	UART 1 serial Receive Data [10].
TXD1	O5/4m	10	15	UART 1 serial Transmit Data [10].
CTS1	I5	17	28	UART 1 Clear To Send [11].
DSR1	I5	16	25	UART 1 Data Set Ready [11].
RI1	I5	15	23	UART 1 Ring Indicator [11].
DCD1	I5	14	22	UART 1 Data Carrier Detect [11].
RTS1/DE1	O5/4m	11	17	UART 1 Request To Send/ Driver output Enable [12] [13].
DTR1/RE1	O5/4m	13	20	UART 1 Data Terminal Ready/Receiver output Enable [12] [13].

Note 10: To enable these multi-function pins, please set MP0_10_PSEL = 1 in HWCFG offset 0x001.
Note 11: To enable these multi-function pins, please set MP2_54/76_PSEL = 1 in HWCFG offset 0x002.
Note 12: To enable these multi-function pins, please set MP0_32_PSEL = 1 in HWCFG offset 0x001.
Note 13: To decide use RTS1/DTR1 or DE1/RE1_n please refer high speed UART register description as below section.

Table 1-13: High Speed SPI Pin Description

High Speed SPI Interface				
Pin Name	Type	Pin No		Pin Description
		64	100	
MSS0	O5/T/4m	38	60 (36)	SPI Master controller Slave Select 0 (14). MSS0 is a tri-stateable output, which requires an external pull-up resistor.
MSS1	O5/T/4m	23	38	SPI Master controller Slave Select 1 (15). MSS1 is a tri-stateable output, which requires an external pull-up resistor.
MSS2	O5/T/4m	- (25)	39 (40)	SPI Master controller Slave Select 2 (16). MSS2 is a tri-stateable output, which requires an external pull-up resistor.
MSCLK	O5/T/4m	21	35 (34)	SPI Master controller CLocK (14). MSCLK is a tri-stateable output. At Mode 0 or 2, SCLK requires external pull-down resistor; while at Mode 1 or 3, SCLK requires external pull-up resistor.
MMISO	I5	34	53 (29)	SPI Master controller Master Input Slave Output line (14). MMISO is used to receive serial data.
MMOSI	O5/T/4m	35	55 (32)	SPI Master controller Master Output Slave Input line (14). MMOSI is used to transmit serial data and is a tri-stateable output.
SSS	I5	- (38)	36 (60)	SPI Slave controller Slave Select (17). SSS is an active low input
SSCLK	I5	- (21)	34 (35)	SPI Slave controller CLocK (17).
SMISO	O5/T/4m	- (34)	29 (53)	SPI Slave controller Master Input Slave Output line (17). SMISO is used to transmit serial data and is a tri-stateable output.
SMOSI	I5	- (35)	32 (55)	SPI Slave controller Master Output Slave Input line (17). SMOSI is used to receive serial data.

Note 14: To enable these multi-function pins, please set MP0_74_PSEL = 1 in HWCFG offset 0x001 and SPI_SW_PSEL = 0 in HWCFG offset 0x003.In AX68004 package, MSS0/MSCLK/MMISO/MMOSI have two pinouts options, and the parenthesis indicates the 2nd option, enabled by setting MP3_30_PSEL = 1 in HWCFG offset 0x003 and SPI_SW_PSEL = 1.

Note 15: To enable these multi-function pins, please set MP2_0_PSEL = 1 in HWCFG offset 0x002.

Note 16: To enable these multi-function pins, please set MP1_7_PSEL = 1 in HWCFG offset 0x001. MSS2 have two pinouts options, and the parenthesis indicates the 2nd option, enabled by setting BUZZER_PSEL = 1 in HWCFG offset 0x003.

Note 17: To enable these multi-function pins, please set MP3_30_PSEL = 1 and SPI_SW_PSEL = 0. In AX68004 package, SSS/SSCLK/SMISO/SMOSI has two pinouts options, and the parenthesis indicates the 2nd option, enabled by setting MP0_74_PSEL = 1 and SPI_SW_PSEL = 1.

Table 1-14: PS2 Pin Description

PS2 Interface				
Pin Name	Type	Pin No		Pin Description
		64	100	
PS2A_CK	B5/T/4m	-	27	PS2 controller A ClocK line [18]. PS2A_CK is a tri-stateable output, which requires an external pull-up resistor.
PS2A_D	B5/T/4m	-	26	PS2 controller A Data line [18]. PS2A_D is a tri-stateable output, which requires an external pull-up resistor.
PS2B_CK	B5/T/4m	-	24	PS2 controller B ClocK line [18]. PS2B_CK is a tri-stateable output, which requires an external pull-up resistor.
PS2B_D	B5/T/4m	-	21	PS2 controller B Data line [18]. PS2B_D is a tri-stateable output, which requires an external pull-up resistor.

Note 18: To enable these multi-function pins, please set MP3_74_PSEL = 1 in HWCFG offset 0x002.

Table 1-15: Power, Ground Pin Description

Power, Ground				
Pin Name	Type	Pin No		Pin Description
		64	100	
VDDIO	P	8, 22, 37, 62	11, 37, 58, 94	Digital Power for I/O pins, 3.3V. Please add a 0.1uF bypass capacitor between each VCCIO and GND.
VDDK	P	3, 12, 18, 27, 33, 44, 59	5, 19, 30, 44, 51, 67, 90	Digital Power for core, 1.8V. Please add a 0.1uF bypass capacitor between each VCCK and GND.
VSS	P	24	13, 61, 96	Digital Ground for core and I/O pins.
VDD_FLASH	P	31	49	Power for flash memory pin, 1.8V.
VSS_FLASH	P	32	50	Ground for flash memory pin.

2.0 Function Description

2.1 Clock Generation

AX6800x requires an external 12MHz crystal as the main clock source. The clock source provides the reference timing to the internal 96MHz PLL (Phase-Locked Loop) block to generate 96MHz clock. The 96MHz clock can be divided to 48 and 12MHz clock. The SYSCK_SEL input is used to select the operating system clock frequency between 48MHz and 96MHz. The 12MHz and 48MHz can be used as the clock source for the USB process to handle the data transmission and some USB protocol scheme. The recommended reference frequency of external 12MHz Crystal is 12MHz +/-50ppm, 45 ~ 55% clock duty cycle.

2.2 Reset Generation

During the VDDIO power-on, the internal Power-On-Reset (POR) can generate a reset pulse to reset all the function blocks, including Flash memory, CPU Core and all the peripherals, when the VDDIO power pin rises to certain threshold voltage level. The RST_N input is “AND” operating with the POR output so the manual reset event can be applied by external system circuitry.

NOTICE: Due to AX6800x needs to be supplied dual powers for all IO and core powers and the POR is designed to detect the VDDIO power only. It is important to make sure the VDDK stabled before VDDIO ramp up or down cross the V_{rr} and V_{fr} voltages. Suggested the VDDIO and VDDK are from same power source and use LDO regulator for 1.8V power source (Drop Out voltage ≤ 0.3 V) on the board level design. Please reference Section 4.3 and 4.4 for the detail.

2.3 CPU Core and Debugger

2.3.1 CPU Core

The 1T 8051/80390 CPU core of AX6800x is an ultra-high performance, speed optimized, 8-bit embedded controller dedicated for operation with fast on-chip memories. The CPU core has been designed with a special concern about performance to power consumption ratio. The CPU core is 100% binary-compatible with the industry standard 8051 8-bit micro-controller. The CPU core can address up to 128K bytes of linear program space. The CPU core has Pipelined RISC architecture, which can be 10 times faster compared to standard architecture and executes 96 million instructions per second when operating in 96Mhz.

The main features of 1T 8051/80390 CPU core are listed below:

- 100% software compatible with industry standard 8051
- Maximum operating clock frequency of 96M Hz
- Pipelined RISC architecture enables to execute instructions 10 times faster compared to standard 8051
  - 20-bit FLAT program addressing mode – 80C390 instructions set
  - 16-bit LARGE program addressing mode – 80C51 instructions set
- 24 times faster multiplication
- 12 times faster addition
- 256 bytes of internal (on-chip) Data Memory
- Up to 128K bytes of Program Memory
  - On-chip SRAM used for mirrored program: 0 to 8K bytes
  - On-chip Flash memory used for program: 0 to 128K bytes in FLAT mode
- Up to 32K bytes of External Data Memory(xDATA)
- User programmable Program Memory wait states

2.3.2 Debugger

The Debugger inside AX6800x provides an in-circuit emulator feature and it is used to connect to an external In-Circuit-Emulation (ICE) adaptor board, which manages communication between the Debugger inside AX6800x and the Debug Software on a PC. The Hardware Assisted Debugger (HAD2) is the ICE adaptor board that manages communication between the Debugger inside AX6800x and an USB port of the host PC running Debug Software.

The Debug Software is a Windows based application. It is fully compatible with all existing 8051/80390 C compilers and Assemblers. The Debug Software allows user to work in two major modes: software simulator mode and hardware debugger mode. Those two modes assure software validation in simulation mode and then real-time debugging of developed software inside AX6800x using debugger mode. Once loaded, the program may be observed in Source Window, run at full-speed, single stepped by machine or C level instructions, or stopped at any of the breakpoints.

2.4 Flash Controller and On-Chip Flash Memory

2.4.1 Program Loader

The Program Loader activates right after chip reset or software reboot command and performs copying CPU program code from on-chip Flash memory to on-chip 8K bytes Program SRAM for "Program Code Mirroring".

2.4.2 Flash Controller and In-Application Programming

Flash Controller supports Flash memory access related Word Read, Word Write, Sector Erase, Chip Erase command signal generation needed for CPU's special SFR access and software DMA's write access. Along with Software DMA controller, it supports various DMA transfer direction such as Flash memory to External Data Memory (P2D), External Data Memory (xDATA) to Flash memory (D2P), Flash memory to Flash memory (P2P), etc. for so-called In-Application Programming (IAP) function during run-time. For each Word Write access, Flash Controller will perform the read back check automatically. If the read back check encountered the mismatch happened, the Flash Controller will interrupt CPU to inform the current Word Write access is incorrect.

2.4.3 In-System Programming

ISP Controller supports In-System Programming (ISP) function through either UART 0 interface to program on-chip Flash memory.

Upon enabled (via BURN_FLASH_EN pin), ISP controller allows on-chip Flash memory to be programmed by ASIX's Flash Programming utility software on a PC with a standard RS-232 port. The link speed (baud rate) of UART 0 used for communicating to the PC's RS-232 port can be selectable between 921.6K or 115.2K bps (via BURN_FLASH_921K pin). When developing AX6800x software or manufacturing AX6800x based systems, ASIX's Flash Programming utility can provide easy and fast Flash memory programming capability.

2.4.4 On-Chip Flash Memory

The main features of the on-chip Flash memory are listed below,

- Requires only 1.8V power for read, erase and write operations
- Fast Read, Write and Erase
  - Read access time: 40ns
  - Write (programming) access time: 20us (typical)
  - Page erase time: 2ms
  - Mass Erase time: 10ms
- Minimum 100,000 erase/program cycles
- Minimum 10 years data retention under maximum 20 times pre-cycles
- Program code download protection in hardware to prevent unauthorized program code download.

2.5 Memory Controller and On-Chip Data Memory

AX6800x supports xDATA memory of CPU up to 32K bytes.

The Memory Arbiter – provides fair access arbitration for xDATA memory (on-chip 32KB Data SRAM) among CPU and the DMA Controllers.

2.6 DMA Controller

The DMA Controllers support direct xDATA memory (on-chip 32KB Data SRAM) read and write access without CPU intervention for the USB Host Controller, USB Device Controller, High Speed SPI, I2C, High Speed UART 1, as well as bulk data copy for Software DMA.

2.7 Interrupt Controller

The Interrupt Controller supports one external interrupt pin, INT0, having two levels of interrupt priority control. They can be in high or low-level priority group (set via IP and EIP SFR register). The INT0 external interrupt pins can be either low-level trigger or falling-edge trigger. Also, the Interrupt Controller supports various interrupt requests internal to AX6800x, again each having two levels of interrupt priority control.

2.8 Watchdog Timer

The Watchdog Timer is a user programmable clock counter that can serve as:

- A time-base generator
- An event timer
- System supervisor

The watchdog timer runs on the operating system clock, which supplies to a series of dividers. The divider output is selectable, and determines interval between timeouts.

When the timeout is reached, an interrupt flag will be set, and if enabled, a reset will occur (to reset CPU core). The interrupt flag will cause an interrupt to occur if enabled. The reset and interrupt are discrete functions that may be acknowledged or ignored, together or separately for various applications.

2.9 Power Management Unit

Table 2-1 below lists the 3 possible modes of operation of AX6800x, namely Full Speed mode, STOP mode, Deep Sleep mode. For typical power consumption of AX6800x in these operation modes, please refer to Section 4.2.

Operation Mode	Description
Full Speed	The operating system clock of CPU and peripherals is running at full clock rate (i.e., 48 or 96 MHz, depending on SYSCK_SEL setting).
STOP	The STOP mode is when CPU is in complete stop mode, the operating system clock of CPU and peripherals is turned off, but the 12MHz crystal oscillation and 96MHz PLL clock still run.
Deep Sleep	The Deep Sleep mode is when CPU is in complete stop mode, the operating system clock of CPU and peripherals is turned off, and the 12MHz crystal oscillation and 96MHz PLL clock are turned off too.

Table 2-1: Three Power Management Operation Modes of AX6800x

2.10 Timers and Counters

The CPU of AX6800x provides three 16-bit timer/counters, namely, Timer 0, Timer 1, and a fully compatible with the standard 8052 Timer 2, and one dedicated Millisecond Timer, which is programmable with 1ms resolution for software use.

In the “timer mode”, timer registers are incremented in every 12 or 4 operating system clock periods when appropriate timer is enabled. In the “counter mode”, the timer registers are incremented at every falling transition on their corresponding input pins: TM0_CK, TM1_CK or TM2_CK. The input pins are sampled at every operating system clock period.

2.11 UARTs

AX6800x supports 2 UART interfaces, namely, UART 0 and High Speed UART 1. The UART 0 has the same functionality as standard 8051 UARTs and both support full duplex and receive double-buffered, meaning it can commence reception of a second byte before a previously received byte has been read from the receive register.

The High Speed UART 1 of AX6800x is compatible with standard 16550 device architecture that provides serial communication capabilities to communicate with Modem or other external device (e.g. computer) using RS-232 or RS-485 protocols. The High Speed UART 1 supports transfer baud rate up to 921.6 Kbps, provides 16-byte Transmitter and Receiver FIFO for data buffering, supports DMA mode burst transfer for data receive and transmit process, and supports Auto-hardware flow control (Auto-RTS and Auto-CTS) and Auto-software flow control (Auto-send and Auto-detect Xon and Xoff characters) to reduce CPU/software loading.

2.12 GPIOs

The CPU of AX6800x supports four 8-bit bi-directional, open-drain, general purpose input and output ports, namely, P0[7:0], P1[7:0], P2[7:0] and P3[7:0]. Each port bit can be individually accessed by bit addressable instructions.

For the special application, like push button, P0 and P2 support de-bounce and interrupt function which can be programmed to detect the rising, falling edge and both interrupt event. Each bit in these two ports support the wake-up function also. It can wake-up CPU from STOP or deep sleep mode. The function can be enabled or disabled separately per bit.

2.13 Buzzer Controller

The Buzzer Controller of AX6800x supports 8 kinds of frequency and 5 duration times can be selected. CPU can start the buzzer sound and will be interrupted when the duration is time up.

2.14 I2C Controller

The I2C Controller of AX6800x consists of an I2C master controller to support communication to external I2C devices (Monitor), 2/4 I2C slave controllers to support communication to external Host with I2C master (PC).

I2C master controller supports the auto-detection function to detect the external monitor has been plugged/un-plugged and the auto-load function to load the EDID contents from external monitor to internal 32KB SRAM automatically.

Each I2C slave controller also supports the DMA function to read EDID information from 32KB SRAM to external Host automatically.

2.15 High Speed SPI Controller

The High Speed Serial Peripheral Interface (SPI) Controller provides a full-duplex, synchronous serial communication interface (4 wires) to flexibly work with numerous SPI peripheral devices or microcontroller with SPI master. The High Speed SPI Controller consists of a High Speed SPI master controller with 3 slave select pins, MSS[2:0], to connect up to 7 SPI devices and a High Speed SPI slave controller to support communication with external microcontroller with SPI master.

For high performance applications, the High Speed SPI Controller in master and slave mode both support burst-type transfer for receiving data from SPI bus to CPU xDATA memory via DMA write access (SPI RX DMA) and for transmitting data from xDATA memory to SPI bus via DMA read access (SPI TX DMA).

2.16 PS/2 Controller

The PS/2 Controller provides two independent PS/2 serial interfaces to the bidirectional protocol that can handle data transmission between the host (PC) and the PS/2 device (Keyboard or Mouse). It also supports error detection (for parity and stop bit) on all data received from PS/2 device and the timer control to timeout the device which failed to respond and clock period.

2.17 USB Root Hub and Host Controller

The USB Host Controller built-in one root hub and provide 2/4 downstream ports to communication with numerous USB full/low speed devices and compliant USB2.0 Full/Low speed standard, supporting data transfer at full speed (12Mbit/s) and low speed (1.5 Mbit/s).

The USB Host Controller supports UHCI data transfer type schedule order to transfer Isochronous, Interrupt, Control and Bulk data type, each packet type can be enabled or disabled by software commands. It also supports one memory buffer to store receive or transfer data, and the memory buffer be divided to 3 memory area, namely, ISTL, INTL and ATL, for four USB transfer type as above mention, each memory area also be divided to more little buffer and it calls Transfer Descriptor (TD) structure. The total memory size is limited up to 4K bytes by Host Control (HC) in 32KB Data SRAM.

The USB Host Controller supports 8 TDs for ISTL, 32 TDs for INTL and ATL in once transfer, the ISTL transfer is also support automatic to synchronization one in advance assignment SOF interval per software assign, each INTL TD also supports automatic interrupt polling rate to reduce CPU/software loading, the ATL supports two different block size for control and bulk transfer enhancement memory used.

2.18 USB Device Controller

The AX6800x built-in 2/4 USB Device Controllers, compliant USB 2.0 Full-speed standard, supporting data transfer at full speed (12Mbit/s) only.

The USB Device Controller supports 8 controllable Device Addresses and each Device Address supports 8 configurable Endpoints. Each Endpoint supports four kinds of transfer types, Control, Bulk, Interrupt and Isochronous. AX6800x provides the programmable Maximum packet size and buffer Size for these transfer types. The USB Device Controller can reference the Endpoint Index Table in xDATA memory for the pointer of the Endpoint buffers to store the receiving/transmitting packet data to/from xDATA memory.

Each USB Device Controller integrated the controllable pull up resistance. It can be enabled when software detected the VBUS supplied from external Host Controller (Attached) or disabled to disconnect the external Host Device. Furthermore, the USB Device Controller also supports suspend function when bus idle over the specification of USB standard and wakeup function for USB resume protocol, bus reset and cable plug/unplug.

The USB Device Controller responds the device status like USB bus status, endpoint transfer status, enhanced IN-NAK status (responded the host when data not ready for IN transfer) for bulk transfer and other endpoint status to CPU used by registers and interrupt. There is a 16-stage FIFO to record the endpoint transfer success status for the interrupt status register. Software uses them to handle Endpoint transaction protocol with the external host controller.

3.0 Memory Map Description

3.1 Hardware Configuration with Flash information Memory Map

The Hardware Configuration in flash information page is used to store the chip hardware settings for the multi-function pin related settings.

The Hardware Configuration settings are from 0x000 ~ 0x00F in flash information page. It will be loaded into the chip by the Program Loader after chip power on reset.

The Software Configuration settings are from 0x010 in same information page. It is reserved for the Firmware used. Normally software will store some important parameters like vender ID, product ID and so on … in this field and will be used by the CPU Driver during initialization.

Below table shows the Hardware Configuration (HWCFG) memory map.

Table 3-1: Hardware Configuration Flash Information Memory Map

Offset	Description
0x000	Flag
0x003 ~ 0x001	Multi-function Pin Setting 2 ~ 0 (3 Bytes, 0: LSB)
0x004	Programmable USB Pull Disable
0x005	Reserved
0x00F ~ 0x006	Reserved for Hardware future use
0x2FF ~ 0x010	Reserved for Software Configuration settings
0x3FF ~ 0x300	Reserved for Flash manufacturing use

3.1.1 Flag (0x00)

This field indicated the Hardware Parameter Setting is valid or not. The value should be 0xA6 to indicate those Hardware settings have been programed into information sector normally and Bootloader can use these values to configure the hardware. If the setting is invalid, bootloader will not load these values and will remind the multi-function IO in blocked state.

3.1.2 Multi-function Pin Setting (0x03 ~ 0x01)

Multi-function Pin Setting 0 (0x01)

Bit	7	6	5	4	3	2	1	0
Name	MP1_7_PSEL	MP1_6_PSEL	MP1_54_PSEL	MP1_32_PSEL	MP1_10_PSEL	MP0_74_PSEL	MP0_32_PSEL	MP0_10_PSEL
Reset Value	0	0	0	0	0	0	0	0

Bit	Name	Description
0	MP0_10_PSEL	CPU GPIO Port 0, Bit 1 ~ 0 Pin Select. This selects the desired pin function of below multi-function pins (port 0 or HS UART 1).

QFN Pin #	LQFP Pin #	MP0_10_PSEL = 0	MP0_10_PSEL = 1
9	12	P00	RXD1
10	15	P01	TXD1

Bit	Name	Description
1	MP0_32_PSEL	CPU GPIO Port 0, Bit 3 ~ 2 Pin Select. This selects the desired pin function of below multi-function pins (port 0 or HS UART 1).

QFN Pin #	LQFP Pin #	MP0_32_PSEL = 0	MP0_32_PSEL = 1
11	17	P02	RTS1/DE1
13	20	P03	DTR1/RE1

Bit	Name	Description
2	MP0_74_PSEL	CPU GPIO Port 0, Bit 7 ~ 4 Pin Select. This selects the desired pin function of below multi-function pins (port 0 or SPI Master).

QFN Pin #	LQFP Pin #	MP0_74_PSEL = 0	MP0_74_PSEL = 1
38	60	P04	MSS0
21	35	P05	MSCLK
35	55	P06	MMOSI
34	53	P07	MMISO

Bit	Name	Description
3	MP1_10_PSEL	CPU GPIO Port 1, Bit 1 ~ 0 Pin Select. This selects the desired pin function of below multi-function pins (port 1 or Timer0).

QFN Pin #	LQFP Pin #	MP1_10_PSEL = 0	MP1_10_PSEL = 1
--	9	P10	TM0_CK
--	14	P11	TM0_GT

Bit	Name	Description
4	MP1_32_PSEL	CPU GPIO Port 1, Bit 3 ~ 2 Pin Select. This selects the desired pin function of below multi-function pins (port 1 or Timer1).

QFN Pin #	LQFP Pin #	MP1_32_PSEL = 0	MP1_32_PSEL = 1
--	16	P12	TM1_CK
--	18	P13	TM1_GT

<table>
<tr><td>5</td><td>MP1_54_
PSEL</td><td>CPU GPIO Port 1, Bit 7 ~ 4 Pin Select.
This selects the desired pin function of below multi-function pins (port 1 or Timer2).

<table><tr><th rowspan="2">QFN
Pin #</th><th rowspan="2">LQFP
Pin #</th><th colspan="2">MP1_54_PSEL</th></tr><tr><th>= 0</th><th>= 1</th></tr><tr><td>--</td><td>46</td><td>P14</td><td>TM2_CK</td></tr><tr><td>--</td><td>43</td><td>P15</td><td>TM2_GT</td></tr></table></td></tr>
<tr><td>6</td><td>MP1_6_
PSEL</td><td>CPU GPIO Port 1, Bit 6 Pin Select.
This selects the desired pin function of below multi-function pins (port 1 or INT0/external wakeup).

<table><tr><th rowspan="2">QFN
Pin #</th><th rowspan="2">LQFP
Pin #</th><th colspan="2">MP1_6_PSEL</th></tr><tr><th>= 0</th><th>= 1</th></tr><tr><td>--</td><td>41</td><td>P16</td><td>INT0/EXT</td></tr></table></td></tr>
<tr><td>7</td><td>MP1_7_
PSEL</td><td>CPU GPIO Port 1, Bit 7 Pin Select.
This selects the desired pin function of below multi-function pins (port 1 or MSS2).

<table><tr><th rowspan="2">QFN
Pin #</th><th rowspan="2">LQFP
Pin #</th><th colspan="2">MP1_7_PSEL</th></tr><tr><th>= 0</th><th>= 1</th></tr><tr><td>--</td><td>39</td><td>P17</td><td>MSS2</td></tr></table></td></tr>
</table>

Multi-function Pin Setting 1 (0x02)

Bit	7	6	5	4	3	2	1	0
Name	I2C_U1_PSEL	I2C_U0_PSEL	MP3_74_PSEL	MP3_30_PSEL	MP2_76_PSEL	MP2_54_PSEL	MP2_31_PSEL	MP2_0_PSEL
Reset Value	0	0	0	0	0	0	0	0

Bit	Name	Description
0	MP2_0_PSEL	CPU GPIO Port 2, Bit 0 Pin Select. This selects the desired pin function of below multi-function pins (port 2 or MSS1).

QFN Pin #	LQFP Pin #	MP2_0_PSEL = 0	MP2_0_PSEL = 1
23	38	P20	MSS1

Bit	Name	Description
1	MP2_31_PSEL	CPU GPIO Port 2, Bit 3 ~ 1 Pin Select. This selects the desired pin function of below multi-function pins (port 2 or DOCD).

QFN Pin #	LQFP Pin #	MP2_31_PSEL = 0	MP2_31_PSEL = 1
36	57	P21	DB_DI
20	33	P22	DB_CKO
19	31	P23	DB_DO

Bit	Name	Description
2	MP2_54_PSEL	CPU GPIO Port 2, Bit 5 ~ 4 Pin Select. This selects the desired pin function of below multi-function pins (port 2 or HSUART).

QFN Pin #	LQFP Pin #	MP2_54_PSEL = 0	MP2_54_PSEL = 1
17	28	P24	CTS1
16	25	P25	DSR1

Bit	Name	Description
3	MP2_76_PSEL	CPU GPIO Port 2, Bit 7 ~ 6 Pin Select. This selects the desired pin function of below multi-function pins (port 2 or HSUART).

QFN Pin #	LQFP Pin #	MP2_76_PSEL = 0	MP2_76_PSEL = 1
15	23	P26	RI1
14	22	P27	DCD1

Bit	Name	Description
4	MP3_30_PSEL	CPU GPIO Port 3, Bit 3 ~ 0 Pin Select. This selects the desired pin function of below multi-function pins (port 3 or SPI Slave).

QFN Pin #	LQFP Pin #	MP3_30_PSEL = 0	MP3_30_PSEL = 1
--	36	P30	SSS
--	34	P31	SSCLK
--	32	P32	SMOSI
--	29	P33	SMISO

Bit	Name	Description
5	MP3_74_PSEL	CPU GPIO Port 3, Bit 7 ~ 4 Pin Select. This selects the desired pin function of below multi-function pins (port 3 or PS/2).

QFN Pin #	LQFP Pin #	MP3_74_PSEL = 0	MP3_74_PSEL = 1
--	27	P34	PS2A_CK
--	26	P35	PS2A_D
--	24	P36	PS2B_CK
--	21	P37	PS2B_D

<table>
<tr>
<td>6</td>
<td>I2C_U0_
PSEL</td>
<td>I2C Slave port 0 Pin Select.
This selects the desired pin function of below multi-function pins (I2C slave port0 or Port0).

<table>
<tr><th rowspan="2">QFN
Pin #</th><th rowspan="2">LQFP
Pin #</th><th colspan="2">I2C_U0_PSEL</th></tr>
<tr><th>= 0</th><th>= 1</th></tr>
<tr><td>4</td><td>6</td><td>U0_SCL</td><td>P04</td></tr>
<tr><td>5</td><td>7</td><td>U0_SDA</td><td>P05</td></tr>
</table>
Note: if MP0_74_PSEL = 1’b0, the I2C_U0_PSEL will be forced to 1’b0 automatically.</td>
</tr>
<tr>
<td>7</td>
<td>I2C_U1_
PSEL</td>
<td>I2C Slave port 1 Pin Select.
This selects the desired pin function of below multi-function pins (I2C slave port1 or Port0).

<table>
<tr><th rowspan="2">QFN
Pin #</th><th rowspan="2">LQFP
Pin #</th><th colspan="2">I2C_U1_PSEL</th></tr>
<tr><th>= 0</th><th>= 1</th></tr>
<tr><td>1</td><td>2</td><td>U1_SCL</td><td>P06</td></tr>
<tr><td>2</td><td>4</td><td>U1_SDA</td><td>P07</td></tr>
</table>
Note: if MP0_74_PSEL = 1’b0, the I2C_U1_PSEL will be forced to 1’b0 automatically.</td>
</tr>
</table>

Multi-function Pin Setting 2 (0x03)

Bit	7	6	5	4	3	2	1	0
Name	Reserved				SPI_SW_PSEL	BUZZER_PSEL	USB_D1_PSEL	USB_D0_PSEL
Reset Value					0	0	0	0

Bit	Name	Description
0	USB_D0_PSEL	USB Down Stream Port 0 Pin Select. This selects the desired pin function of below multi-function pins (USB D0 or port 0). **QFN Pin # / LQFP Pin # / USB_D0_PSEL** **= 0 / = 1** 42 / 65 / D0_VBEN / P00 40 / 63 / D0_VOC / P01 Note: if MP0_10_PSEL = 1'b0, the USB_D0_PSEL will be forced to 1'b0 automatically.
1	USB_D1_PSEL	USB Down Stream Port 1 Pin Select. This selects the desired pin function of below multi-function pins (USB D1 or port 0). **QFN Pin # / LQFP Pin # / USB_D1_PSEL** **= 0 / = 1** 41 / 64 / D1_VBEN / P02 39 / 62 / D1_VOC / P03 Note: if MP0_32_PSEL = 1'b0, the USB_D1_PSEL will be forced to 1'b0 automatically.
2	BUZZER_PSEL	Buzzer Pin Select. This selects the desired pin function of below multi-function pins (Buzzer or MSS2). **QFN Pin # / LQFP Pin # / BUZZER_PSEL** **= 0 / = 1** 25 / 40 / BUZZER / MSS2 Note: if MP1_7_PSEL = 1'b1, the BUZZER_PSEL will be forced to 1'b0 automatically.
3	SPI_SW_PSEL	SPI Master and Slave pin swap. Set this bit to 1 will swap the pin between SPI master and Slave. **QFN Pin # / LQFP Pin # / MP3_30_PSEL** **= 0 / = 1** P04 / P04 / MSS0 / SSS P05 / P05 / MSCLK / SSCLK P06 / P06 / MMOSI / SMOSI P07 / P07 / MMISO / SMISO P30 / P30 / SSS / MSS0 P31 / P31 / SSCLK / MSCLK P32 / P32 / SMOSI / MMOSI P33 / P33 / SMISO / MMISO
7:4		Reserved

3.1.3 Programmable USB Pull Disable (0x04)

Programmable USB Pull Disable (0x04)

Bit	7	6	5	4	3	2	1	0
Name	D3PD	D2PD	D1PD	D0PD	U3PU	U2PU	U1PU	U0PU
Reset Value	0	0	0	0	0	0	0	0

Bit	Name	Description
0	U0PU	USB Up Stream Port0 pull up disable 1: force the D+ 1.5K pull up disable. 0: Control the D+ pull up by Hardware automatically. Note: when set this bit to 1, should add the external 1.5K pull up for D+ off-chip.
1	U1PU	USB Up Stream Port1 pull up disable 1: force the D+ 1.5K pull up disable. 0: Control the D+ pull up by Hardware automatically. Note: when set this bit to 1, should add the external 1.5K pull up for D+ off-chip.
2	U2PU	USB Up Stream Port2 pull up disable 1: force the D+ 1.5K pull up disable. 0: Control the D+ pull up by Hardware automatically. Note: when set this bit to 1, should add the external 1.5K pull up for D+ off-chip.
3	U3PU	USB Up Stream Port3 pull up disable 1: force the D+ 1.5K pull up disable. 0: Control the D+ pull up by Hardware automatically. Note: when set this bit to 1, should add the external 1.5K pull up for D+ off-chip.
4	D0PD	USB Down Stream Port0 pull down disable 1: force the D+ and D- 15K pull down disable. 0: always pull down the D+ and D- by 15K ohm. Note: when set this bit to 1, should add the external 15K pull down for D+/D- off-chip.
5	D1PD	USB Down Stream Port1 pull down disable 1: force the D+ and D- 15K pull down disable. 0: always pull down the D+ and D- by 15K ohm. Note: when set this bit to 1, should add the external 15K pull down for D+/D- off-chip.
6	D2PD	USB Down Stream Port2 pull down disable 1: force the D+ and D- 15K pull down disable. 0: always pull down the D+ and D- by 15K ohm. Note: when set this bit to 1, should add the external 15K pull down for D+/D- off-chip.
7	D3PD	USB Down Stream Port3 pull down disable 1: force the D+ and D- 15K pull down disable. 0: always pull down the D+ and D- by 15K ohm. Note: when set this bit to 1, should add the external 15K pull down for D+/D- off-chip.

3.1.4 Reserved (0x05)

This field should be set to 0x00.

3.2 Program Memory Map

The CPU has separated address spaces for program and data memory. The Program Memory, Internal Data Memory, External Data Memory (xDATA), SFRs areas each has its own address spaces.

As shown in below figure, the CPU core can address up to 128K bytes of linear program space without bank select. The CPU starts execution of program code at location 0x000000 in LARGE mode, after each reset. The CPU can be then switched to FLAT mode to support 128K bytes of linear program code space.

Program Protection Bit is used to protect the program code be read by ISP or DoCD. This bit is located at the bit7 in the last byte of first 8K in flash memory (address 0x01FFF, bit7). If this bit is set to '0', it will enable the program code protection. Only perform the flash Mass Erase can set this bit back to '1' to unprotect the program code.

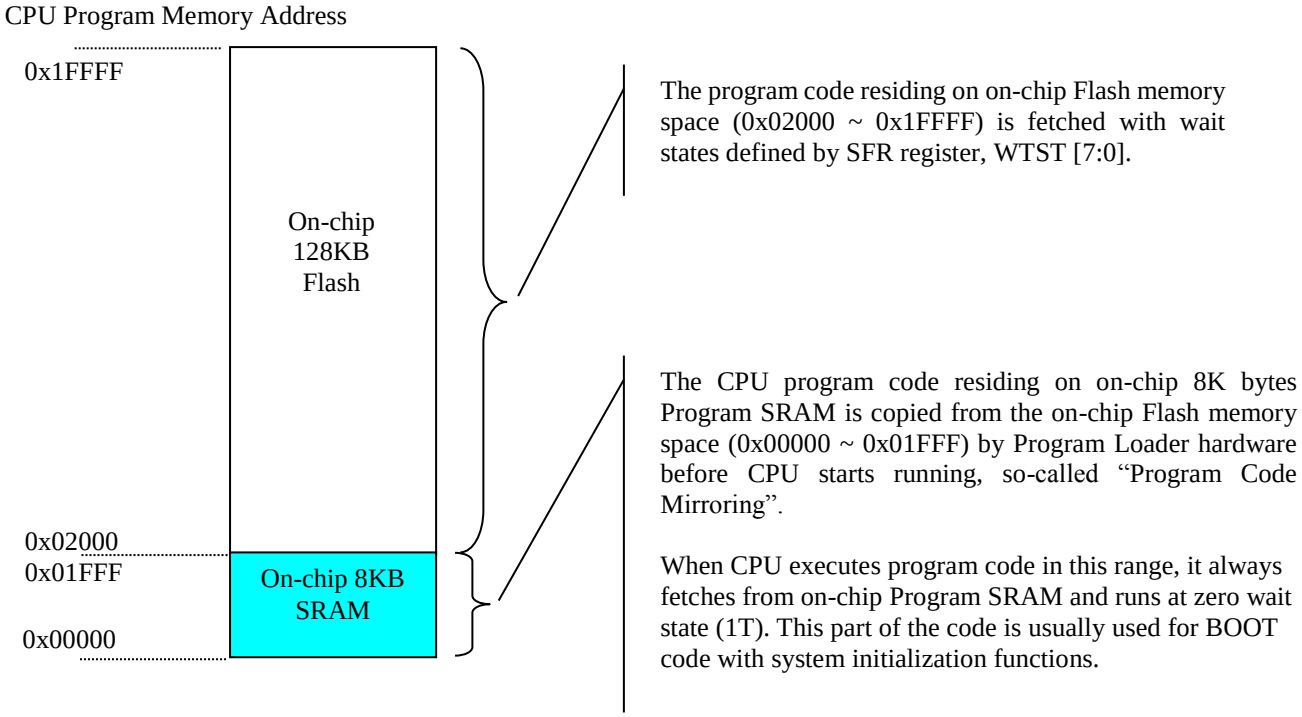


Figure 3-1: The Program Memory Map of CPU

3.3 External Data (xDATA) Memory Map

The data memory of CPU core is divided onto 32 Kbytes of External Data (xDATA) Memory and 256 bytes of Internal Data Memory, plus a 128-bytes of SFR memory area.

The CPU core can address up to 32 Kbytes of External Data (xDATA) memory space without bank select. The xDATA memory is accessed by MOVX instructions only.

3.4 Internal Data Memory and SFR Register Map

The figure below shows the Internal Data Memory (256 bytes) and Special Function Register (SFR) map of CPU core. The lower internal memory consists of four register banks with eight registers each; a bit addressable segment with 128 bits (16 bytes) begins at 0x20, and a scratch pad area with 208 bytes. With the indirect addressing mode, range 0x80 to 0xFF of the highest 128 bytes of the internal memory is addressed. With the direct addressing mode, range 0x80 to 0xFF, the SFR memory area is accessed.

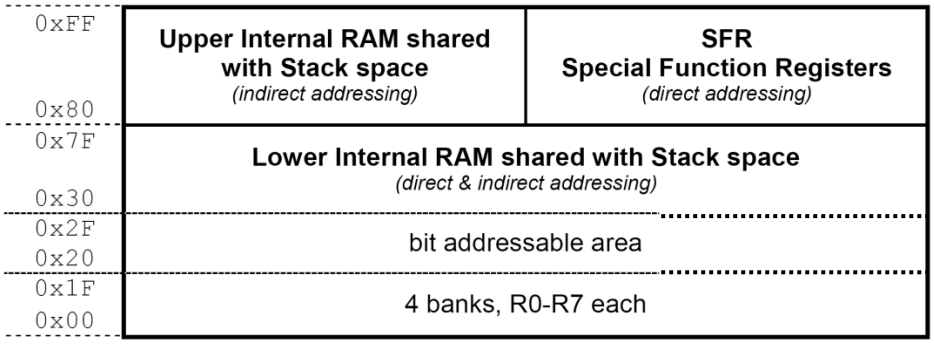


Figure 3-2: The Internal Memory Map of CPU

Table 3-2 below shows the CPU SFR Register Map. Note that all registers in the column with Offset+0 are bit addressable.

SFR Offset	Offset + 0	Offset + 1	Offset + 2	Offset + 3	Offset + 4	Offset + 5	Offset + 6	Offset + 7
0xF8	**EIP**							
0xF0	**B**							
0xE8	**EIE**	**STATUS**	**MXAX**	**TA**	*SPICIR*	*SPIDR*		
0xE0	**ACC**		*MCIR*	*MDR*	*U1CIR*	*U1DR*		
0xD8	**WDCON**	*SDSTSR*	*DCIR*	*DDR*	PS2CIR	PS2DR		*CRR*
0xD0	**PSW**	*FCIR*	*FDR*	*FCISR*	*FCDP*	*PCKEN*		
0xC8	**T2CON**		**RLDL**	**RLDH**	**TL2**	**TH2**		
0xC0					*HCIS*	*HCOIS*	*HCCIR*	*HCDR*
0xB8	**IP**			*DC3ISR*	*DC3INSR*	*DC3ESMR*	*DC3CIR*	*DC3DR*
0xB0	**P3**			*DC2ISR*	*DC2INSR*	*DC2ESMR*	*DC2CIR*	*DC2DR*
0xA8	**IE**			*DC1ISR*	*DC1INSR*	*DC1ESMR*	*DC1CIR*	*DC1DR*
0xA0	**P2**			*DC0ISR*	*DC0INSR*	*DC0ESMR*	*DC0CIR*	*DC0DR*
0x98	**SCON0**	**SBUF0**			*WKUPSR*	**ACON**	*PISSR*	*UDCSR*
0x90	**P1**	**EIF**	**WTST**	**DPX0**		**DPX1**	*I2CCIR*	*I2CDR*
0x88	**TCON**	**TMOD**	**TL0**	**TL1**	**TH0**	**TH1**	**CKCON**	*CSRR*
0x80	**P0**	**SP**	**DPL0**	**DPH0**	**DPL1**	**DPH1**	**DPS**	**PCON**

Bolded: are 1T-80390 CPU core related registers.
Italic: AX6800x's peripheral function's registers.
(M): SFR register available in Local Bus Master Mode.
(S): SFR register available in Local Bus Slave Mode.
(D): SFR register available in Digital Video Port Mode.

Table 3-2: The CPU SFR Register Map

4.0 Electrical Specification

4.1 DC Characteristics

4.1.1 Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
VDDK, VDD_FLASH	Digital core power supply.	- 0.5 to 2.5	V
VDDIO	Power supply of 3.3V I/O.	- 0.5 to 4.6	V
VDDA_PLL	Analog power supply for PLL.	- 0.5 to 2.5	V
VDDA_USB	Analog power supply for 3.3V USB I/O.	- 0.5 to 4.6	V
V_{IN}	Input voltage of 3.3V I/O.	- 0.5 to 4.6	V
	Input voltage of 3.3V I/O with 5V tolerant.	- 0.5 to 6	V
U[3:0]_DP, U[3:0]_DM, D[3:0]_DP, D[3:0]_DM	Input Voltage of USB I/O	- 0.5 to 6	V
T_{STG}	Storage temperature.	- 65 to 150	℃
I_{IN}	DC input current.	50	mA
I_{OUT}	Output short circuit current.	50	mA

Note:
Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted in the recommended operating condition section of this datasheet. Exposure to absolute maximum rating condition for extended periods may affect device reliability.

4.1.2 Recommended Operating Condition

Symbol	Parameter	Min	Typ	Max	Units
VDDIO	Power supply of 3.3V I/O.	2.97	3.3	3.63	V
VDDK, VDD_FLASH	Digital core power supply.	1.62	1.8	1.98	V
VDDA_PLL	Analog power supply for PLL.	1.62	1.8	1.98	V
VDDA_USB	Analog power supply for USB I/O.	3.0	3.3	3.6	V
V_{IN}	Input voltage of 3.3 V I/O.	0	3.3	3.63	V
	Input voltage of 3.3 V I/O with 5 V tolerant.	0	3.3	5.25	V
Tj	AX6800x operating junction temperature.	-40	25	105	℃
Ta	AX6800x operating ambient temperature.	0	-	70	℃

4.1.3 Leakage Current and Capacitance

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{IN}	Input leakage current. No pull-up or pull-down.	3.3V IO pins. Vin = 3.3 or 0V.	-	±1	-	μA
		3.3V with 5V tolerant I/O pins. Vin = 5 or 0V.	-	±1	-	μA
I_{OZ}	Tri-state leakage current.		-	±1	-	μA
C_{PAD}	Pad capacitance.		-	-	5	pF

Note:
The capacitance listed above includes pad capacitance and package capacitance.

4.1.4 DC Characteristics of 3.3V with 5V Tolerant I/O Pins

Symbol	Parameter	Conditions	Min	Typ	Max	Units
VDDIO	Power supply of 3.3V I/O.	3.3V I/O	2.97	3.3	3.63	V
Vil	Input low voltage.	LVTTL	-	-	0.8	V
Vih	Input high voltage.		2.0	-	-	V
Vt	Switching threshold.		0.85	0.97	1.09	V
Vt-	Schmitt trigger negative going threshold voltage.	LVTTL	1.0	1.05	1.13	V
Vt+	Schmitt trigger positive going threshold voltage		1.85	2.02	2.22	V
Vol	Output low voltage.	|Iol| = 8.65mA(Typ)	-	-	0.4	V
Voh	Output high voltage.	|Ioh| = 11.2mA(Typ)	2.4	-	-	V
Vopu (1)	Output pull-up voltage for 5V tolerant IO	With internal pull-up resistor	VDDIO – 0.9	-	-	V
Iol	Output low current.	Vol = 0.4V	5.32	8.65	12	mA
Ioh	Output high current.	Voh = 2.4V	5.52	11.2	18.9	mA
Rpu	Input pull-up resistance.		59.2	73.4	94.9	KΩ
Rpd	Input pull-down resistance.		54.4	74.3	120	KΩ
Iin	Input leakage current.	Vin = 5 or 0V	-	-	1	μA
	Input leakage current with pull-up resistance.	Vin = 0 V	13.4	22.1	34.9	μA
	Input leakage current with pull-down resistance.	Vin = VDDIO	9.98	21.1	39.2	μA
Ioz	Tri-state output leakage current.	Vin = 5.5V or 0	-	-	1	μA

Note:
1. This parameter indicates that the pull-up resistor for the 5V tolerant I/O pins cannot reach VDDIO DC level even without DC loading current.

4.1.5 USB Transceivers Specification

The below specifications are measured under the following conditions, unless stated otherwise:
VDDIO = VDDA_USB = 3.3 V; VDDK = 1.8 V; external pull-up 1.5KΩ or external pull-down 15KΩ; external series resistances (Rs=27Ω); T_a = 25 ℃.

Symbol	Description	Conditions	Min	Typ	Max	Units
Analog Inputs/Outputs (U[3:0]_DP, U[3:0]_DM, D[3:0]_DP, D[3:0]_DM)						
V_{DI}	Differential Input Sensitivity	$\|V_{DP}-V_{DM}\|$	0.2	-	-	V
V_{CM}	Differential Common-Mode Voltage	Includes V_{DI} range	0.8	-	2.5	V
V_{ILSE}	Single-Ended input Low Voltage	-	-	-	0.8	V
V_{IHSE}	Single-Ended input High Voltage	-	2.0	-	-	V
V_{OL}	Output-Voltage Low	R_L = 1.5KΩ to +3.6V	-	-	0.3	V
V_{OH}	Output-Voltage High	R_L = 15KΩ to VSS	2.8	-	-	V
I_{LZ}	Off-State Leakage Current		-10	-	10	uA
Z_{DRV}	Driver Output Impedance	Steady-state drive	24	-	44	Ω
R_{PU}	Internal Pull-up Resistance		0.89		1.575	KΩ
R_{PD}	Internal Pull-down Resistance		14.25		35	KΩ
AC Specification						
T_{FR}	Full-Speed Rise Time	10% to 90% of $\|V_{OH} - V_{OL}\|$, C_L=50pF	4	-	20	ns
T_{FF}	Full-Speed Fall Time	90% to 10% of $\|V_{OH} - V_{OL}\|$, C_L=50pF	4	-	20	ns
T_{LR}	Low-Speed Rise Time	10% to 90% of $\|V_{OH} - V_{OL}\|$, C_L=200pF ~ 600pF	75	-	300	ns
T_{LF}	Low-Speed Fall Time	90% to 10% of $\|V_{OH} - V_{OL}\|$, C_L=200pF ~ 600pF	75	-	300	ns
T_{RFM}	Rise/Fall-Time Matching	Excluding the first transition from idle state	90	-	111	%
V_{CRS}	Output-Signal Crossover Voltage	Excluding the first transition from idle state	1.3	-	2.0	V

4.2 Power Consumption

AX68002 chip only power consumption

Item	Conditions	VDDIO + VDDK + VDD_FLASH Analog (VDDA_USB + VDDA_PLL)		Units
		48Mhz	96Mhz	
CPU in Full Speed operation	KVM application with heavy traffic.	60	92	mA
CPU in STOP mode	CPU clock stops, 12MHz Crystal Oscillation/96MHz PLL clock still runs.	17	17	mA
Deep Sleep mode	CPU clock stops, 12MHz Crystal Oscillation/96MHz PLL clock stops.	9	9	mA

Note:
Above current value are typical values measured on AX68002 development board.

Symbol	Description	Conditions	Min	Typ	Max	Units
Θ_{JC}	Thermal resistance of junction to case	64-pin QFP package	-	6.1	-	℃/W
Θ_{JA}	Thermal resistance of junction to ambient	64-pin QFP package, still air	-	29.8	-	℃/W

AX68004 chip only power consumption

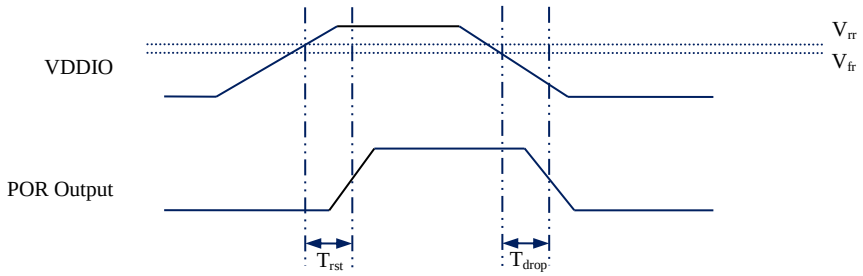
Item	Conditions	VDDIO + VDDK + VDD_FLASH Analog (VDDA_USB + VDDA_PLL)		Units
		48Mhz	96Mhz	
CPU in Full Speed operation	KVM application with heavy traffic.	78	118	mA
CPU in STOP mode	CPU clock stops, 12MHz Crystal Oscillation/96MHz PLL clock still runs.	15	15	mA
Deep Sleep mode	CPU clock stops, 12MHz Crystal Oscillation/96MHz PLL clock stops.	8	8	mA

Note:
Above current value are typical values measured on AX68004 development board.

Symbol	Description	Conditions	Min	Typ	Max	Units
Θ_{JC}	Thermal resistance of junction to case	100-pin LQFP package	-	21.0	-	℃/W
Θ_{JA}	Thermal resistance of junction to ambient	100-pin LQFP package, still air	-	42.9	-	℃/W

4.3 Power-On-Reset (POR) Specification

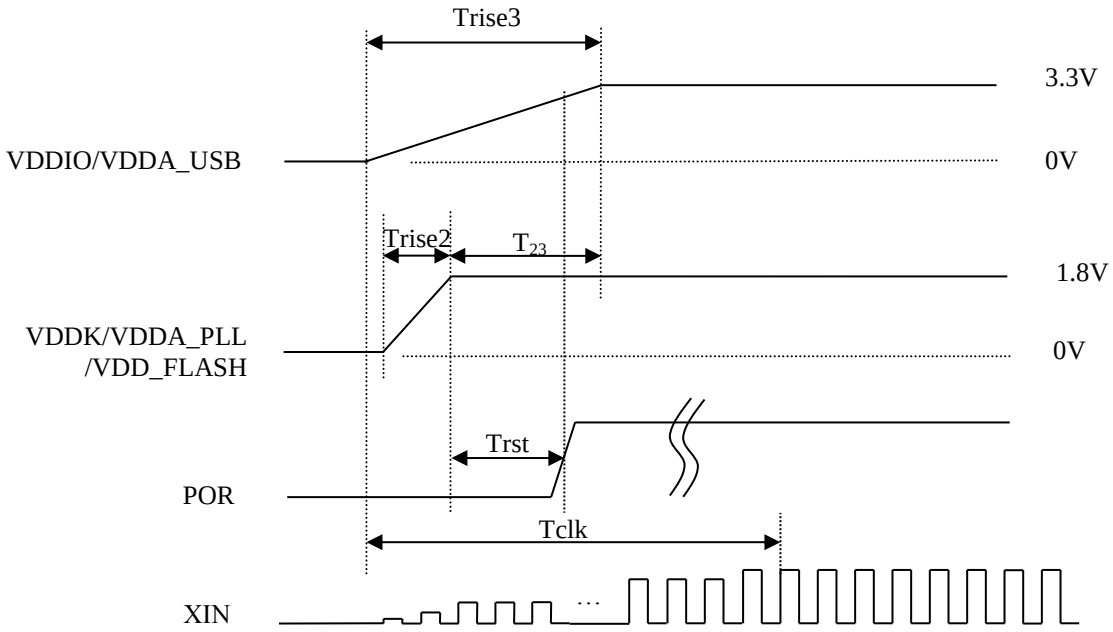
Below figures and table shows the two POR circuit spec during power ramp-up/down.



Symbol	Description	Conditions	Min.	Typ.	Max.	Units
VDDIO	Power supply voltage to be detected	-		3.3		V
V_{rr}	VDDIO rise relax voltage	-			2.85	V
V_{fr}	VDDIO fall release voltage	-	2.1			V
V_{hs}	Power trigger Hysteresis	-	0.15			V
T_{rst}	Reset time after POR trigger up	VDDIO slew rate = 2.5V / 1ms		50		µs
T_{drop}	Drop time of VDDIO to reset	VDDIO slew rate = 2.5V / 1ms		50		µs

4.4 Power-up/-down Sequence

Power-up Sequence

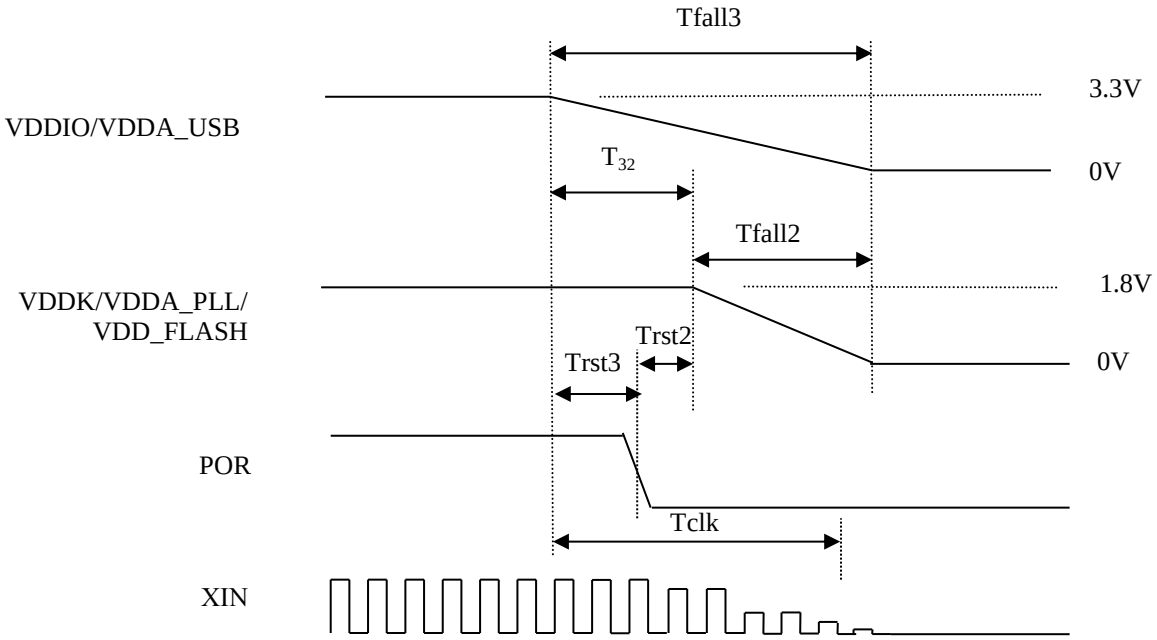


Symbol	Parameter	Conditions	Min	Typ	Max	Units
T_{rise3}	3.3V power supply rise time.	From 0V to 3.3V.	-	1.5	-	ms
T_{rise2}	1.8V power supply rise time.	From 0V to 1.8V.	-	240	-	us
T_{23}	VDDK rising to 1.8V to VDDIO rising to 3.3V interval.		-	1.2	-	ms
Tclk	12MHz crystal oscillator start-up time.	From VDDIO rising to 3.3V to clock stable of 12MHz crystal oscillator.	-	2.0	-	ms
Trst	POR asserted low level interval.	From VDDK rising to 1.8V to POR going high.	-	920	-	us

Note:
1. The above typical timing data is measured from AX6800x test board.
2. The Trst typical value is measured from AX6800x test board with the internal POR.

Figure 4-1: Power-up Sequence Timing Diagram and Table

Power-down Sequence



Symbol	Parameter	Conditions	Min	Typ	Max	Units
T_{fall3}	3.3V power supply fall time.	From 3.3V to 0V.	-	>1	-	s
T_{fall2}	1.8V power supply fall time.	From 1.8V to 0V.	-	700	-	ms
T_{32}	VDDIO falling from 3.3V to VDDK falling from 1.8V interval.		-	8	-	ms
Tclk	12MHz crystal oscillator stop time.	VDDIO falling from 3.3V to last clock transition of 12MHz crystal oscillator.	-	100	-	ms
Trst3	VDD3IO falling from 3.3V to POR asserted low level interval.		-	6.5	-	ms
Trst2	POR asserted low level to VDDK falling from 1.8V interval.		-	1.5	-	ms

Note: The above typical timing data is measured from AX6800x test board.

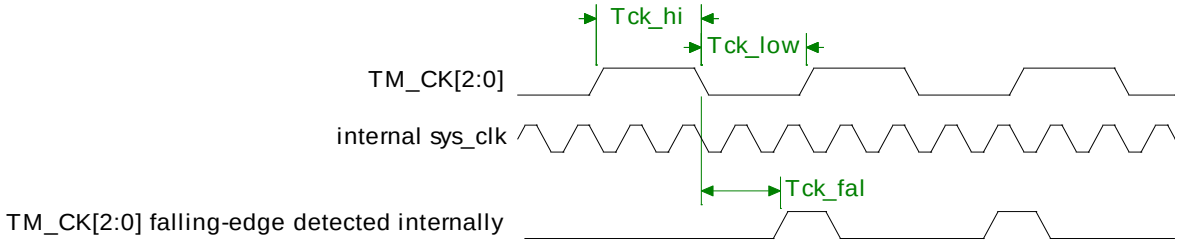
Figure 4-2: Power-down Sequence Timing Diagram and Table

4.5 AC Timing Characteristics

4.5.1 Clock Input Timing Specification

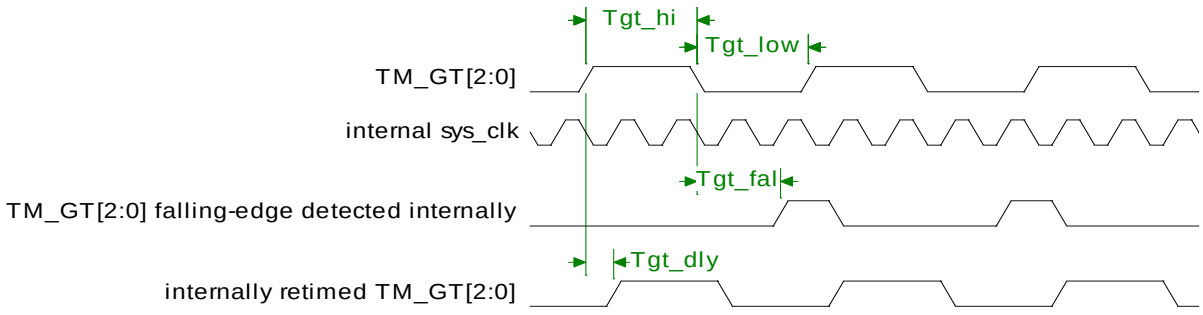
Symbol	Parameter	Min	Typ	Max	Units
-	Nominal Frequency	-	12	-	MHz
-	Frequency Stability	-50	-	+50	ppm
C_L	Crystal Load Capacitance	-	12.5	-	pF

4.5.2 Timer 0/1/2 Interface Timing



Symbol	Description	Min	Typ	Max	Units
Tck_hi	TM_CK[2:0] high pulse width	2	-	-	Tsys_clk
Tck_low	TM_CK[2:0] low pulse width	2	-	-	Tsys_clk
Tck_fal	TM_CK[2:0] falling-edge internal detection time	1 ~ 2	-	2	Tsys_clk

Figure 4-3: TM_CK[2:0] Timing Diagram and Table



Symbol	Description	Min	Typ	Max	Units
Tgt_hi	TM_GT[2:0] high pulse width	2	-	-	Tsys_clk
Tgt_low	TM_GT[2:0] low pulse width	2	-	-	Tsys_clk
Tgt_fal	TM_GT[2:0] falling-edge internal detection time	1 ~ 2	-	2	Tsys_clk
Tgt_dly	TM_GT[2:0] internally retimed delay	0.5	-	1	Tsys_clk

Figure 4-4: TM_GT[2:0] Timing Diagram and Table

4.5.3 High Speed UART

The High Speed UART 1 data transmit and receive is via TXD1 and RXD1 pins. The complete data transmit/receive includes 1 start bit, 5~8 data bit, 1 parity bit (if supported parity check) and 1~2 stop bit. Software can set HS_DLLR, HS_DLHR and HS_DPR register to decide the baud rate. Please refer to HS_DLLR register description for baud rate setting.

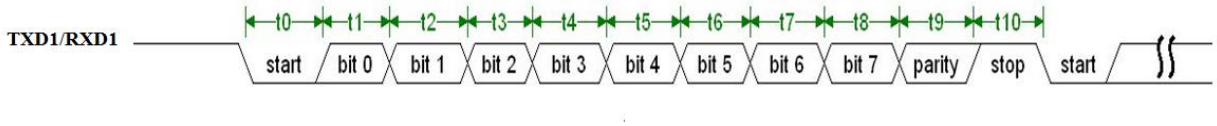
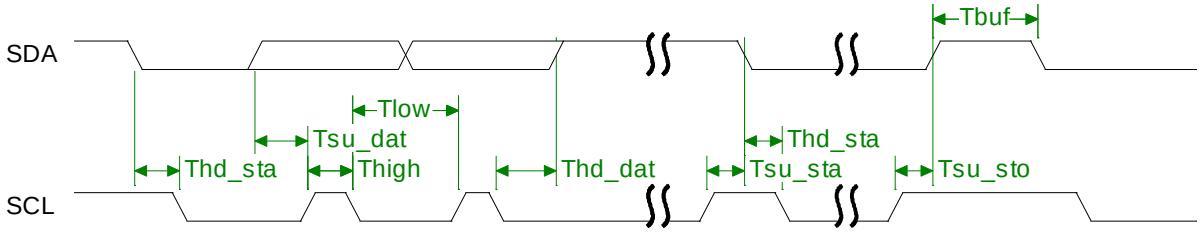


Figure 4-5: TXD1 and RXD1 Timing Diagram

Note:
1. t0 is start bit time; t1 ~ t8 is data bit time; t9 is parity bit time; t10 is stop bit time.
2. t0 ~ t9 = 1/Baud Rate;
   t10 = 1 / baud rate (1 stop bit)
   t10 = 1.5 * (1 / baud rate) (1.5 stop bit)
   t10 = 2 * (1 / baud rate) (2 stop bit)
3. RXD1 baud rate tolerance +/- 3%.

4.5.4 I2C Interface Timing



Symbol	Parameter	Min	Typ	Max	Units
Fclk	SCL clock frequency	-	-	100, 400	KHz
Thd_sta	Hold time of (repeated) START condition. After this period, the first clock pulse is generated	-	2	-	Tprsc[2]
Thigh	High period of the SCL clock	-	2	-	Tprsc
Tlow	Low period of the SCL clock	-	3	-	Tprsc
Tsu_sta	Setup time for a repeated START condition	-	2	-	Tprsc
Tsu_dat	Data Setup time	-	1	-	Tprsc
Thd_dat	Data hold time	-	2	-	Tprsc
Tsu_sto	Setup time for STOP condition	-	3	-	Tprsc
Tbuf	Bus free time between a STOP and START condition	-	4	-	Tprsc

Table 4-1: I2C Master Controller Timing Table

Symbol	Parameter	Min	Typ	Max	Units
Fclk	SCL clock frequency	-	-	380	KHz
Thd_sta	Hold time of (repeated) START condition. After this period, the first clock pulse is generated	1	-	-	Tsys_clk[3]
Thigh	High period of the SCL clock in Standard mode	4	-	-	µs
	High period of the SCL clock in Fast mode	0.6	-	-	µs
Tlow	Low period of the SCL clock	0.4	-	-	µs
Tsu_sta	Setup time for a repeated START condition	1	-	-	Tsys_clk
Tsu_dat	Data Setup time	3	-	-	Tsys_clk
Thd_dat	Data hold time	0.4	-	-	µs
Tsu_sto	Setup time for STOP condition	1	-	-	Tsys_clk
Tbuf	Bus free time between a STOP and START condition	12	-	-	Tsys_clk

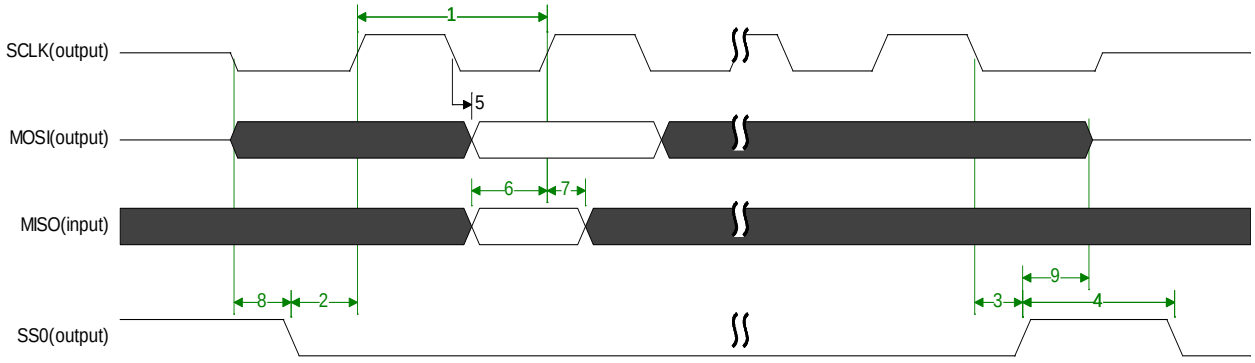
Table 4-2: I2C Slave Controller Timing Table

[2] Tprsc = 1 / Fprsc, where Fprsc = Operating system clock frequency / (PRER + 1). The PRER is I2C Clock Prescale Register.

[3] Tsys_clk = 10.416/20.833ns for 96/48 MHz operating system clock.

4.5.5 High Speed SPI Interface Timing

4.5.5.1 Master Mode



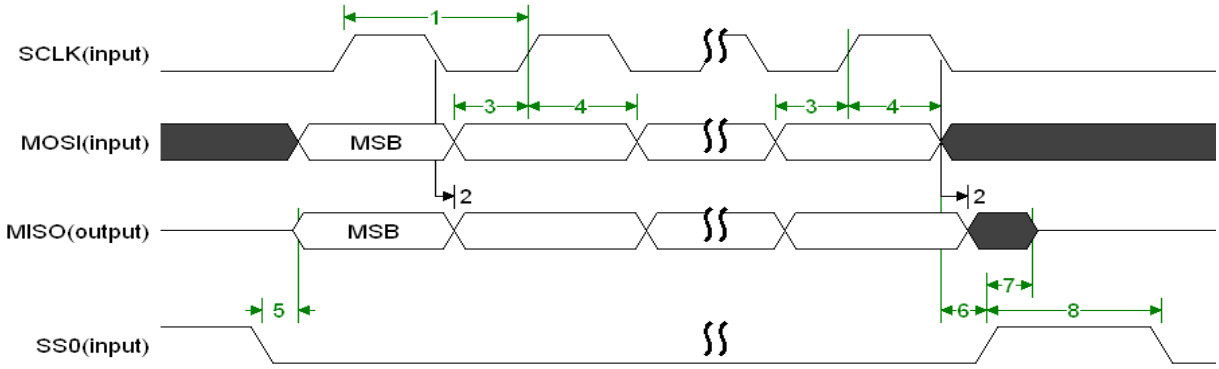
Symbol	Description	Min	Typ	Max	Units
1	SCLK clock frequency	-	$\frac{Fsys\_clk}{(SPIBRR + 1) * 2}$	-	MHz[4]
2	Setup time of SS[2:0] to the first SCLK edge	-	(SPIDS * Tsys_clk[5]) + 0.5 * Tsclk[6]	-	ns
3	Hold time of SS[2:0] after the last SCLK edge	-	(SPIDS * Tsys_clk) + N * Tsclk[7]	-	ns
4	Minimum idle time between transfers (minimum SS[2:0] high time)	-	((32 * SPIDT + 6) * Tsys_clk) + (0.5 * Tsclk)	-	ns
5	MOSI data valid time, after SCLK edge	-	-	0.6	ns
6	MISO data setup time before SCLK edge	13.8	-	-	ns
7	MISO data hold time after SCLK edge	0	-	-	ns
8, 9	Bus drive time before SS[2:0] assertion and after SS[2:0] de-assertion	-	0.5 * Tsclk	-	

Figure 4-6: High Speed SPI Master Controller Timing Diagram and Table

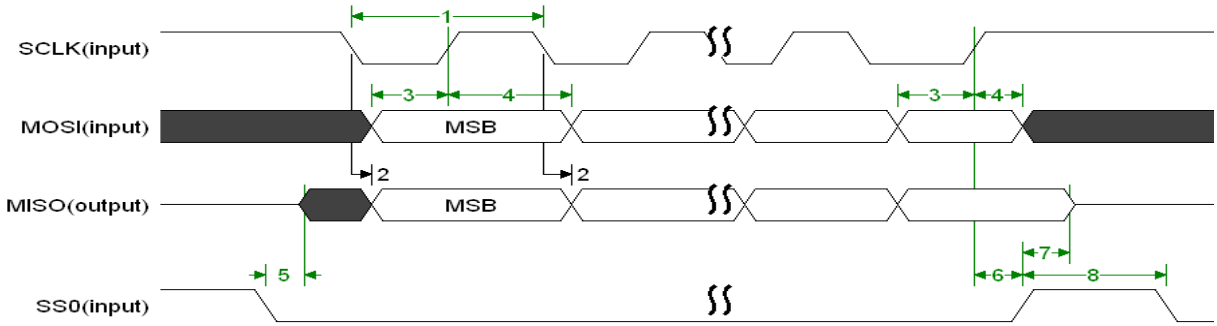
[4] Fsys_clk is the operating system clock frequency, 48 or 96MHz. The SPIBRR is SPI Baud Rate Register.
[5] Tsys_clk = 1 / Fsys_clk, operating system clock period.
[6] Tsclk = SCLK clock period.
[7] The N = 0.5 when operating in Mode 0 or Mode 1; The N = 1 when operating in Mode 2 or Mode 3.

4.5.5.2 Slave Mode

Mode 0



Mode 3

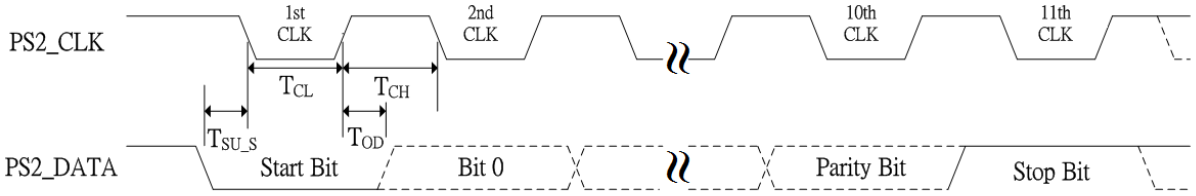


Symbol	Description	Min	Typ	Max	Units
1	SCLK clock frequency	-	-	20	MHz
2	MISO data valid time after SCLK edge	4.4	-	22	ns
3	MOSI data setup time before SCLK edge	1.8	-	-	ns
4	MOSI data hold time after SCLK edge	0.4	-	-	ns
5	SS0 setup time before MISO active	3.6	-	8.2	ns
6	SS0 hold time after SCLK edge	3	-	-	ns
7	MISO data hold time after SS0 de-assertion	1.7	-	4.2	ns
8	SS0 negation to next SS0 assertion time	20	-	-	ns

Figure 4-7: High Speed SPI Slave Controller Timing Diagram and Table

4.5.6 PS/2 Interface Timing

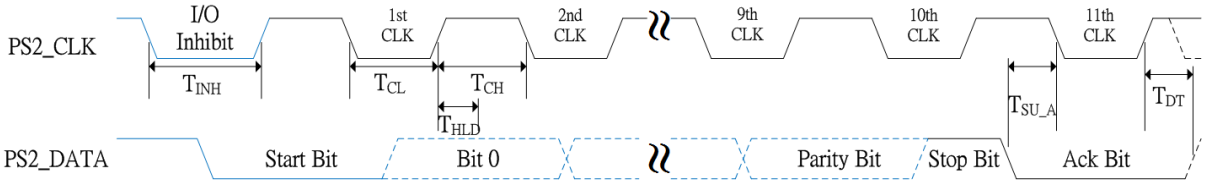
4.5.6.1 PS2 Host Receiving Data Timing



Symbol	Description	Min	Typ	Max	Units
T_{SU_S}	Time from Data transition to falling edge of CLK	5	15	25	us
T_{OD}	Time from rising edge of CLK to Data transition	5	15	T_{CH}-5	us
T_{CL}	Duration of CLK low (inactive)	30	40	50	us
T_{CH}	Duration of CLK high (active)	30	40	50	us
T_{SU_S}	Time from Data transition to falling edge of CLK	5	15	25	us

Figure 4-8: PS2 Host Receiving Data Timing Diagram and Table

4.5.6.2 Host Sending Data Timing

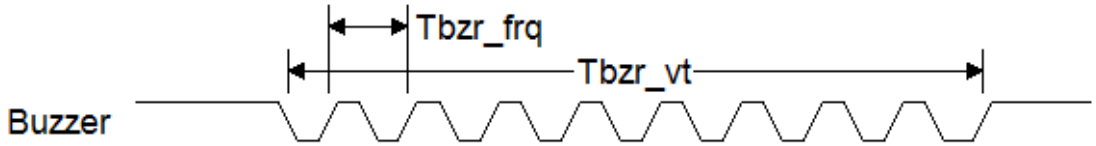


Symbol	Description	Min	Typ	Max	Units
T_{INH}	Host bring CLK low to inhibit I/O (request to send)		(TINH[8] - 1) * 10		us
T_{CL}	Duration of CLK low (inactive)	30	40	50	us
T_{CH}	Duration of CLK high (active)	30	40	50	us
T_{HLD}	Time from low to high CLK transition when Device samples Data	5	15	25	us
T_{SU_A}	Time from falling edge of Data to falling edge of CLK	30	40	50	us
T_{DT}	Time from rising edge of CLK11 to rising edge of Ack Bit	-	-	50	

[8]: The TINH is the Inhibit timing register.

Figure 4-9: PS2 Host Sending Data Timing Diagram and Table

4.5.7 Buzzer Interface Timing



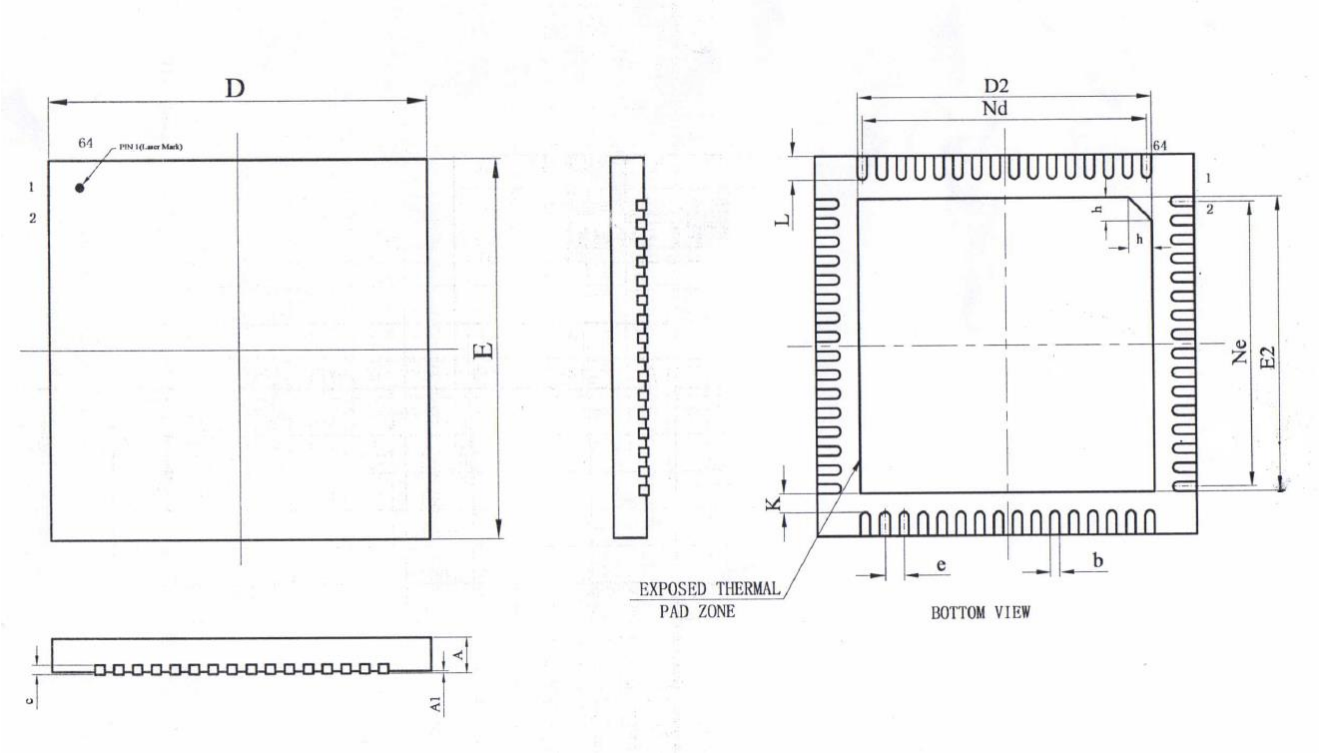
Symbol	Description	Min	Typ	Max	Units
Tbzr_frq	Buzzer Frequency[9]	0	523, 587, 659, 698, 784, 880, 988	988	Hz
Tbzr_vt	Buzzer Voice Time[10]	0.125	2/(BVT+1)	2	Second

[9]: There are 8 frequencies can be selected by setting BFR[2:0] register.
[10]: The BVT[2:0] is Buzzer Voice Time register.

Figure 4-10: Buzzer Output Timing Diagram and Table

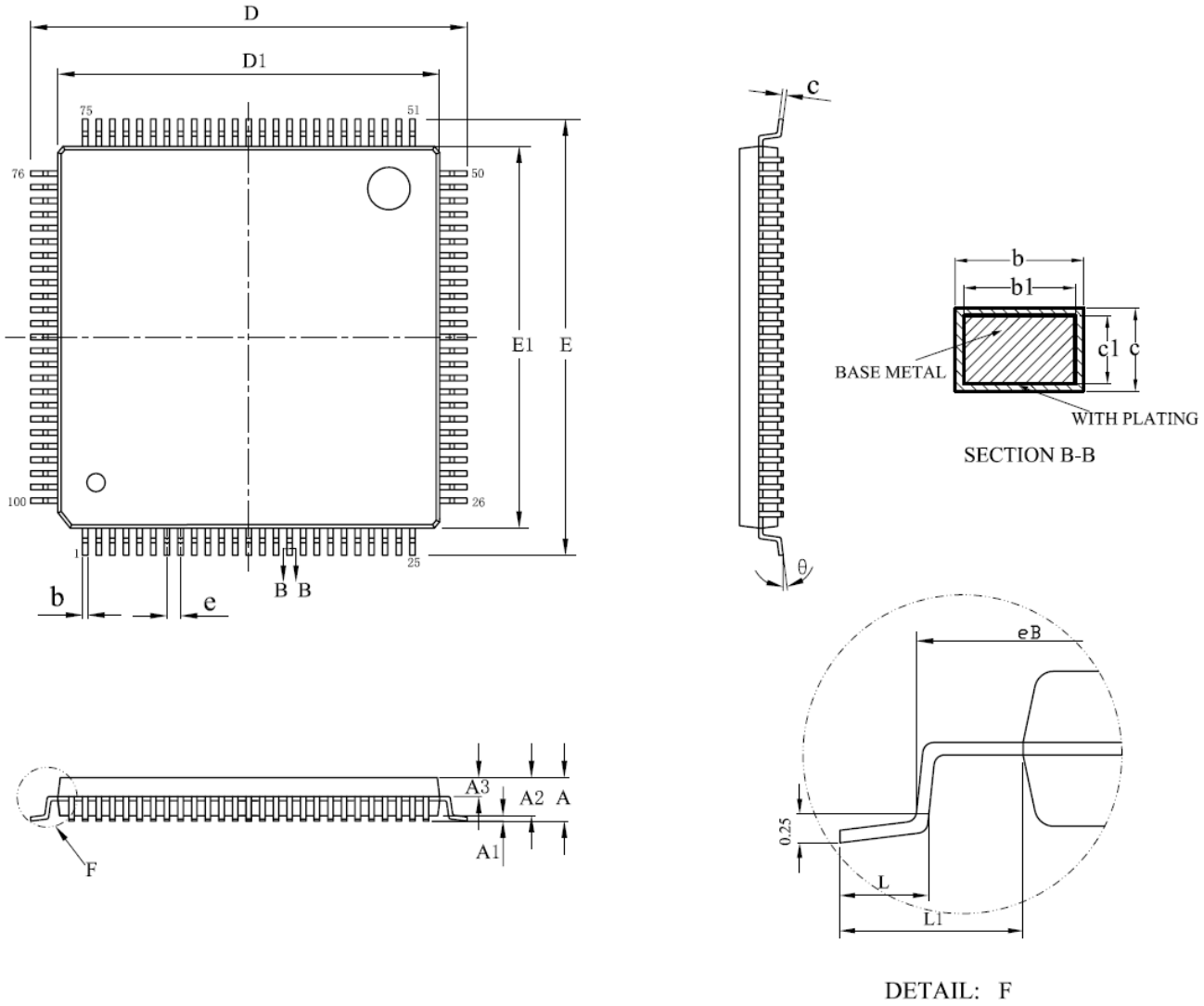
5.0 Package Information

5.1 64-pin QFN package



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	—	0.02	0.05
b	0.15	0.20	0.25
c	0.18	0.20	0.25
D	7.90	8.00	8.10
D2	6.10	6.20	6.30
e	0.40BSC		
Nd	6.00BSC		
E	7.90	8.00	8.10
E2	6.10	6.20	6.30
Ne	6.00BSC		
L	0.45	0.50	0.55
K	0.20	—	—
h	0.30	0.35	0.40

5.2 100-pin LQFP package



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.60
A1	0.05	—	0.20
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.19	—	0.27
b1	0.18	0.20	0.23
c	0.13	—	0.18
c1	0.12	0.13	0.14
D	15.80	16.00	16.20
D1	13.90	14.00	14.10
E	15.80	16.00	16.20
E1	13.90	14.00	14.10
eB	15.05	—	15.35
e	0.50BSC		
L	0.45	—	0.75
L1	1.00BSC		
θ	0	—	7°

6.0 Ordering Information

Part Number	Description
AX68002 QF	64-pin QFN lead Free package, commercial temperature range: 0 to 70℃.
AX68004 LF	100-pin LQFP lead Free package, commercial temperature range: 0 to 70℃.

7.0 Revision History

Revision	Date	Comments
V1.00	2015/01/16	Initial release.
V1.01	2015/02/05	Corrected package information in Section 1.2
V1.02	2015/05/28	Specified the condition for the data retention of eFlash

ASIX Electronics Corporation.

4F, No. 8, Hsin Ann Rd., HsinChu Science Park,
HsinChu, Taiwan, R.O.C.

TEL: 886-3-5799500
FAX: 886-3-5799558

Email: support@asix.com.tw
Web: http://www.asix.com.tw