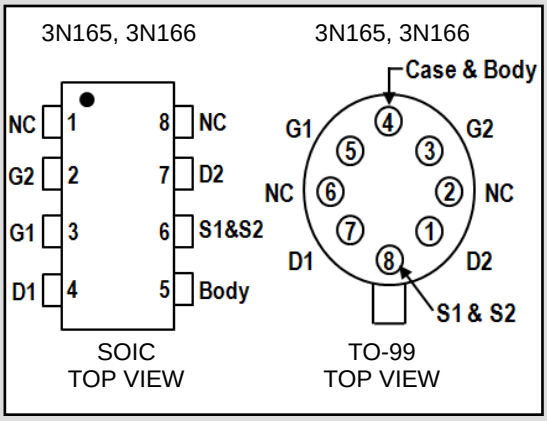
LINEAR SYSTEMS

Twenty-Five Years Of Quality Through Innovation

3N165, 3N166

MONOLITHIC DUAL P-CHANNEL ENHANCEMENT MODE MOSFET

FEATURES	
VERY HIGH INPUT IMPEDANCE	
HIGH GATE BREAKDOWN	
ULTRA LOW LEAKAGE	
LOW CAPACITANCE	
ABSOLUTE MAXIMUM RATINGS (NOTE 1) (T_A=25°C unless otherwise noted)	
Drain-Source or Drain-Gate Voltage **(NOTE 2)**	
3N165	40 V
3N166	30 V
Gate-Gate Voltage	±80 V
Drain Current **(NOTE 2)**	50 mA
Storage Temperature	-55ºC to +150ºC
Operating Temperature	-55ºC to +150ºC
Lead Temperature (Soldering, 10 sec.)	+300ºC
Power Dissipation (One Side)	300 mW
Total Derating above 25ºC	4.2 mW/ºC



ELECTRICAL CHARACTERISTICS (T_A=25°C and V_{BS}=0 unless otherwise noted)

SYMBOL	CHARACTERISTIC	3N165 & 3N166 MIN	3N165 & 3N166 MAX	3N165 & 3N166 MIN	3N165 & 3N166 MAX	UNITS	CONDITIONS
I_{GSSR}	Gate Reverse Leakage Current	--	10	--	100	pA	V_{GS}=40V
I_{GSSF}	Gate Forward Leakage Current	--	-10	--	-100		V_{GS}=-40V
		--	-25	--	--		T_A=+125ºC
I_{DSS}	Drain to Source Leakage Current	--	-200		-200		V_{DS}=-20 V, V_{GS}=V_{BS}=0V
I_{SDS}	Source to Drain Leakage Current	--	-400	--	-400		V_{SD}=-20 V, V_{GD}=V_{DB}=0V
$I_{D(on)}$	On Drain Current	-5	-30	-5	-30	mA	V_{DS}=-15V V_{GS}=-10 V V_{SB}=0V
$V_{GS(th)}$	Gate Source Threshold Voltage	-2	-5	-2	-5	V	V_{DS}=-15V I_D=-10µA V_{SB}=0V
$V_{GS(th)}$	Gate Source Threshold Voltage	-2	-5	-2	-5	V	V_{DS}=V_{GS} I_D=-10µA V_{SB}=0V
$r_{DS(on)}$	Drain Source ON Resistance	--	300	--	300	ohms	V_{GS}=-20V I_D=-100µA V_{SB}=0V
g_{fs}	Forward Transconductance	1500	3000	1500	3000	µS	V_{DS}=-15V I_D=-10mA f=1kHz
g_{os}	Output Admittance	--	300	--	300	µS	V_{SB}=0V
C_{lss}	Input Capacitance	--	3.0	--	3.0	pF	
C_{rss}	Reverse Transfer Capacitance	--	0.7	--	1.0		V_{DS}=-15V I_D=-10mA f=1MHz
C_{oss}	Output Capacitance	--	3.0	--	3.0		**(NOTE 3)** V_{SB}=0V
$R_E(Y_{ls})$	Common Source Forward Transconductance	1200	--			µS	V_{DS}=-15V I_D=-10mA f=100MHz **(NOTE 3)** V_{SB}=0V

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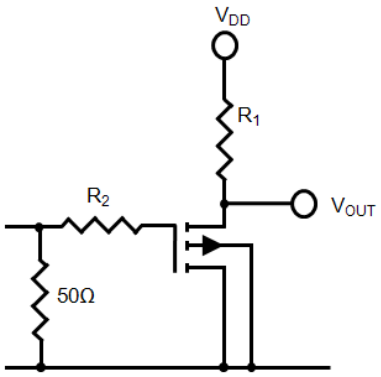
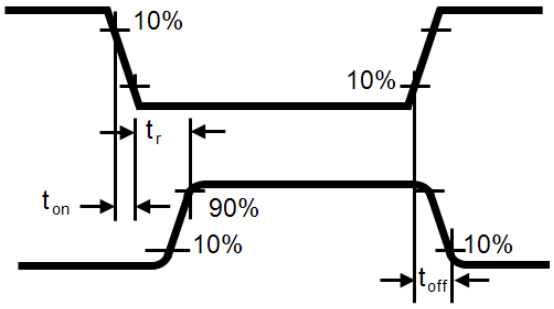
MATCHING CHARACTERISTICS 3N165

SYMBOL	CHARACTERISTIC	LIMITS MIN.	LIMITS MAX.	UNITS	CONDITIONS
G_{fs1}/G_{fs2}	Forward Transconductance Ratio	0.90	1.0		V_{DS}=-15V I_D=-500 µA f=1kHz V_{SB}=0V
V_{GS1-2}	Gate Source Threshold Voltage Differential	--	100	mV	V_{DS}=-15V I_D=-500 µA V_{SB}=0V
$\Delta V_{GS1-2}/\Delta T$	Gate Source Threshold Voltage Differential Change with Temperature	--	100	µV/ºC	V_{DS}=-15V I_D=-500 µA V_{SB}=0V T_A=-55ºC to = +125ºC



TYPICAL SWITCHING WAVEFORM



INPUT PULSE
Rise Time≤2ns
Pulse Width≥200ns

SAMPLING SCOPE
T_r≤0.2ns
C_{IN}≤2pF
R_{IN}≥10M

Typical Switching Time Test Circuit

NOTES:

1. MOS field effect transistors have extremely high input resistance and can be damaged by the accumulation of excess static charge. To avoid possible damage to the device while wiring, testing, or in actual operation, follow these procedures:
   To avoid the build-up of static charge, the leads of the devices should remain shorted together with a metal ring except when being tested or used. Avoid unnecessary handling. Pick up devices by the case instead of the leads. Do not insert or remove devices from circuits with the power on, as transient voltages may cause permanent damage to the devices.
2. Per transistor.
3. For design reference only, not 100% tested.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Linear Integrated Systems (LIS) is a 25-year-old, third-generation precision semiconductor company providing high-quality discrete components. Expertise brought to LIS is based on processes and products developed at Amelco, Union Carbide, Intersil and Micro Power Systems by company President John H. Hall. Hall, a protégé of Silicon Valley legend Dr. Jean Hoerni, was the director of IC Development at Union Carbide, co-founder and vice president of R&D at Intersil, and founder/president of Micro Power Systems.