

LINEAR SYSTEMS

Twenty-Five Years Of Quality Through Innovation

Linear Integrated Systems

SD-SST211/213/215

N-CHANNEL LATERAL
DMOS SWITCH
ZENER PROTECTED

PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DS}$ Min (V)	$V_{(GS)th}$ Max (V)	$r_{DS(on)}$ Max (Ω)	C_{rss} Max (pF)	t_{ON} Max (ns)
SD211DE	30	1.5	45 @ $V_{GS}=10V$	0.5	2
SD213DE	10	1.5	45 @ $V_{GS}=10V$	0.5	2
SD215DE	20	1.5	45 @ $V_{GS}=10V$	0.5	2
SST211	30	1.5	50 @ $V_{GS}=10V$	0.5	2
SST213	10	1.5	50 @ $V_{GS}=10V$	0.5	2
SST215	20	1.5	50 @ $V_{GS}=10V$	0.5	2

Features

- Ultra-High Speed Switching— t_{ON} : 1ns
- Ultra-Low Reverse Capacitance: 0.2pF
- Low Guaranteed r_{DS} @5V
- Low Turn-On Threshold Voltage
- N-Channel Enhancement Mode

Benefits

- High-Speed System Performance
- Low Insertion Loss at High Frequencies
- Low Transfer Signal Loss
- Simple Driver Requirement
- Single Supply Operation

Applications

- Fast Analog Switch
- Fast Sample-and-Holds
- Pixel-Rate Switching
- DAC Deglitchers
- High-Speed Driver

Description

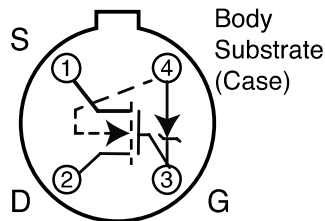
The SD211DE/SST211 series consists of enhancement-mode MOSFETs designed for high speed low-glitch switching in audio, video and high-frequency applications. The SD211 may be used for a ± 5 -V analog switching or as a high speed driver of the SD214. The SD214 is normally used for ± 10 -V analog switching. These MOSFETs utilize lateral construction to achieve low

capacitance and ultra-fast switching speeds. An integrated ZENER diode provides ESD protection. These devices feature a poly-silicon gate for manufacturing reliability.

For similar products see: quad array—SD5000/5400 series, non-Zener protection—SD210DE/214DE.

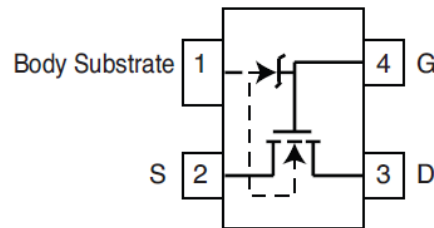
TOP VIEW

SD211DE, SD213DE, SD215DE



TO-206AF
(TO-72)

TO-253 (SOT-143)



TOP VIEW
SST211, SST213, SST215

Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Gate Drain, Gate Source Voltage	(SD211DE/SST211)-30/25V (SD213DE/SST213)-15/25V (SD215DE/SST215)-25/30V	Drain-Substrate Voltage	(SD211DE/SST211)30V (SD213DE/SST213)15V (SD215DE/SST215)25V
Gate-Substrate Voltage ^a	(SD211DE/SST211)-0.3/25V (SD213DE/SST213)-0.3/25V (SD215DE/SST215)-0.3/30V	Source-Substrate Voltage	(SD211DE/SST211)15V (SD213DE/SST213)15V (SD215DE/SST215)25V
Drain-Source Voltage	(SD211DE/SST211)30V (SD213DE/SST213)10V (SD215DE/SST215)20V	Drain Current50mA
Voltage	(SD211DE/SST211)10V (SD213DE/SST213)10V (SD215DE/SST215)20V	Lead Temperature (1/16" from case for 10 seconds)300°C
		Storage Temperature-65 to 150°C
		Operating Junction Temperature-55 to 125°C
		Power Dissipation300mW

Notes:
a. Derate 3mW/°C above 25°C

Specifications^a

PARAMETER	SYMBOL ^b	TEST CONDITIONS ^b	TYP ^b	LIMITS						UNIT	
				211 Series		213 Series		215 Series			
				Min	Max	Min	Max	Min	Max		
Static											
Drain - Source Breakdown Voltage	$V_{(BR)DS}$	$V_{GS} = V_{BS} = 0V, I_D = 10 \mu A$	35	30						V	
		$V_{GS} = V_{BS} = -5V, I_D = 10 nA$	30	10		10		20			
Source - Drain Breakdown Voltage	$V_{(BR)SD}$	$V_{GS} = V_{BD} = -5V, I_S = 10 nA$	22	10		10		20			
Drain - Substrate Breakdown Voltage	$V_{(BR)DBO}$	$V_{GB} = 0V, I_D = 10 nA$ Source Open	35	15		15		25			
Source - Substrate Breakdown Voltage	$V_{(BR)SBO}$	$V_{GB} = 0V, I_S = 10 \mu A$ Drain Open	35	15		15		25			
Drain - Source Leakage	$I_{DS(off)}$	$V_{GS} = V_{BS} = -5V$	$V_{DS} = 10V$	0.4		10		10			nA
			$V_{DS} = 20V$	0.9					10		
Source - Drain Leakage	$I_{SD(off)}$	$V_{GD} = V_{BD} = -5V$	$V_{SD} = 10V$	0.5		10		10			
			$V_{SD} = 20V$						10		
Gate Leakage	I_{GBS}	$V_{DB} = V_{SB} = 0V, V_{GB} = 30V$	0.01		100		100		100		
Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 1 \mu A,$ $V_{SB} = 0V$	0.8	0.5	1.5	0.1	1.5	0.1	1.5	V	
Drain - Source On-Resistance	$r_{DS(on)}$	$V_{SB} = 0V$ $I_D = 1mA$	$V_{GS} = 5V$ (SD Series)	58		70		70		70	Ω
			$V_{GS} = 5V$ (SST Series)	60		75		75		75	
			$V_{GS} = 10V$ (SD Series)	38		45		45		45	
			$V_{GS} = 10V$ (SST Series)	40		50		50		50	
			$V_{GS} = 15V$	30							
			$V_{GS} = 20V$	26							
			$V_{GS} = 25V$	24							

Specifications^a

PARAMETER	SYMBOL ^b	TEST CONDITIONS ^b	TYP ^c	LIMITS						UNIT	
				211 Series		213 Series		215 Series			
				Min	Max	Min	Max				
Dynamic											
Forward Transconductance	g_{fs}	$V_{DS} = 10V, V_{SB} = 0V, I_D = 20mA, f = 1kHz$	SD Series	11	10		10		10		mS
	g_{os}		SST Series	10.5	9		9		9		
			All	0.9							
Gate Node Capacitance	$C_{(GS+GD+GB)}$	$V_{DS} = 10V, f = 1MHz, V_{GS} = V_{BS} = -15V$	SD Series	2.5		3.5		3.5		3.5	pF
Drain Node Capacitance	$C_{(GD+DB)}$			1.1		1.5		1.5		1.5	
Source Node Capacitance	$C_{(GS+SB)}$		3.7		5.5		5.5		5.5		
Reverse Transfer Capacitance	C_{rss}		SST Series	4.2							
			SD Series	0.2		0.5		0.5		0.5	
Switching											
Turn-On Time	$t_{D(on)}$	SD Series Only $V_{SB} = 0V, V_{IN} 0 \text{ to } 5V, R_G = 25\Omega, V_{DD} = 5V, R_L = 680\Omega$	0.5		1		1		1	ns	
	t_r		0.6		1		1		1		
Turn-Off Time	$t_{D(off)}$		2								
	t_f		6								

Notes:

- $T_A = 25^\circ C$ unless otherwise notes.
- B is the body (substrate) and $V_{(BR)}$ is breakdown voltage.
- Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

Linear Integrated Systems (LIS) is a 25-year-old, third-generation precision semiconductor company providing high-quality discrete components. Expertise brought to LIS is based on processes and products developed at Amelco, Union Carbide, Intersil and Micro Power Systems by company President John H. Hall. Hall, a protégé of Silicon Valley legend Dr. Jean Hoerni, was the director of IC Development at Union Carbide, co-founder and vice president of R&D at Intersil, and founder/president of Micro Power Systems.