Am27C040

4 Megabit (524,288 x 8-Bit) CMOS EPROM

**Advanced
Micro
Devices**

DISTINCTIVE CHARACTERISTICS

- **Fast access time**
  - 100 ns
- **Low power consumption**
  - 100 µA maximum CMOS standby current
- **JEDEC-approved pinout**
  - Plug in upgrade of 1 Mbit EPROM and 2 Mbit EPROMs
  - Easy upgrade from 28-pin JEDEC EPROMs
- **Single +5 V power supply**
- **±10% power supply tolerance standard on most speeds**

- **100% Flashrite™ programming**
  - Typical programming time of 1 minute
- **Latch-up protected to 100 mA from –1 V to Vcc + 1 V**
- **High noise immunity**
- **Compact 32-pin DIP, PDIP, LCC and PLCC packages require no hardware change for upgrades to 8 Mbits**
- **DESC SMD No. 5962-91752**

GENERAL DESCRIPTION

The Am27C040 is a 4 Mbit ultraviolet erasable programmable read-only memory. It is organized as 512K words by 8 bits per word, operates from a single +5 V supply, has a static standby mode, and features fast single address location programming. Products are available in windowed ceramic DIP and LCC packages, as well as plastic one-time programmable (OTP) packages.

Typically, any byte can be accessed in less than 100 ns, allowing operation with high-performance microprocessors without any WAIT states. The Am27C040 offers separate Output Enable ($\overline{OE}$) and Chip Enable ($\overline{CE}$)

controls, thus eliminating bus contention in a multiple bus microprocessor system.

AMD's CMOS process technology provides high speed, low power, and high noise immunity. Typical power consumption is only 100 mW in active mode, and 100 µW in standby mode.

All signals are TTL levels, including programming signals. Bit locations may be programmed singly, in blocks, or at random. The Am27C040 supports AMD's Flashrite programming algorithm (100 µs pulses) resulting in typical programming time of 1 minute.
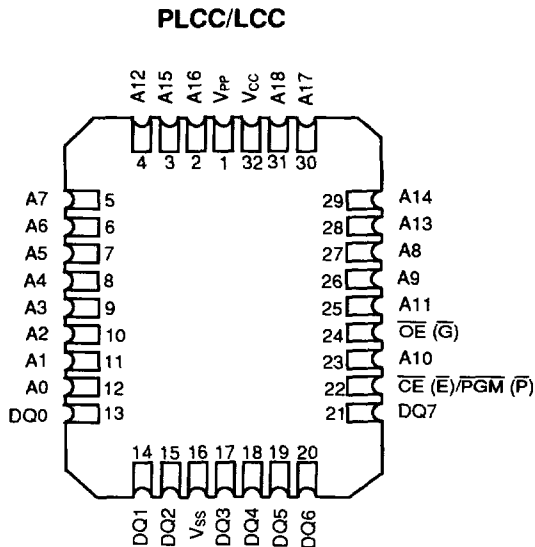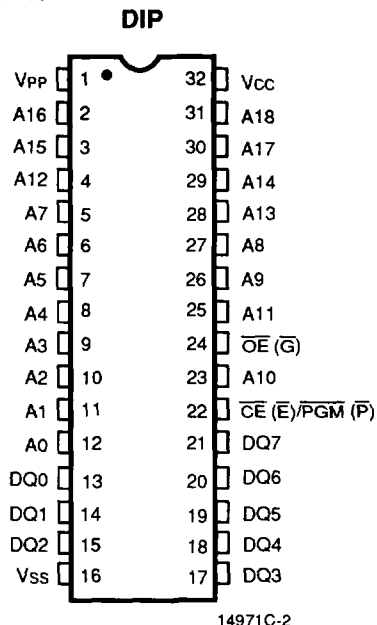
BLOCK DIAGRAM
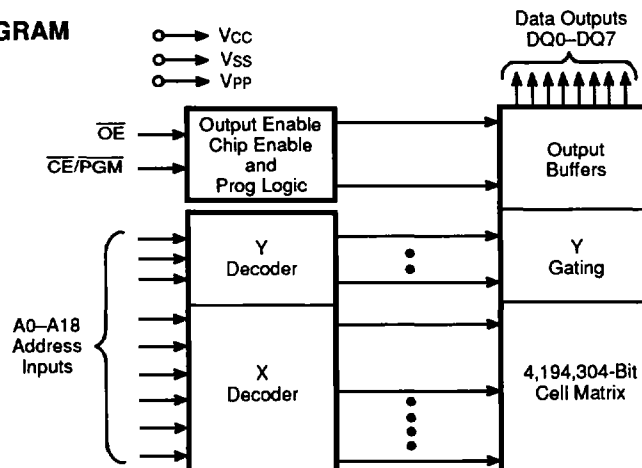
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PRODUCT SELECTOR GUIDE

Family Part No.	Am27C040			
Ordering Part No:				
Vcc ±5%	-105	-125		
Vcc ±10%	-100	-120	-150	-200
Max Access Time (ns)	100	120	150	200
$\overline{CE}$ (E) Access (ns)	100	120	150	200
$\overline{OE}$ (G) Access (ns)	40	50	65	75

CONNECTION DIAGRAMS
Top View

DIP

PLCC/LCC

```
VPP    1 ●    32   Vcc
A16    2      31   A18
A15    3      30   A17
A12    4      29   A14
A7     5      28   A13
A6     6      27   A8
A5     7      26   A9
A4     8      25   A11
A3     9      24   OE (G)
A2    10      23   A10
A1    11      22   CE (E)/PGM (P)
A0    12      21   DQ7
DQ0   13      20   DQ6
DQ1   14      19   DQ5
DQ2   15      18   DQ4
Vss   16      17   DQ3
```

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```
          A12 A15 A16 VPP Vcc A18 A17
           4   3   2   1  32  31  30

A7  ] 5                         29 [ A14
A6  ] 6                         28 [ A13
A5  ] 7                         27 [ A8
A4  ] 8                         26 [ A9
A3  ] 9                         25 [ A11
A2  ] 10                        24 [ OE (G)
A1  ] 11                        23 [ A10
A0  ] 12                        22 [ CE (E)/PGM (P)
DQ0 ] 13                        21 [ DQ7

          14  15  16  17  18  19  20
         DQ1 DQ2 Vss DQ3 DQ4 DQ5 DQ6
```
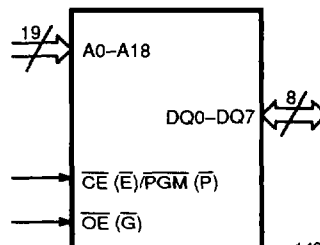
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Notes:
1. JEDEC nomenclature is in parentheses.
2. The 32-pin DIP to 32-pin LCC configuration varies from the JEDEC 28-pin DIP to 32-pin LCC configuration.

PIN DESIGNATIONS

A0–A18	=	Address Inputs
$\overline{CE}$ (E)/$\overline{PGM}$ (P)	=	Chip Enable Input
DQ0–DQ7	=	Data Input/Outputs
$\overline{OE}$ (G)	=	Output Enable Input
Vcc	=	Vcc Supply Voltage
VPP	=	Program Supply Voltage
Vss	=	Ground

LOGIC SYMBOL

```
  19 /          ┌──────────┐
 ──/──▶│ A0–A18              │
       │                     │
       │          DQ0–DQ7 ◀═══▶ 8 /
       │                     │
  ─────▶│ CE (E)/PGM (P)      │
       │                     │
  ─────▶│ OE (G)              │
       └──────────┘
```
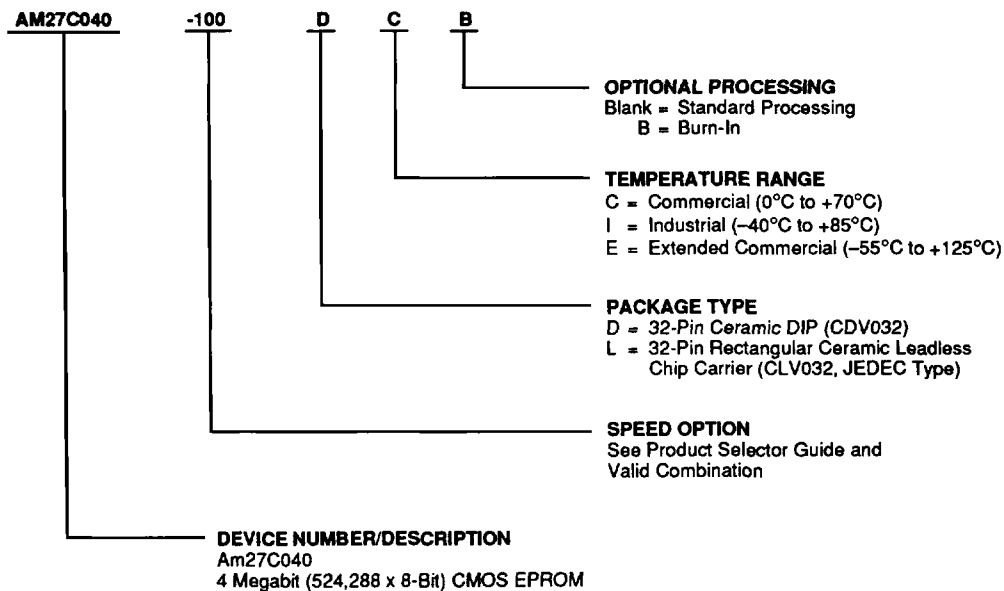
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ORDERING INFORMATION

EPROM Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

AM27C040	-100	D	C	B

OPTIONAL PROCESSING
Blank = Standard Processing
B = Burn-In

TEMPERATURE RANGE
C = Commercial (0°C to +70°C)
I = Industrial (–40°C to +85°C)
E = Extended Commercial (–55°C to +125°C)

PACKAGE TYPE
D = 32-Pin Ceramic DIP (CDV032)
L = 32-Pin Rectangular Ceramic Leadless Chip Carrier (CLV032, JEDEC Type)

SPEED OPTION
See Product Selector Guide and Valid Combination

DEVICE NUMBER/DESCRIPTION
Am27C040
4 Megabit (524,288 x 8-Bit) CMOS EPROM

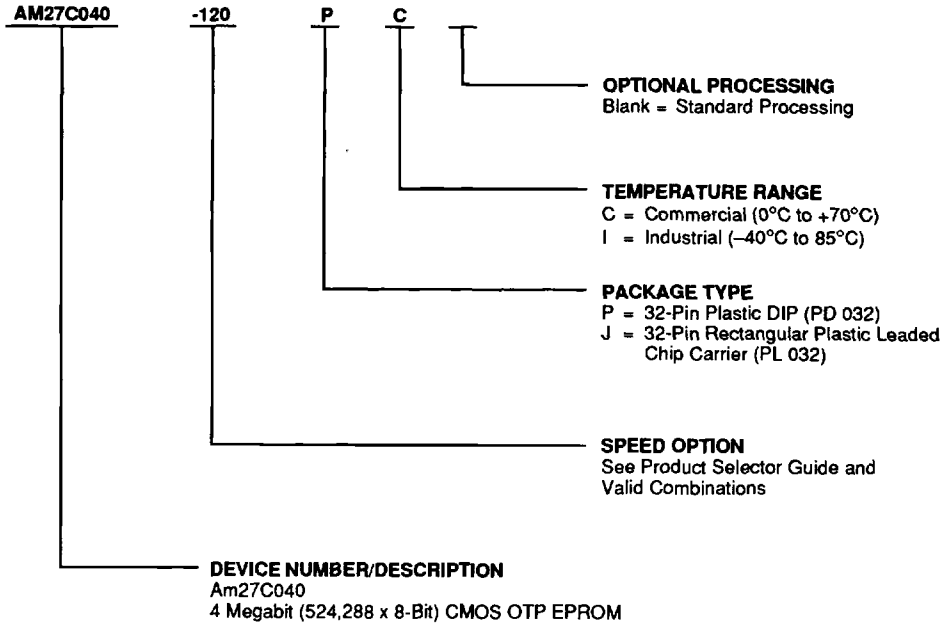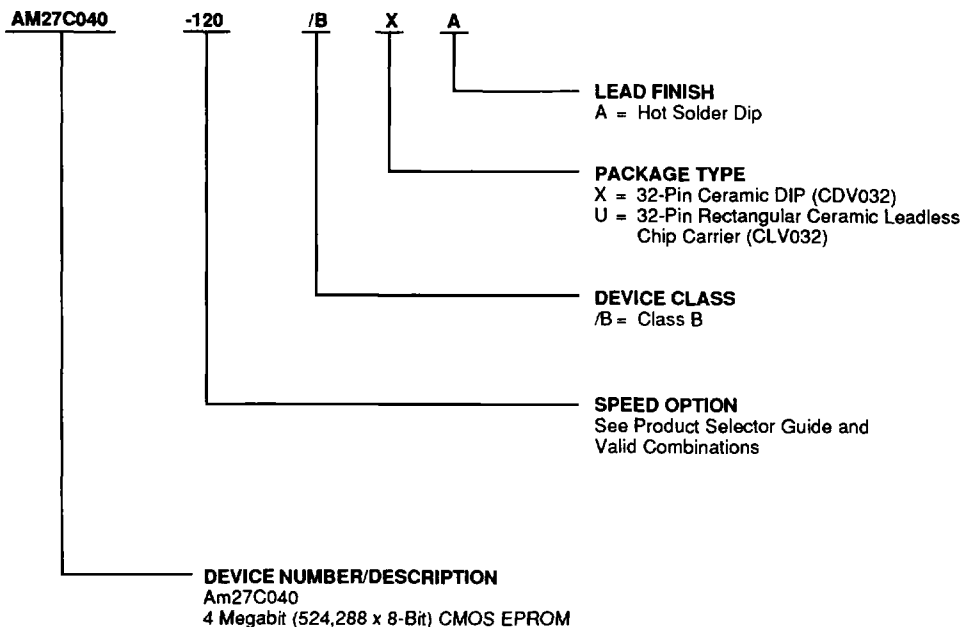| Valid Combinations	
AM27C040-100	DC, DCB, LC, LCB
AM27C040-105	DC, DCB, DI, DIB, LC, LCB, LI, LIB
AM27C040-120	
AM27C040-125	
AM27C040-150	DC, DCB, DE, DEB, DI, DIB, LC, LCB, LI, LIB, LE, LEB
AM27C040-200	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

ORDERING INFORMATION

OTP Products (Preliminary)

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

```
AM27C040        -120      P     C
```

OPTIONAL PROCESSING
Blank = Standard Processing

TEMPERATURE RANGE
C = Commercial (0°C to +70°C)
I = Industrial (–40°C to 85°C)

PACKAGE TYPE
P = 32-Pin Plastic DIP (PD 032)
J = 32-Pin Rectangular Plastic Leaded
        Chip Carrier (PL 032)

SPEED OPTION
See Product Selector Guide and
Valid Combinations

DEVICE NUMBER/DESCRIPTION
Am27C040
4 Megabit (524,288 x 8-Bit) CMOS OTP EPROM

Valid Combinations	
AM27C040-100	
AM27C040-105	
AM27C040-120	PC, JC, PI, JI
AM27C040-125	
AM27C040-150	
AM27C040-200	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

MILITARY ORDERING INFORMATION

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883 requirements. The order number (Valid Combination) is formed by a combination of:

```
AM27C040        -120      /B      X      A
```

LEAD FINISH
A = Hot Solder Dip

PACKAGE TYPE
X = 32-Pin Ceramic DIP (CDV032)
U = 32-Pin Rectangular Ceramic Leadless
        Chip Carrier (CLV032)

DEVICE CLASS
/B = Class B

SPEED OPTION
See Product Selector Guide and
Valid Combinations

DEVICE NUMBER/DESCRIPTION
Am27C040
4 Megabit (524,288 x 8-Bit) CMOS EPROM

Valid Combinations	
AM27C040-120	
AM27C040-150	/BXA, /BUA
AM27C040-200	
AM27C040-250	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

Group A Tests

Group A tests consist of Subgroups
1, 2, 3, 7, 8, 9, 10, 11.

FUNCTIONAL DESCRIPTION

Erasing the Am27C040

In order to clear all locations of their programmed contents, it is necessary to expose the Am27C040 to an ultraviolet light source. A dosage of 15 W seconds/cm² is required to completely erase an Am27C040. This dosage can be obtained by exposure to an ultraviolet lamp —wavelength of 2537 Å— with intensity of 12,000 µW/cm² for 15 to 20 minutes. The Am27C040 should be directly under and about one inch from the source and all filters should be removed from the UV light source prior to erasure.

It is important to note that the Am27C040, and similar devices, will erase with light sources having wavelengths shorter than 4000 Å. Although erasure times will be much longer than with UV sources at 2537Å, nevertheless the exposure to fluorescent light and sunlight will eventually erase the Am27C040 and exposure to them should be prevented to realize maximum system reliability. If used in such an environment, the package window should be covered by an opaque label or substance.

Programming the Am27C040

Upon delivery, or after each erasure, the Am27C040 has all 4,194,304 bits in the "ONE", or HIGH state. "ZEROs" are loaded into the Am27C040 through the procedure of programming.

The programming mode is entered when 12.75 V ± 0.25 V is applied to the V$_{PP}$ pin, $\overline{CE/PGM}$ is at V$_{IL}$ and $\overline{OE}$ is at V$_{IH}$.

For programming, the data to be programmed is applied 8 bits in parallel to the data output pins.

The Flashrite algorithm reduces programming time by using 100 µs programming pulse and by giving each address only as many pulses as are necessary in order to reliably program the data. After each pulse is applied to a given address, the data in that address is verified. If the data does not verify, additional pulses are given until it verifies or the maximum is reached. This process is repeated while sequencing through each address of the Am27C040. This part of the algorithm is done at V$_{CC}$ = 6.25 V to assure that each EPROM bit is programmed to a sufficiently high threshold voltage. After the final address is completed, the entire EPROM memory is verified at V$_{CC}$ = V$_{PP}$ = 5.25 V.

Please refer to Section 6 for programming flow chart and characteristics.

Program Inhibit

Programming of multiple Am27C040s in parallel with different data is also easily accomplished. Except for $\overline{CE/PGM}$, all like inputs of the parallel Am27C040 may be common. A TTL low-level program pulse applied to an Am27C040 $\overline{CE/PGM}$ input with V$_{PP}$ = 12.75 V ± 0.25 V, and $\overline{OE}$ HIGH will program that Am27C040. A high-level $\overline{CE/PGM}$ input inhibits the other Am27C040s from being programmed.

Program Verify

A verify should be performed on the programmed bits to determine that they were correctly programmed. The verify should be performed with $\overline{OE}$ and $\overline{CE/PGM}$ at V$_{IL}$, and V$_{PP}$ between 12.5 V and 13.0 V.

Auto Select Mode

The auto select mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the Am27C040.

To activate this mode, the programming equipment must force 12.0 V ± 0.5 V on address line A9 of the Am27C040. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from V$_{IL}$ to V$_{IH}$. All other address lines must be held at V$_{IL}$ during auto select mode.

Byte 0 (A0 = V$_{IL}$) represents the manufacturer code, and Byte 1 (A0 = V$_{IH}$), the device identifier code. For the Am27C040, these two identifier bytes are given in the Mode Select table. All identifiers for manufacturer and device codes will possess odd parity, with the MSB (DQ7) defined as the parity bit.

Read Mode

The Am27C040 has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{CE/PGM}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t$_{ACC}$) is equal to the delay from $\overline{CE/PGM}$ to output (t$_{CE}$). Data is available at the outputs t$_{OE}$ after the falling edge of $\overline{OE}$, assuming that $\overline{CE/PGM}$ has been LOW and addresses have been stable for at least t$_{ACC}$ − t$_{OE}$.

Standby Mode

The Am27C040 has a CMOS standby mode which reduces the maximum V_{CC} current to 100 µA. It is placed in CMOS-standby when $\overline{CE/PGM}$ is at $V_{CC} \pm 0.3$ V. The Am27C040 also has a TTL-standby mode which reduces the maximum V_{CC} current to 1.0 mA. It is placed in TTL-standby when $\overline{CE/PGM}$ is at V_{IH}. When in standby mode, the outputs are in a high-impedance state, independent of the $\overline{OE}$ input.

Output OR-Tieing

To accommodate multiple memory connections, a two-line control function is provided to allow for:

■ Low memory power dissipation

■ Assurance that output bus contention will not occur

It is recommended that $\overline{CE/PGM}$ be decoded and used as the primary device-selecting function, while $\overline{OE}$ be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low-power standby mode and that the outut pins are only active when data is desired from a particular memory device.

System Applications

During the switch between active and standby conditions, transient current peaks are produced on the rising and falling edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. At a minimum, a 0.1 µF ceramic capacitor (high frequency, low inherent inductance) should be used on each device between V_{CC} and V_{SS} to minimize transient effects. In addition, to overcome the voltage drop caused by the inductive effects of the printed circuit board traces on EPROM arrays, a 4.7 µF bulk electrolytic capacitor should be used between V_{CC} and V_{SS} for each eight devices. The location of the capacitor should be close to where the power supply is connected to the array.

MODE SELECT TABLE

Mode	Pins	$\overline{CE/PGM}$	$\overline{OE}$	A0	A9	V_{PP}	Outputs
Read		V_{IL}	V_{IL}	X	X	X	D_{OUT}
Output Disable		V_{IL}	V_{IH}	X	X	X	High Z
Standby (TTL)		V_{IH}	X	X	X	X	High Z
Standby (CMOS)		$V_{CC} \pm 0.3$ V	X	X	X	X	High Z
Program		V_{IL}	V_{IH}	X	X	V_{PP}	D_{IN}
Program Verify		V_{IL}	V_{IL}	X	X	V_{PP}	D_{OUT}
Program Inhibit		V_{IH}	X	X	X	V_{PP}	High Z
Auto Select (Note 3)	Manufacturer Code	V_{IL}	V_{IL}	V_{IL}	V_H	X	01H
	Device Code	V_{IL}	V_{IL}	V_{IH}	V_H	X	9BH

Notes:

1. $V_H = 12.0$ V ± 0.5 V

2. X can be either V_{IL} or V_{IH}

3. A1–A8 = A10–A18 = V_{IL}

ABSOLUTE MAXIMUM RATINGS

Storage Temperature:
OTP Products . . . . −65°C to +125°C
All Other Products . . . . −65°C to +150°C

Ambient Temperature
with Power Applied . . . . −55°C to +125°C

Voltage with Respect to V_{SS}:
All pins except A9, V_{PP}, and
Vcc (Note 1) . . . . −0.6 V to Vcc + 0.6 V

A9 and V_{PP} (Note 2) . . . . −0.6 V to 13.5 V

Vcc . . . . −0.6 V to 7.0 V

Notes:

1. *During transitions, the input may overshoot V_{SS} to −2.0 V for periods of up to 20 ns. Maximum DC voltage on input and I/O may overshoot to V_{CC} + 2.0 V for periods of up to 20 ns.*

2. *During transitions, A9 and V_{PP} may overshoot V_{SS} to −2.0 V for periods of up to 20 ns. A9 and V_{PP} must not exceed 13.5 V for any period of time.*

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Case Temperature (Tc) . . . . 0°C to +70°C

Industrial (I) Devices

Case Temperature (Tc) . . . . −40°C to +85°C

Extended Commercial (E) Devices

Case Temperature (Tc) . . . . −55°C to +125°C

Military (M) Devices

Case Temperature (Tc) . . . . −55°C to +125°C

Supply Read Voltages:

Vcc for Am27C040-XX5 . . . . . +4.75 V to +5.25 V
Vcc for Am27C040-XX0 . . . . . +4.50 V to +5.50 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating ranges unless otherwise specified (Notes 1, 3 and 4) (for APL products, Group A, Subgroups 1, 2, 3, 6 and 7 are tested unless otherwise noted)

Parameter Symbol	Parameter Description	Test Conditions		Min	Max	Unit
V_{OH}	Output HIGH Voltage	$I_{OH} = -400 \mu A$		2.4		V
V_{OL}	Output LOW Voltage	$I_{OL} = 2.1$ mA			0.45	V
V_{IH}	Input HIGH Voltage			2.0	$V_{CC} + 0.5$	V
V_{IL}	Input LOW Voltage			−0.5	+0.8	V
I_{LI}	Input Load Current	$V_{IN} = 0$ V to V_{CC}	C/I Devices		1.0	μA
			E/M Devices		5.0	
I_{LO}	Output Leakage Current	$V_{OUT} = 0$ V to V_{CC}	C/I Devices		5.0	μA
			E/M Devices		10.0	
I_{CC1}	V_{CC} Active Current (Note 3)	$\overline{CE} = V_{IL}$, f = 5 MHz, $I_{OUT} = 0$ mA	C/I Devices		40	mA
			E/M Devices		60	
I_{CC2}	V_{CC} TTL Standby Current	$\overline{CE} = V_{IH}$			1.0	mA
I_{CC3}	V_{CC} CMOS Standby Current	$\overline{CE} = V_{CC} \pm 0.3$ V			100	μA
I_{PP1}	V_{PP} Current During Read	$\overline{CE} = \overline{OE} = V_{IL}$, $V_{PP} = V_{CC}$			100	μA

Notes:

1. V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.

2. **Caution:** The Am27C040 must not be removed from (or inserted into) a socket when V_{CC} or V_{PP} is applied.

3. I_{CC1} is tested with $\overline{OE}/V_{PP} = V_{IH}$ to simulate open outputs.

4. Minimum DC Input Voltage is −0.5 V. During transitions, the inputs may overshoot to −2.0 V for periods less than 20 ns. Maximum DC Voltage on output pins is $V_{CC} + 0.5$ V, which may overshoot to $V_{CC} + 2.0$ V for periods less than 20 ns.
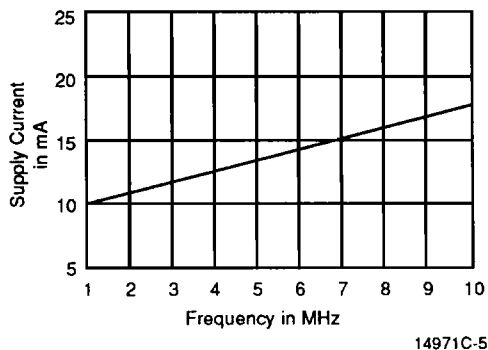

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Figure 1. Typical Supply Current vs. Frequency
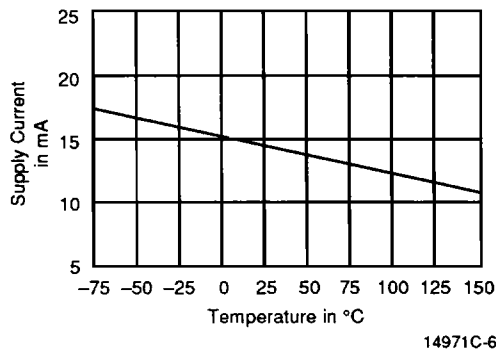$V_{CC} = 5.0$ V, T = 25°C

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Figure 2. Typical Supply Current vs. Temperature
$V_{CC} = 5.5$ V, f = 5 MHz

CAPACITANCE

Parameter Symbol	Parameter Description	Test Conditions	CDV032		CLV032		PD 032		PL 032		Unit
			Typ	Max	Typ	Max	Typ	Max	Typ	Max	
C$_{IN}$	Input Capacitance	V$_{IN}$ = 0 V	10	12	8	10	10	12	8	10	pF
C$_{OUT}$	Output Capacitance	V$_{OUT}$ = 0 V	12	15	9	12	12	15	9	12	pF

Notes:

1. This parameter is only sampled and not 100% tested.

2. T$_A$ = +25°C, f = 1 MHz.

SWITCHING CHARACTERISTICS over operating ranges unless otherwise specified (Notes 1, 3 and 4) (for APL products, Group A, Subgroups 9, 10 and 11 are tested unless otherwise noted)

Parameter Symbols		Parameter Description	Test Conditions		Am27C040					Unit
JEDEC	Standard				-105 -100	-125 -120	-150	-200	-255 -250	
t$_{AVQV}$	t$_{ACC}$	Address to Output Delay	$\overline{CE}$ = $\overline{OE}$ = V$_{IL}$	Min						ns
				Max	100	120	150	200	250	
t$_{ELQV}$	t$_{CE}$	Chip Enable to Output Delay	$\overline{OE}$ = V$_{IL}$	Min						ns
				Max	100	120	150	200	250	
t$_{GLQV}$	t$_{OE}$	Output Enable to Output Delay	$\overline{CE}$ = V$_{IL}$	Min						ns
				Max	40	50	55	60	60	
t$_{EHQZ}$ t$_{GHQZ}$	t$_{DF}$ (Note 2)	Chip Enable HIGH or Output Enable HIGH, whichever comes first, to Output Float		Min	0	0	0	0	0	ns
				Max	30	30	30	40	60	
t$_{AXQX}$	t$_{OH}$	Output Hold from Addresses, $\overline{CE}$, or $\overline{OE}$, whichever occurred first		Min	0	0	0	0	0	ns
				Max						

Notes:

1. V$_{CC}$ must be applied simultaneously or before V$_{PP}$, and removed simultaneously or after V$_{PP}$.

2. This parameter is only sampled and not 100% tested.

3. **Caution:** The Am27C040 must not be removed from, or inserted into a socket or board when V$_{PP}$ or V$_{CC}$ is applied.

4. Output Load: 1 TTL gate and C$_L$ = 100 pF,
   Input Rise and Fall Times: 20 ns,
   Input Pulse Levels: 0.45 V to 2.4 V,
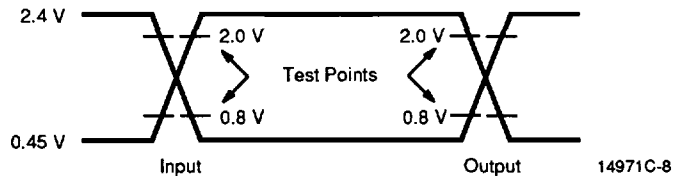   Timing Measurement Reference Level—Inputs: 0.8 V and 2 V,
   Outputs: 0.8 V and 2 V
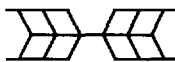
SWITCHING TEST CIRCUIT
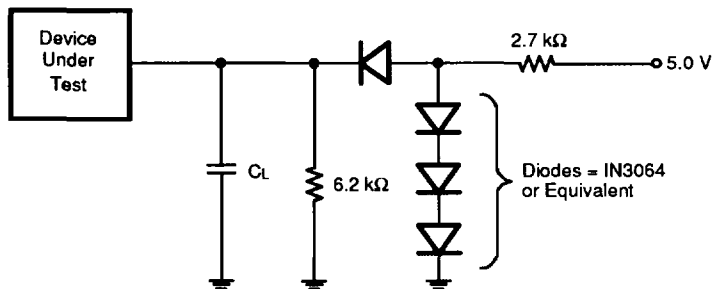
14971C-7

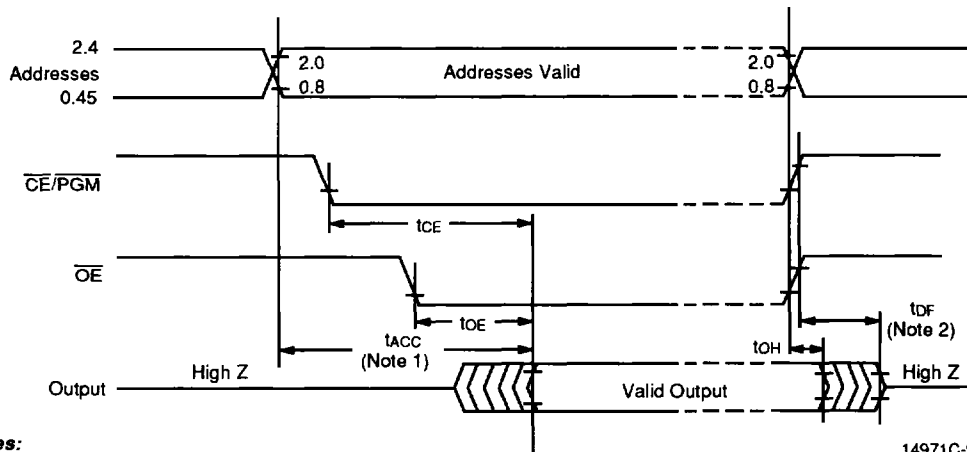$C_L = 100$ pF including jig capacitance

SWITCHING TEST WAVEFORM

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AC Testing: Inputs are driven at 2.4 V for a Logic "1" and 0.45 V for a Logic "0." Input pulse rise and fall times are ≤ 20 ns.

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must Be Steady	Will Be Steady
	May Change from H to L	Will Be Changing from H to L
	May Change from L to H	Will Be Changing from L to H
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High Impedance "Off" State

KS000010

SWITCHING WAVEFORM

2.4
Addresses
0.45

2.0
0.8
Addresses Valid
2.0
0.8

$\overline{CE/PGM}$

t_{CE}

$\overline{OE}$

t_{OE}

t_{DF} (Note 2)

t_{ACC} (Note 1)

t_{OH}

High Z

Output

High Z

Valid Output

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Notes:

1. $\overline{OE}$ may be delayed up to t_{ACC} – t_{OE} after the falling edge of the addresses without impact on t_{ACC}.

2. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.