Am29540

Programmable FFT Address Sequencer

DISTINCTIVE CHARACTERISTICS

- Generates data and coefficient addresses
- Programmable transform length 2 to 65,536 points
- Radix-2 or Radix-4
- In-place or non-in-place transformation
- Decimation in frequency (DIF) or decimation in time (DIT) FFT algorithms supported
- 40-pin DIP package, 5 volt single supply

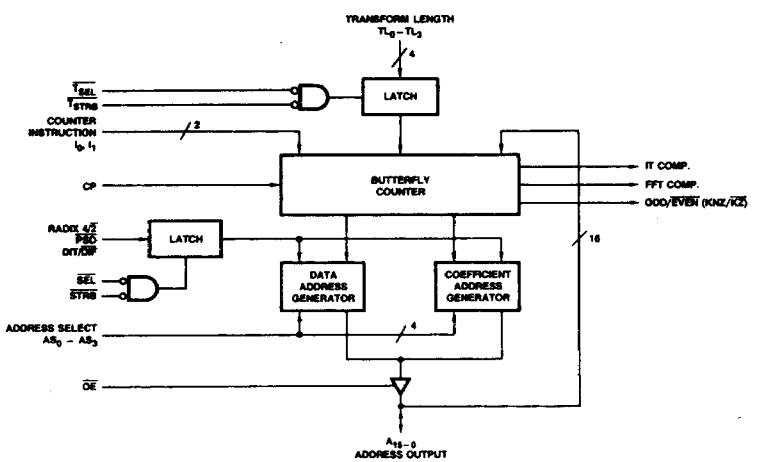
GENERAL DESCRIPTION

The Am29540 Fast Fourier Transform Address Sequencer generates all the data (RAM) and coefficient (ROM) addresses necessary to perform the repetitive butterfly operations of the FFT. Decimation in time and decimation in frequency algorithms are supported (control DIT/$\overline{\text{DIF}}$) in radix-2 or radix-4 (RADIX 4/$\overline{2}$). A radix-2 real valued input (RVI) transform is also supported. For radix-2 operation the transform length is programmable in powers of 2 from 2 to 65,536 points. In radix-4 the range is 4 to 65,536 in powers of 4.

Address sequences can be selected to be compatible with data which may or may not have been pre-scrambled ('bit-reversed'). If the data has been pre-scrambled the control $\overline{\text{PSD}}$ must be LOW to select the correct sequence. If the data is not pre-scrambled ($\overline{\text{PSD}}$ HIGH) and an in-place transform is performed, the output data will necessarily be in bit-reversed order. If this is not desirable, alternate addresses are available for a non-in-place, non-bit-reversing algorithm.

The butterfly counter operates on the positive clock edge and responds to four instructions. COUNT causes the counter to increment to the next butterfly. RESET causes the counter to initialize for the specified transform length. RESET/LOAD causes the counter to initialize and a data address offset to be loaded into the part via the bi-directional 3-state ADDRESS port. This offset is effectively OR-ed onto the higher significant bits of the address which are unused for the selected transform length. A HOLD instruction is also provided. Three status lines are provided. ODD/$\overline{\text{EVEN}}$ (KNZ/$\overline{\text{KZ}}$) controls the alternation of read and write memories for non-in-place transforms and determines the butterfly structure in the RVI transform. The flag has the function KNZ/$\overline{\text{KZ}}$ when RVI data addresses are selected (AS = 12 to 15). Iteration complete (IT COMP) flags the bottom of a "column" of butterflies and is used in conjunction with block floating point schemes. FFT COMP identifies the last butterfly of the transform.

BLOCK DIAGRAM



BDR02240

FFT Address Sequencer

03567C

Refer to Page 13-1 for Essential Information on Military Devices

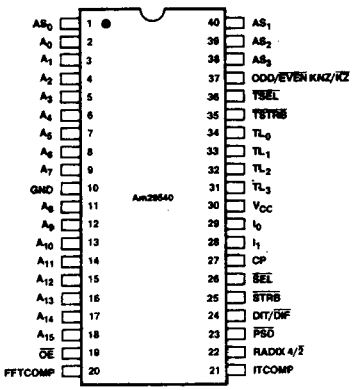
RELATED PRODUCTS

Part No.	Description
Am29501	Multi-port pipelined processor (Byte-slice™)
Am29516/17	16 x 16 parallel multiplier
Am29520/21	Multilevel pipeline register
Am29526/ 27/28/29	High speed sine/cosine generators
Am29825	High performance 8-bit register

Byte-Slice is a trademark of Advanced Micro Devices, Inc.

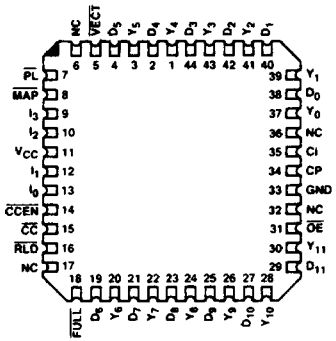
CONNECTION DIAGRAM
Top View

D-40-1



CDR04360

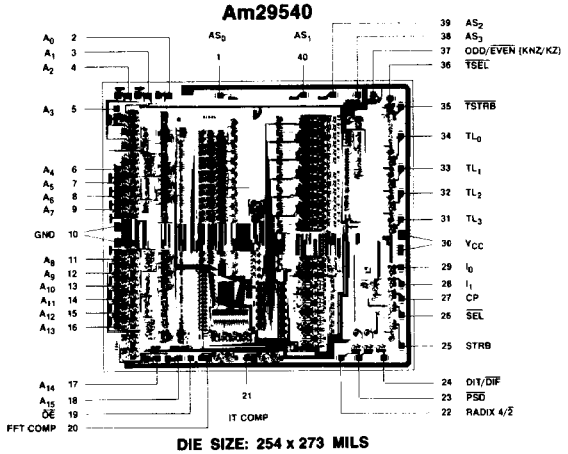
L-44-1



CD004690

Note: Pin 1 is marked for orientation

METALLIZATION AND PAD LAYOUT
Am29540



DIE SIZE: 254 x 273 MILS

ORDERING INFORMATION

AMD products are available in several packages and operating ranges. The order number is formed by a combination of the following: Device number, speed option (if applicable), package type, operating range and screening option (if desired).

Am29540 **P** **C** **B**

- **B** — Screening Option
  - Blank – Standard Processing
  - B – Burn-in
- **C** — Temperature (see Operating Range)
  - C – Commercial (0 to +70°C)
  - M – Military (–55 to +125°C)
- **P** — Package
  - D– 40 pin CERDIP
  - L– 44 pin Leadless Chip Carrier
  - X– Dice
- **Am29540** — Device Type
  - Programmable FFT Address Sequencer

Valid Combinations	
Am29540	DC, DCB, DMB LC, LMB

Valid Combinations

Consult the AMD sales office in your area to determine if a device is currently available in the combination you wish.

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Refer to Page 13-1 for Essential Information on Military Devices

PIN DESCRIPTION

*Pin No.	Name	I/O	Description
31-34	TL_3, TL_2 TL_1, TL_0	I	Transform length control determines the number of points to be transformed. (See Figure 1.)
36, 35	$\overline{TSEL}$, $\overline{TSTRB}$	I	Transform length latch enables. These active LOW inputs are ANDed to control the latch. The latch is transparent when both $\overline{TSEL}$ and $\overline{TSTRB}$ are LOW.
29, 28	I_0, I_1	I	Counter Instruction inputs determine one of four available butterfly counter instructions: Hold, Reset, Reset/Load and Count. (See Figure 2.)
27	CP	I	Butterfly counter clock (positive edge active).
22	Radix 4/$\overline{2}$	I	The Radix control determines whether addresses will be generated for Radix-4 (HIGH) for Radix-2 (LOW) transforms.
23	$\overline{PSD}$	I	The Pre-Scrambled Data, $\overline{PSD}$, input is used to select an appropriate transform for input data which has previously been digit reversed. Refer to individual transform flow charts for other cases.
24	DIT/$\overline{DIF}$	I	Control input for selection of the Decimation in Frequency algorithm (LOW) or Decimation In Time algorithm (HIGH).
26, 25	$\overline{SEL}$, $\overline{STRB}$	I	Transform type (Radix 4/$\overline{2}$, PSD, DIF/$\overline{T}$) latch enables. These active LOW inputs are ANDed to control the latch. The latch is transparent when both $\overline{SEL}$ and $\overline{STRB}$ are LOW.
1, 38-40	AS_3, AS_2, AS_1, AS_0	I	Address Select control determines address selection. (See Figure 3.)
19	$\overline{OE}$	I	Three-state output enable. The 3-state output is controlled solely by $\overline{OE}$. The output does not automatically become high impedance during the Reset/Load instruction.
2-9, 11-18	A_{15}-A_0 Address Output (offset input)	I/O	Bidirectional 16-bit port to output selected addresses or to input an address offset.
37	ODD/$\overline{EVEN}$, (KNZ/$\overline{KZ}$)	O	For address select 0 to 11 the ODD/$\overline{EVEN}$ output controls the alternation of separate read and write memories for non-in-place transforms. For Address select 12 to 15 KNZ/$\overline{KZ}$ = (LOW) indicates that the rotational constant to be used in the RVI transform is W^0 and that an alternative butterfly must be implemented.
20	FFT COMP	O	FFT Complete = HIGH identifies the last butterfly (or end) of the transform. (See Figure 4.)
21	IT COMP	O	Iteration Complete = HIGH flags the bottom of a 'column' of butterflies. (See Figure 4.)

*DIP Configuration

DETAILED DESCRIPTION

The Am29540 can be pictured as consisting of sixteen 16-bit counters that output on a bidirectional three-state address port, A_{15}–A_0. These sixteen counters generate the data and coefficient addresses required to support the various FFT algorithms.

Decimation-In-Time (DIT) and Decimation-In-Frequency (DIF) algorithms are supported in Radix-2 and Radix-4. Two inputs, DIT/$\overline{DIF}$ and Radix4/$\overline{2}$, control these two parameters without encoding. A third microcode bit, $\overline{PSD}$, enables input data to be bit reversed. $\overline{PSD}$ must be LOW for all transforms with prescrambled (bit reversed) input data. For all in-place transforms with normally-ordered input data, $\overline{PSD}$ must be HIGH. For all non-in-place DIT transforms, $\overline{PSD}$ must be LOW, and for all non-in-place DIF transforms, $\overline{PSD}$ must be HIGH. These three microcode bits can be latched. $\overline{STRB}$ and $\overline{SEL}$ are the latch enables. They are ANDed so that the latch is transparent when both are LOW.

The transform length is latched via the TL_3–TL_0 inputs. $\overline{TSTRB}$ and $\overline{TSEL}$ are the latch enables. They are ANDed so that the latch is transparent when both are LOW. For Radix-4 operations, the transform length is programmable in powers of 4, from 4 to 65,536 points. In Radix-2, the range is 2 to 65,536 points in powers of 2. A Radix-2 Real Valued Input (RVI) algorithm is also supported for transform lengths from 2 to 65,536, in powers of 2. Codes to program the transform length are contained in Figure 1.

Two microcode bits, I_1–I_0, control the operation of the Am29540. The four possible instructions are:

1. HOLD. All counters hold their last values. This instruction is used at any time the counter values must remain constant and could be used during initialization of the part.
2. RESET. All counters are reset to the start of the transform. All unused address lines are set to zero. Control bits DIT/$\overline{DIF}$, Radix 4/$\overline{2}$ and $\overline{PSD}$ are unaffected.
3. RESET/LOAD. All counters are reset to the start of the transform. All unused address lines are set to the current value of the address port. This allows loading of an offset address via the bidirectional address port. This offset is effectively ORed onto the higher significant bits of the address which are unused for the transform length. Only data address counters are affected. Coefficient address counters are not affected.
4. COUNT. All counters are incremented to their next valid address.

Codes for all four instructions are contained in Figure 2.

Four address select controls, AS_3–AS_0, choose which of the sixteen counter outputs are available at the address port. Typically, these bits would come from the microcode. Data addresses are right-justified, A_{15} being the MSB. Coefficient addresses are left-justified: A_{15} is the MSB for Radix-4 operations; A_{14} is the MSB for Radix-2 operations. Codes for AS_3–AS_0 are contained in Figure 3.

Two output flags, ITCOMP and FFTCOMP, indicate counter status. When the bottom of a column of butterflies is reached, Iteration Complete (ITCOMP) goes HIGH. When the last butterfly (or end) of the transform is reached, FFT Complete (FFTCOMP) also goes HIGH. These two flags would typically be condition code inputs to the microprogram sequencer.

A third flag is used to indicate end of column for non-in-place transforms or one of two butterfly types for RVI transforms. For column indication, the flag is called ODD/$\overline{EVEN}$ and can be used to switch memory banks. The flag will be a HIGH for the last column of butterflies. In the RVI transform the flag is called KNZ/$\overline{KZ}$. The equations for the butterfly when the rotational constant is W^0 are different from when the rotational constant is not W^0. When KNZ/$\overline{KZ}$ is LOW, it indicates that the rotational constant to be used is W^0 and that the alternative butterfly equations must be executed. Typically there are two microcode segments. The KNZ/$\overline{KZ}$ flag would be a condition code input to the sequencer to select one of the two segments.

TL_3	TL_2	TL_1	TL_0	Transform Length		
				Radix-2	Radix-4	RVI
L	L	L	L	2	4	4
L	L	L	H	4	4	8
L	L	H	L	8	16	16
L	L	H	H	16	16	32
L	H	L	L	32	64	64
L	H	L	H	64	64	128
L	H	H	L	128	256	256
L	H	H	H	256	256	512
H	L	L	L	512	1024	1024
H	L	L	H	1024	1024	2048
H	L	H	L	2048	4096	4096
H	L	H	H	4096	4096	8192
H	H	L	L	8192	16384	16384
H	H	L	H	16384	16384	32768
H	H	H	L	32768	65536	65536
H	H	H	H	65536	65536	Not Used

Figure 1. Transform Length Control

I_1	I_0	Counter Function
L	L	Hold
L	H	Reset. Reset counter to start of transform with unused address outputs set to 0.
H	L	Reset/Load. Reset counter to start of transform with unused address outputs set to the current value of the address bus.
H	H	Count. Increment butterfly counter.

Figure 2. Counter Instruction Control

FFT Type	AS_3	AS_2
Complex Input	L	X
	X	L
Real Valued Input (RVI)	H	H

Figure 2a. Offset Address Control

AS =	AS_3	AS_2	AS_1	AS_0	Description	Usage
0	L	L	L	L	Data Address 1	Radix 2/4
1	L	L	L	H	Data Address 2	Radix 2/4
2	L	L	H	L	Data Address 3	Radix 4
3	L	L	H	H	Data Address 4	Radix 4
4	L	H	L	L	Alt. Data Address 1	Radix 2/4
5	L	H	L	H	Alt. Data Address 2	Radix 2/4
6	L	H	H	L	Alt. Data Address 3	Radix 4
7	L	H	H	H	Alt. Data Address 4	Radix 4
8	H	L	L	L	Const Address 1	Radix 2/4, Shading
9	H	L	L	H	Const Address 2	Radix 4
10	H	L	H	L	Const Address 3	Radix 4
11	H	L	H	H	$\overline{\text{Const Address 1}}$	Shading
12	H	H	L	L	RVI Data Address 1	RVI
13	H	H	L	H	RVI Data Address 2	RVI
14	H	H	H	L	RVI Data Address 3	RVI
15	H	H	H	H	RVI Data Address 4	RVI

Figure 3. Address Select Control

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65 to +150°C
Temperature Under Bias-T_C ..... −55 to +125°C
Supply Voltage to Ground Potential
Continuous ..... −0.5 to +7.0V
DC Voltage Applied to Outputs For
High Output State ..... −0.5V to +V_{CC} max
DC Input Voltage ..... −0.5 to +5.5V
DC Output Current, Into Outputs 30mA
DC Input Current ..... −30mA to +5.0mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature
DIPs ..... T_A = 0°C to +70°C
Chip Carriers ..... T_C = 0°C to 85°C
Supply Voltage ..... +4.75V to +5.25V

Military (M) Devices
Temperature ..... T_C = −55°C to +125°C
Supply Voltage ..... +4.5V to +5.5V

Operating ranges define those limits over which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified

Parameters	Description	Test Conditions (Note 1)		Min	Typ (Note 2)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	I_{OH} = −2.6mA, COM'L	2.4			Volts
			I_{OH} = −mA, MIL				
V_{OL}	Output LOW Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 12mA			0.5	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs				0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −18mA				−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX, V_{IN} = 0.4V				−0.4	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX, V_{IN} = 2.7V				20	μA
I_I	Input HIGH Current	V_{CC} = MAX, V_{IN} = 5.5V (See Note 5)				100	μA
I_{OZH}	Off State (High Impedance) Output Current	V_{CC} = MAX	V_{IN} = 2.7V			20	μA
I_{OZL}			V_{IN} = 0.4V			0.4	mA
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX		−30		−85	mA
I_{CC}	Power Supply Current (Note 4)	COM'L and MIL	T_A=25°C		320	450	mA
		COM'L Only	T_A = 0 to +70°C (Note 6)			450	
		V_{CC} = MAX	T_A = +70°C (Note 6)			400	
		MIL Only	T_C = −55 to +125°C			470	
		V_{CC} = MAX	T_C = +125°C			350	

Notes: 1. For conditions shown as MIN or MAX, use the appropriate value specified under Operating Ranges for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. $\overline{OE}$ LOW and all inputs LOW.
5. It is limited to 5.5V because A_0 to A_{15} inputs also connect to output transistors.
6. Chip Carriers: T_C = 0 to 85°C.

SWITCHING CHARACTERISTICS over operating range unless otherwise specified (T_A = 25°C, V_{CC} = 5.0V)

Parameters		Description	Test Conditions	Min	Typ	Max	Units
1	t_{PD}	CP to A_{0-15}(AS = 0)	C_L = 50pF See Test Circuits		21	30	ns
1	t_{PD}	CP to A_{0-15}(AS = 1)			21	30	ns
1	t_{PD}	CP to A_{0-15}(AS = 2)			21	30	ns
1	t_{PD}	CP to A_{0-15}(AS = 3)			21	30	ns
1	t_{PD}	CP to A_{0-15}(AS = 4)			21	30	ns
1	t_{PD}	CP to A_{0-15}(AS = 5)			21	30	ns
1	t_{PD}	CP to A_{0-15}(AS = 6)			21	30	ns
1	t_{PD}	CP to A_{0-15}(AS = 7)			21	30	ns
1	t_{PD}	CP to A_{0-15}(AS = 8)			25	32	ns
1	t_{PD}	CP to A_{0-15}(AS = 9)			25	32	ns
1	t_{PD}	CP to A_{0-15}(AS = 10)			30	40	ns
1	t_{PD}	CP to A_{0-15}(AS = 11)			21	40	ns
1	t_{PD}	CP to A_{0-15}(AS = 12)			21	30	ns
1	t_{PD}	CP to A_{0-15}(AS = 13)			21	30	ns
1	t_{PD}	CP to A_{0-15}(AS = 14)			21	30	ns
1	t_{PD}	CP to A_{0-15}(AS = 15)			21	30	ns
2	t_{PD}	Address Select to A_{0-15}	With A_2 LOW		30	40	ns
			With A_2 Active		45	60	ns
3	t_{PHZ}	$\overline{OE}$ to A_{0-15} Disable Time			20	30	ns
4	t_{PLZ}	$\overline{OE}$ to A_{0-15} Disable Time			20	35	ns
5	t_{PZH}	$\overline{OE}$ to A_{0-15} Enable Time			18	30	ns
6	t_{PZL}	$\overline{OE}$ to A_{0-15} Enable Time			16	25	ns
7	t_{PD}	CP to IT COMP			20	30	ns
8	t_{PD}	CP to FFT COMP			20	30	ns
9	t_{PD}	CP to ODD/$\overline{EVEN}$/ (KNZ/$\overline{KZ}$)			30	40	ns
10	t_{PD}	Address Select to ODD/$\overline{EVEN}$/ (KNZ/$\overline{KZ}$)			20	30	ns
11	t_S	Offset Address Input A_{0-15} to CP Set-up Time		10	4		ns
12	t_H	Offset Address Input A_{0-15} to CP Hold Time		0	−1		ns
13	t_S	Counter Instruction to CP Set-up Time		20	11		ns
14	t_H	Counter Instruction to CP Hold Time		0	0		ns
15	t_S	Transform Length Select to CP Set-up Time		40	25		ns
16	t_H	Transform Length Select to CP Hold Time		0	0		ns
17	t_S	Transform Length Select to $\overline{TSTRB}$ ↑ Set-up Time		8	4		ns
18	t_H	Transform Length Select to $\overline{TSTRB}$ ↑ Hold Time		5	3		ns
19	t_S	$\overline{TSEL}$ (HIGH to LOW) to $\overline{TSTRB}$ ↑ Set-up Time		15	10		ns
20	t_H	$\overline{TSEL}$ to $\overline{TSTRB}$↑ Hold Time		15	10		ns
21	t_S	RADIX 4/$\overline{2}$ to CP Set-up Time		25	16		ns
22	t_H	RADIX 4/$\overline{2}$ to CP Hold Time		0	0		ns
23	t_S	RADIX 4/$\overline{2}$, $\overline{PSD}$, DIT/$\overline{DIF}$ to $\overline{STRB}$ ↑ Set-up Time		8	5		ns
24	t_H	RADIX 4/$\overline{2}$, $\overline{PSD}$, DIT/$\overline{DIF}$ to $\overline{STRB}$ ↑ Hold Time		0	0		ns
25	t_S	$\overline{SEL}$ (HIGH to LOW) to $\overline{STRB}$ ↑ Set-up Time		15	10		ns
26	t_H	$\overline{SEL}$ Hold Time to $\overline{STRB}$ ↑ Hold Time		15	10		ns
27	t_S	$\overline{STRB}$ or $\overline{TSTRB}$ to CP Set-up Time		45	30		ns
28	t_{PWSL}	Minimum Strobe Pulse Width LOW		15	10		ns
29	t_{PWH}	CP Pulse Width HIGH		15	10		ns
30	t_{PWL}	CP Pulse Width LOW		15	10		ns

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Refer to Page 13-1 for Essential Information on Military Devices

SWITCHING CHARACTERISTICS over operating range unless otherwise specified

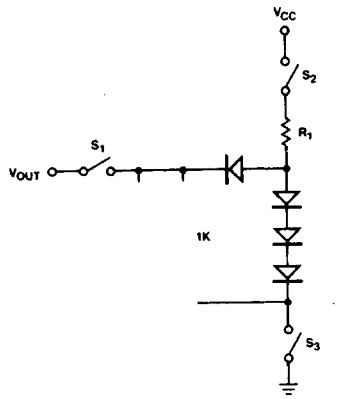
Parameters		Description		Test Conditions	COMMERCIAL Min	COMMERCIAL Max	MILITARY Min	MILITARY Max	Units
1	t_{PD}	CP to A_{0-15}(AS = 0)		C_L = 50pF See Test Circuits		35		40	ns
1	t_{PD}	CP to A_{0-15}(AS = 1)				35		40	ns
1	t_{PD}	CP to A_{0-15}(AS = 2)				35		40	ns
1	t_{PD}	CP to A_{0-15}(AS = 3)				35		40	ns
1	t_{PD}	CP to A_{0-15}(AS = 4)				35		40	ns
1	t_{PD}	CP to A_{0-15}(AS = 5)				35		40	ns
1	t_{PD}	CP to A_{0-15}(AS = 6)				35		40	ns
1	t_{PD}	CP to A_{0-15}(AS = 7)				35		40	ns
1	t_{PD}	CP to A_{0-15}(AS = 8)				42		50	ns
1	t_{PD}	CP to A_{0-15}(AS = 9)				42		50	ns
1	t_{PD}	CP to A_{0-15}(AS = 10)				53		60	ns
1	t_{PD}	CP to A_{0-15}(AS = 11)				53		60	ns
1	t_{PD}	CP to A_{0-15}(AS = 12)				35		40	ns
1	t_{PD}	CP to A_{0-15}(AS = 13)				35		40	ns
1	t_{PD}	CP to A_{0-15}(AS = 14)				35		40	ns
1	t_{PD}	CP to A_{0-15}(AS = 15)				35		40	ns
2	t_{PD}	Address Select to A_{0-15}	With A_2 LOW			45		50	ns
			With A_2 Active			65		70	ns
3	t_{PHZ}	$\overline{OE}$ to A_{0-15} Disable Time				32		35	ns
4	t_{PLZ}	$\overline{OE}$ to A_{0-15} Disable Time				40		45	ns
5	t_{PZH}	$\overline{OE}$ to A_{0-15} Enable Time				35		40	ns
6	t_{PZL}	$\overline{OE}$ to A_{0-15} Enable Time				30		35	ns
7	t_{PD}	CP to IT COMP				40		50	ns
8	t_{PD}	CP to FFT COMP				40		50	ns
9	t_{PD}	CP to ODD/$\overline{EVEN}$/(KNZ/$\overline{KZ}$)				53		60	ns
10	t_{PD}	Address Select to ODD/$\overline{EVEN}$/(KNZ/$\overline{KZ}$)				38		45	ns
11	t_S	Offset Address Input A_{0-15} to CP Setup Time			11		12		ns
12	t_H	Offset Address Input A_{0-15} to CP Hold Time			1		2		ns
13	t_S	Counter Instruction to CP Setup Time			22		25		ns
14	t_H	Counter Instruction to CP Hold Time			0		0		ns
15	t_S	Transform Length Select to CP Setup Time			45		50		ns
16	t_H	Transform Length Select to CP Hold Time			0		0		ns
17	t_S	Transform Length Select to $\overline{TSTRB}$ ↑ Setup Time			9		10		ns
18	t_H	Transform Length Select to $\overline{TSTRB}$ ↑ Hold Time			7		8		ns
19	t_S	$\overline{TSEL}$ (HIGH to LOW) to $\overline{TSTRB}$ ↑ Setup Time			18		20		ns
20	t_H	TSEL to$\overline{TSTRB}$ ↑ Hold Time			18		20		ns
21	t_S	RADIX 4/$\overline{2}$ to CP Setup Time			28		30		ns
22	t_H	RADIX 4/$\overline{2}$ to CP Hold Time			0		0		ns
23	t_S	RADIX 4/$\overline{2}$, $\overline{PSD}$, DIT/$\overline{DIF}$ to $\overline{STRB}$ ↑ Setup Time			9		10		ns
24	t_H	RADIX 4/$\overline{2}$, $\overline{PSD}$, DIT/$\overline{DIF}$ to $\overline{STRB}$ ↑ Hold Time			1		2		ns
25	t_S	$\overline{SEL}$ (HIGH to LOW) to $\overline{STRB}$ ↑ Setup Time			18		20		ns
26	t_H	$\overline{SEL}$ Hold Time to $\overline{STRB}$ ↑ Hold Time			18		20		ns
27	t_S	$\overline{STRB}$ or $\overline{TSTRB}$ to CP Setup Time			50		55		ns
28	t_{PWSL}	Minimum Strobe Pulse Width LOW			18		20		ns
29	t_{PWH}	CP Pulse Width HIGH			18		20		ns
30	t_{PWL}	CP Pulse Width LOW			18		20		ns

03567C

Refer to Page 13-1 for Essential Information on Military Devices

SWITCHING TEST CIRCUIT

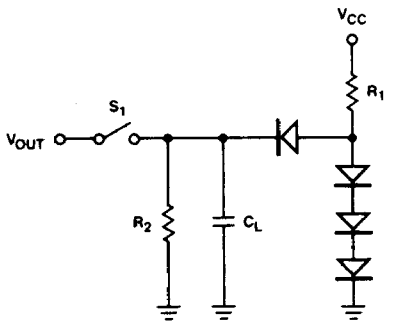
A. THREE-STATE OUTPUTS



TCR01230

$$R_1 = \frac{\frac{5.0 - V_{BE} - V_{OL}}{I_{OL} + V_{OL}}}{1K}$$

B. NORMAL OUTPUTS



TCR01240

$$R_2 = \frac{2.4V}{I_{OH}} \qquad R_1 = \frac{\frac{5.0 - V_{BE} - V_{OL}}{I_{OL} + V_{OL}}}{R_2}$$

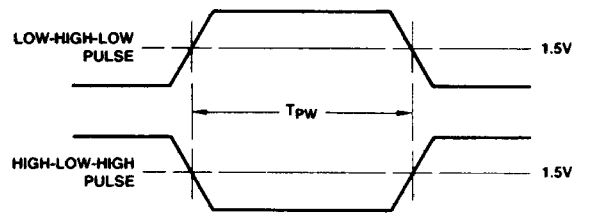
Notes: 1. C_L = 50pF includes scope probe, wiring and stray capacitances without device in test fixture.
2. S_1, S_2, S_3 are closed during function tests and all AC tests except output enable tests.
3. S_1 and S_3 are closed while S_2 is open for t_{PZH} test.
   S_1 and S_2 are closed while S_3 is open for t_{PZL} test.
4. C_L = 5.0pF for output disable tests.

SWITCHING TEST WAVEFORMS

Test	Output Waveform – Measurement Level
All t_{PD}s	V_{OH}, V_{OL}, 1.5V
t_{PHZ}	V_{OH}, 0.5V, 0.0V
t_{PLZ}	3V, 0.5V, V_{OL}
t_{PZH}	V_{OH}, 1.5V, 0.0V
t_{PZL}	3V, 1.5V, V_{OL}

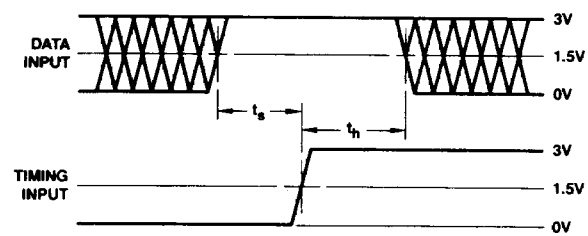
WFR02681

PULSE WIDTH



WFR02850

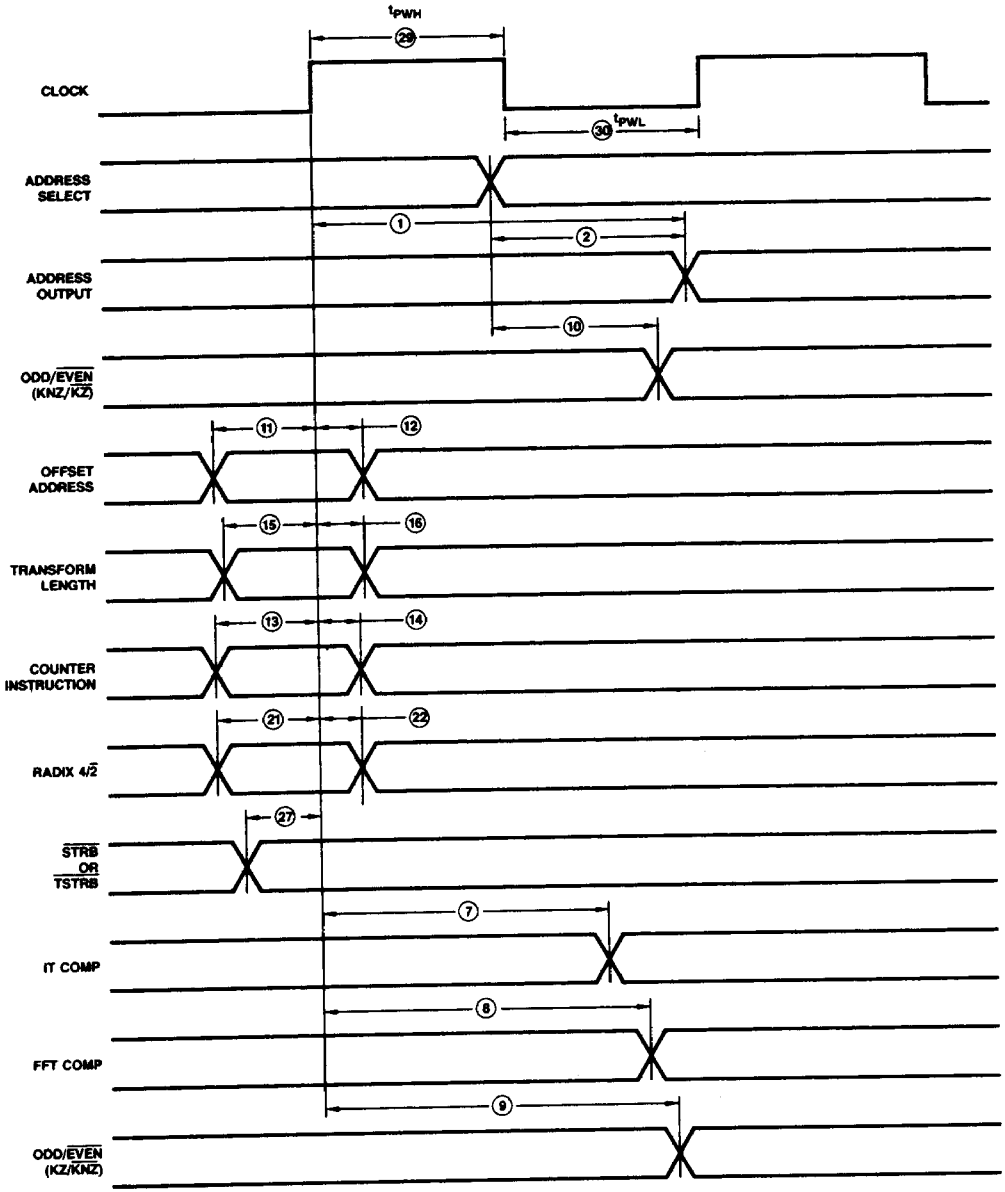
SET-UP AND HOLD TIME



WFR02970

Notes: 1. Diagram shown for HIGH data only. Output transition may be opposite sense.
2. Cross hatched area is don't care condition.

TIMING DIAGRAM

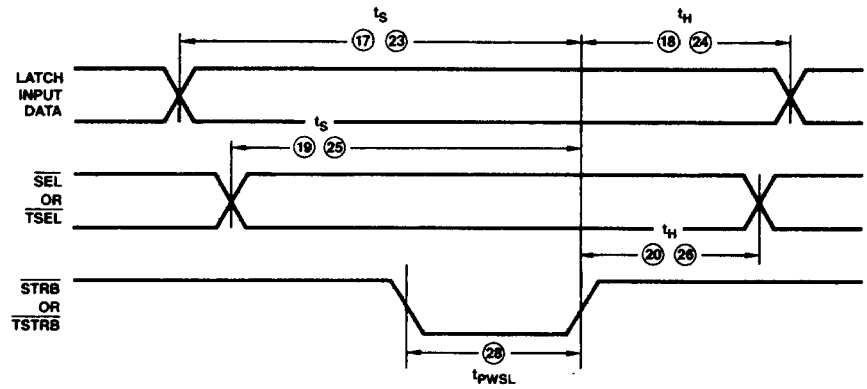


WFR02710

03567C

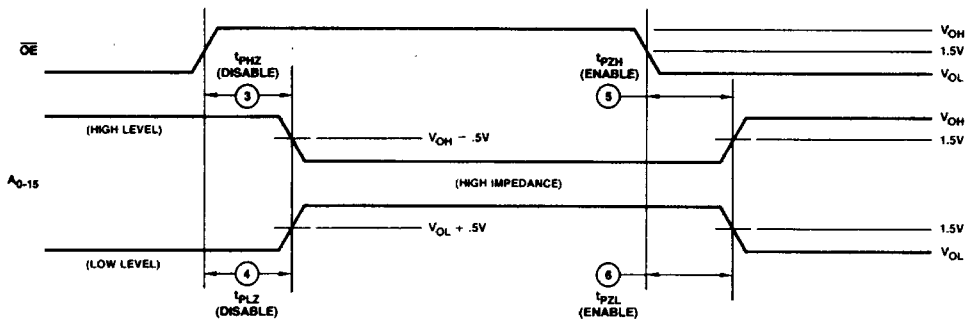
Refer to Page 13-1 for Essential Information on Military Devices

LATCH TIMING DIAGRAM



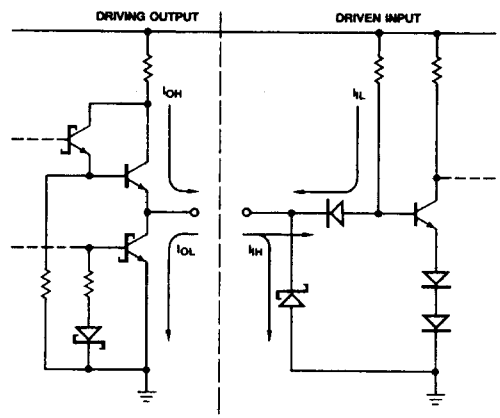
WFR02701

3-STATE TIMING DIAGRAM

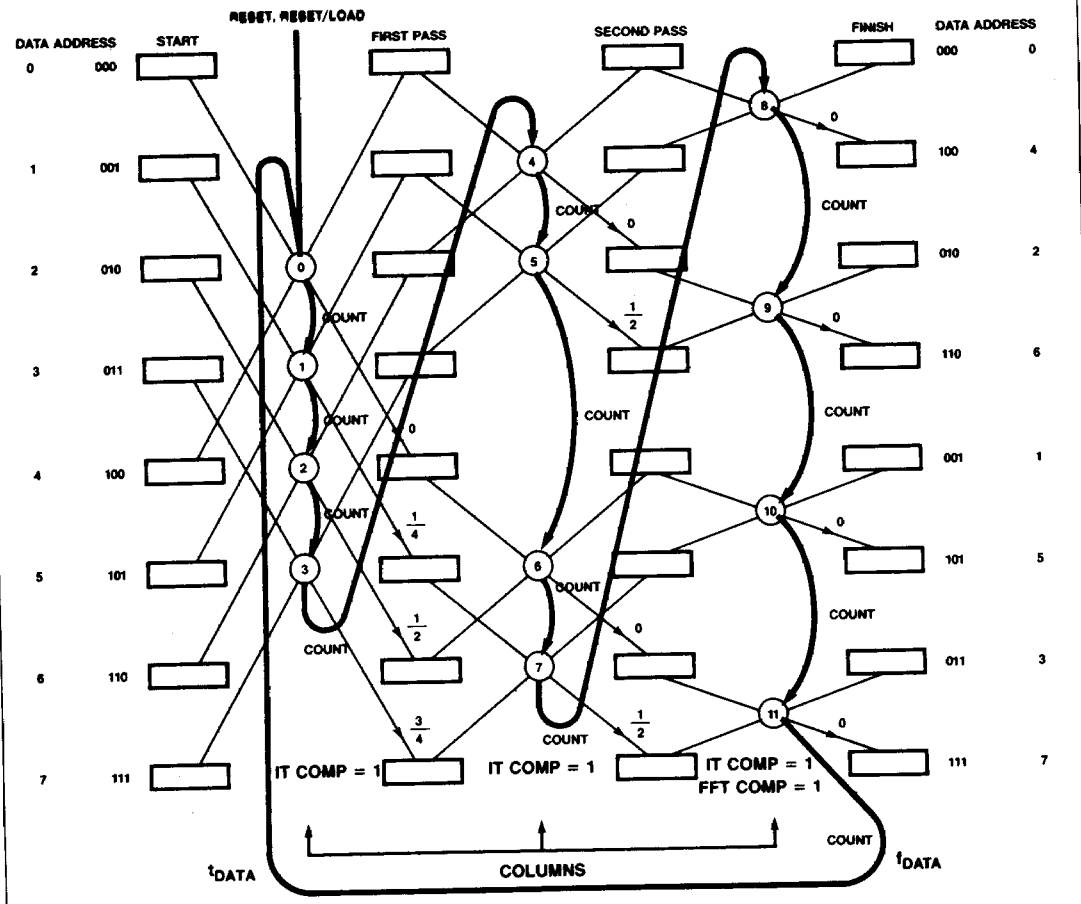


WFR02720

INPUT/OUTPUT CURRENT INTERFACE CONDITIONS

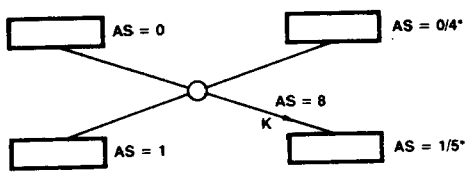


ICR00510



DFR00660

a. Sequence of Operations for Typical FFT



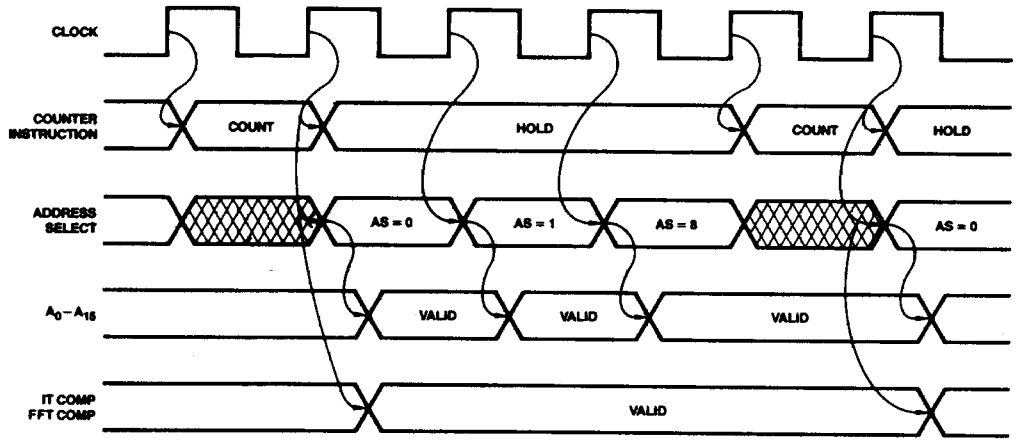
DFR00670

*Note: AS = 4 and AS = 5 are alternate addresses used in non-in-place transformations.

b. Single RADIX-2 Butterfly

Figure 4.

TYPICAL HIGH PERFORMANCE RADIX-2 ADDRESS GENERATION



DFR00690

TRANSFORM CHARACTERISTICS

- 16-Point (N = 16)
- RADIX-2
- DIF
- Normally ordered input data (Bit-reversed output data order)
- In-place
- Complex valued input data

FORWARD TRANSFORM

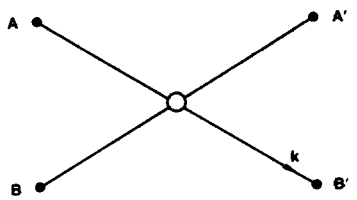
$A' = A + B$
$B' = (A - B)W^k$

INVERSE TRANSFORM

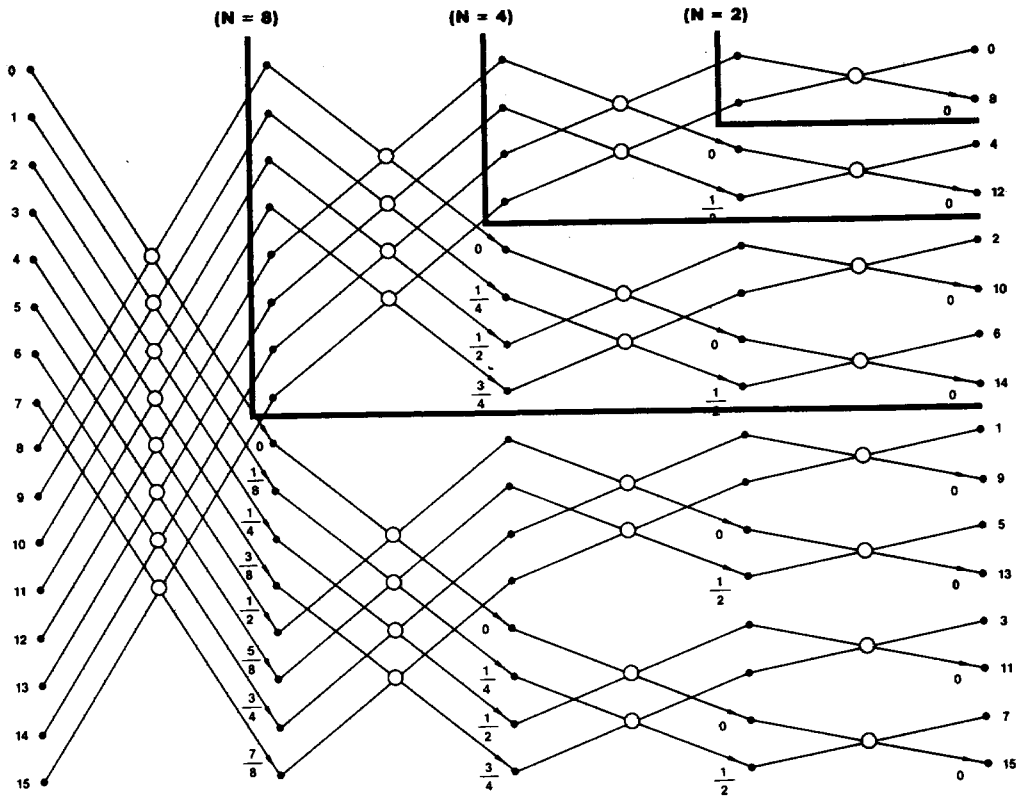
$A' = A + B$
$B' = (A - B)W^{-k}$

$W = e^{-j\pi}$

TYPICAL BUTTERFLY



DFR00640



DFR00700

DIT/$\overline{\text{DIF}}$	$\overline{\text{PSD}}$	RADIX 4/$\overline{2}$
L	H	L

Address of	A	B	A'	B'	W^k
AS =	0	1	0	1	8

7

03567C

Refer to Page 13-1 for Essential Information on Military Devices

TRANSFORM CHARACTERISTICS

- 16-Point (N = 16)
- RADIX-2
- DIF
- Normally ordered output data (Bit-reversed input data order)
- In-place
- Complex valued input data

FORWARD TRANSFORM

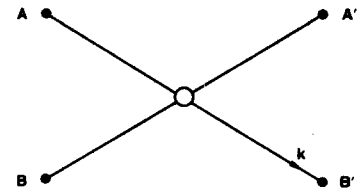
$A' = A + B$
$B' = (A - B)W^k$

INVERSE TRANSFORM

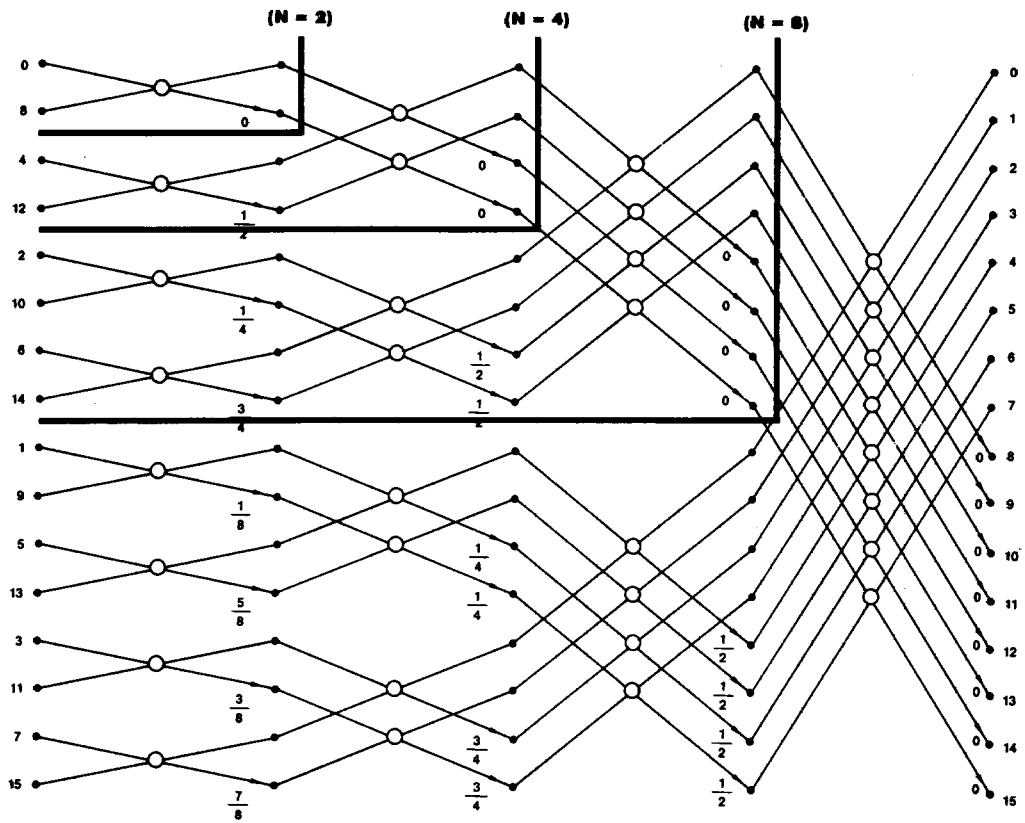
$A' = A + B$
$B' = (A - B)W^{-k}$

$W = e^{-j\pi}$

TYPICAL BUTTERFLY



DFR00640



DFR00630

DIT/$\overline{\text{DIF}}$	$\overline{\text{PSD}}$	RADIX 4/$\overline{2}$
L	L	L

Address of	A	B	A'	B	W_K
AS =	0	1	0	1	8

TRANSFORM CHARACTERISTICS

- 16-Point (N = 16)
- RADIX-2
- DIF
- Normally ordered input and output data (Non-bit-reversing)
- Non-in-place
- Complex valued input data

FORWARD TRANSFORM

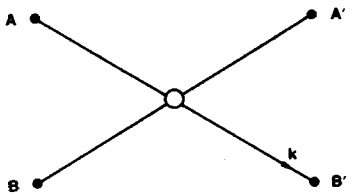
$A' = A + B$
$B' = (A - B)W^k$

INVERSE TRANSFORM

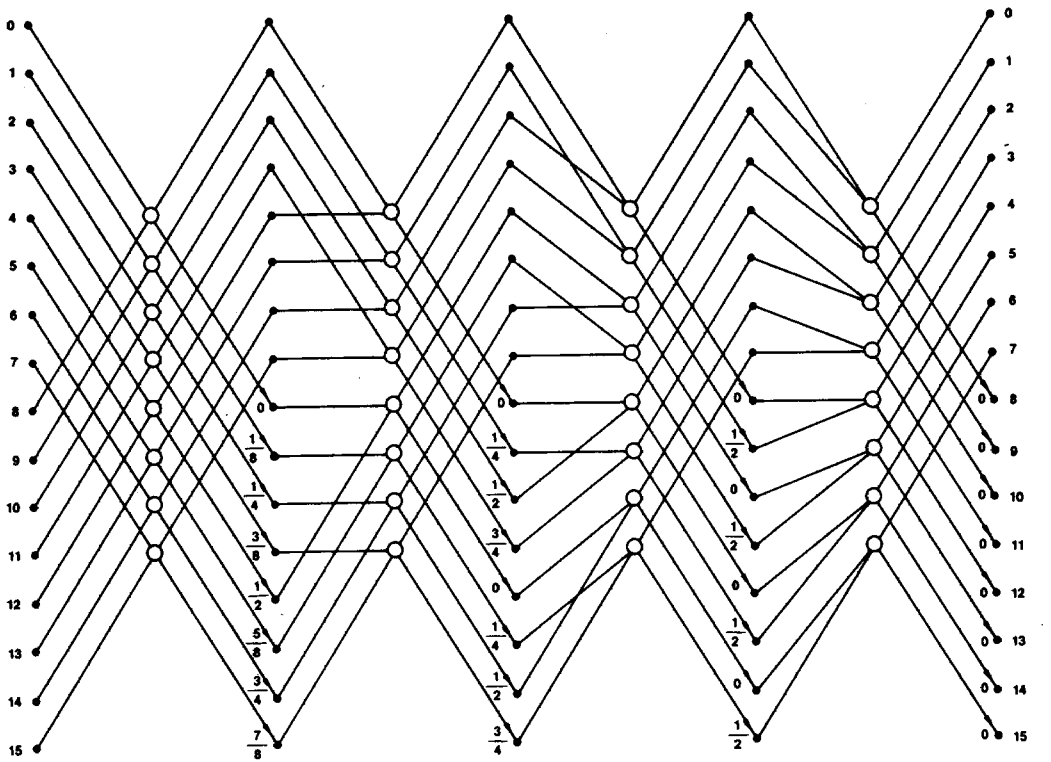
$A' = A + B$
$B' = (A - B)W^{-k}$

$W = e^{-i\pi}$

TYPICAL BUTTERFLY



DFR00640



DFR00650

DIT/$\overline{\text{DIF}}$	$\overline{\text{PSD}}$	RADIX 4/$\overline{2}$
L	H	L

Address of	A	B	A'	B'	W^k
AS =	0	1	4	5	8

03567C

Refer to Page 13-1 for Essential Information on Military Devices

TRANSFORM CHARACTERISTICS

- 16-Point (N = 16)
- RADIX-2
- DIT
- Normally ordered input data (Bit-reversed output data order)
- In-place
- Complex valued input data

FORWARD TRANSFORM

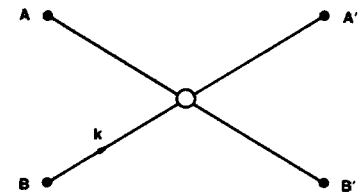
$A' = A + BW^k$
$B' = A - BW^k$

INVERSE TRANSFORM

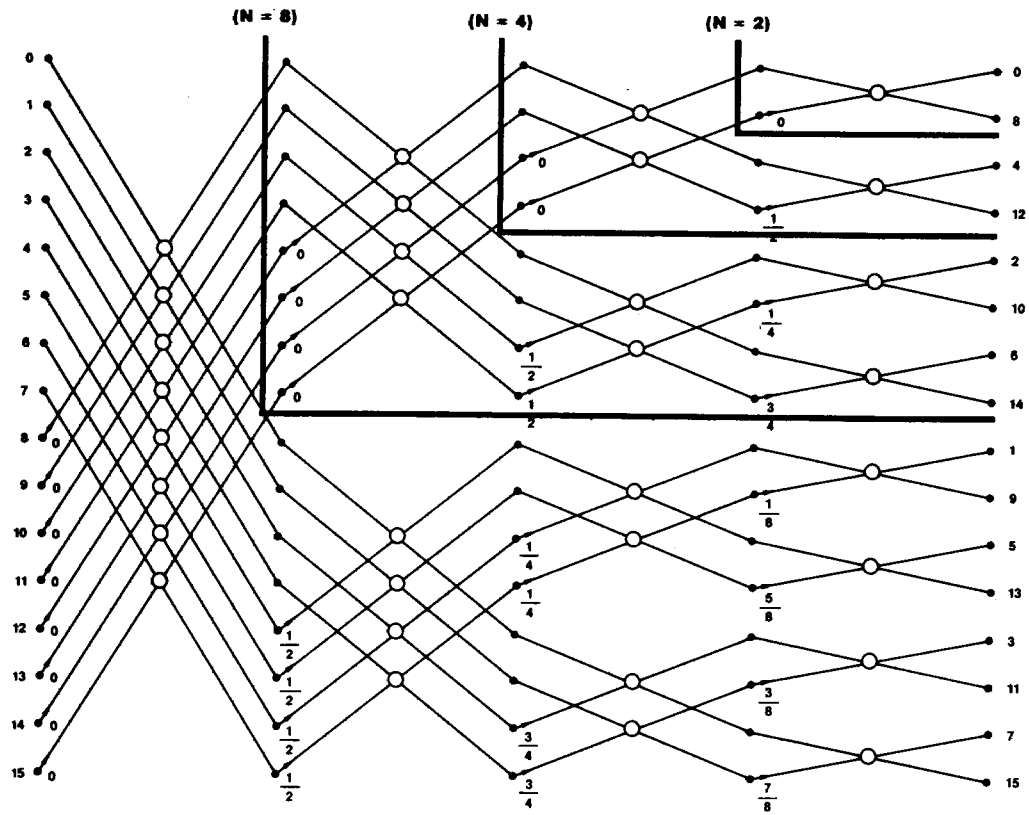
$A' = A + BW^{-k}$
$B' = A - BW^{-k}$

$W = e^{-j\pi}$

TYPICAL BUTTERFLY



DFR00590



DFR00620

DIT/$\overline{\text{DIF}}$	$\overline{\text{PSD}}$	RADIX 4/$\overline{2}$
H	H	L

Address of	A	B	A'	B'	W^k
AS =	0	1	0	1	8

03567C

Refer to Page 13-1 for Essential Information on Military Devices

TRANSFORM CHARACTERISTICS

- 16-Point (N = 16)
- RADIX-2
- DIT
- Normally ordered output data (Bit-reversed input data order)
- In-place
- Complex valued input data

FORWARD TRANSFORM

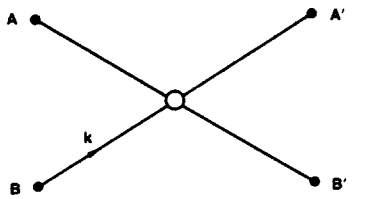
$A' = A + BW^k$
$B' = A - BW^k$

INVERSE TRANSFORM

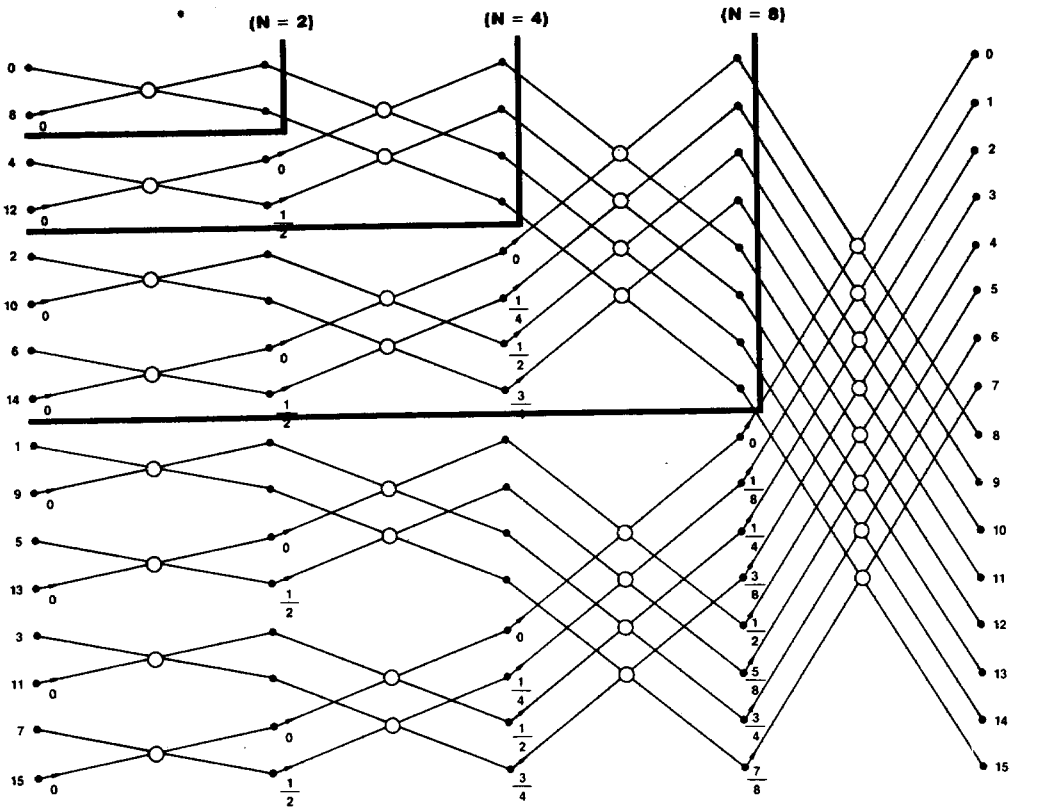
$A' = A + BW^{-k}$
$B' = A - BW^{-k}$

$W = e^{-j\pi}$

TYPICAL BUTTERFLY



DFR00590



DFR00470

DIT/$\overline{DIF}$	$\overline{PSD}$	RADIX 4/$\overline{2}$
H	L	L

Address of	A	B	A'	B'	W^k
AS =	0	1	0	1	8

03567C

Refer to Page 13-1 for Essential Information on Military Devices

TRANSFORM CHARACTERISTICS

- 16-Point (N = 16)
- RADIX-2
- DIT
- Normally ordered input and output data (Non-bit-reversing)
- Non-in-place
- Complex valued input data

FORWARD TRANSFORM

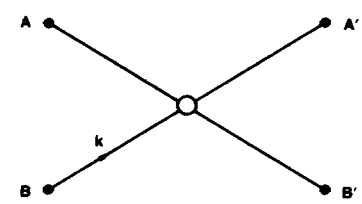
$A' = A + BW^k$
$B' = A - BW^k$

INVERSE TRANSFORM

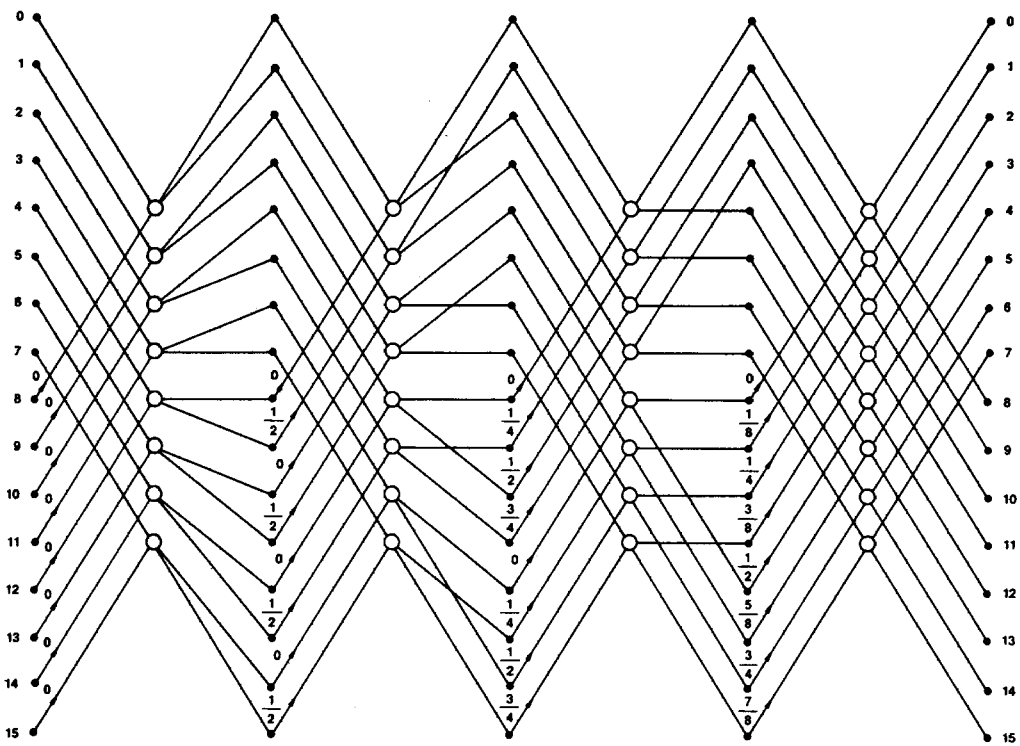
$A' = A + BW^{-k}$
$B' = A - BW^{-k}$

$W = e^{-j\pi}$

TYPICAL BUTTERFLY



DFR00590



DFR00560

DIT/$\overline{DIF}$	$\overline{PSD}$	RADIX 4/2
H	L	L

Address of	A	B	A'	B'	W^k
AS =	4	5	0	1	8

TRANSFORM CHARACTERISTICS

- 16-Point (N = 16)
- RADIX-4
- DIF
- Normally ordered input data
  (Digit-reversed output data order)
- In-place
- Complex valued input data

FORWARD TRANSFORM

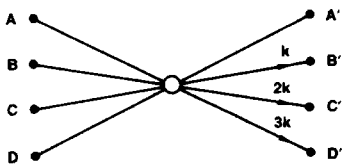
$A' = A + B + C + D$
$B' = (A - jB - C + jD)W^{k}$
$C' = (A - B + C - D)W^{2k}$
$D' = (A + jB - C - jD)W^{3k}$

INVERSE TRANSFORM

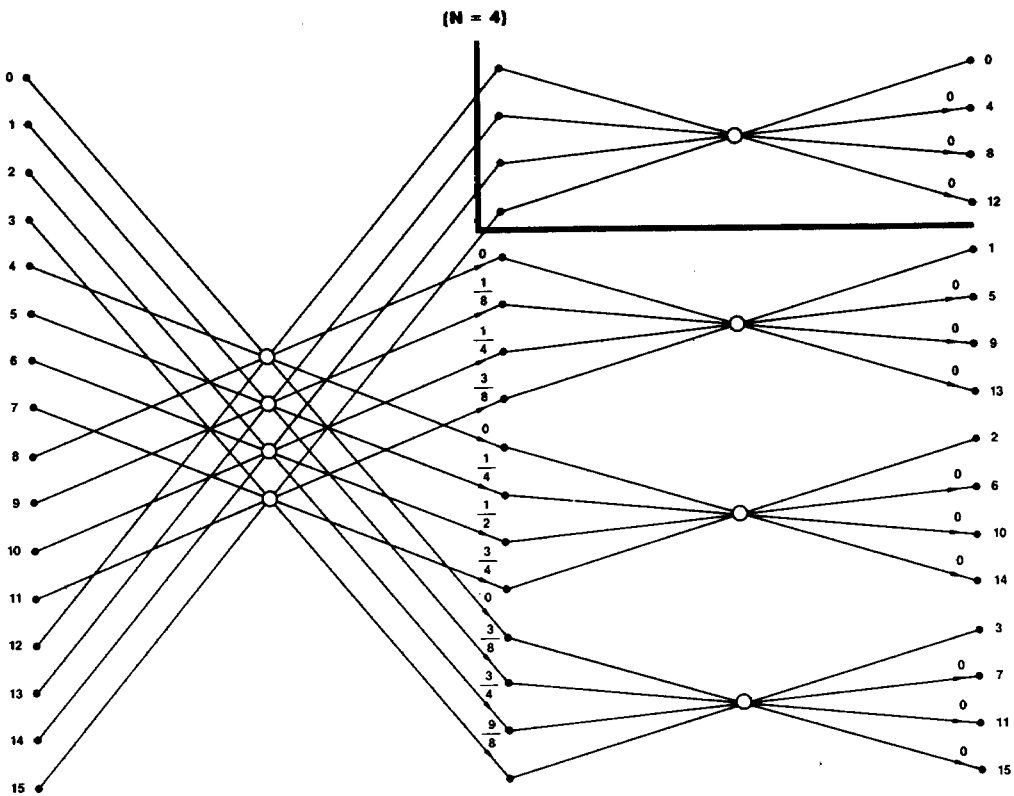
$A' = A + B + C + D$
$B' = (A + jB - C - jD)W^{-k}$
$C' = (A - B + C - D)W^{-2k}$
$D' = (A - jB - C + jD)W^{-3k}$

$W = e^{-j\pi}$

TYPICAL BUTTERFLY



DFR00510



DFR00570

DIT/$\overline{DIF}$	$\overline{PSD}$	RADIX 4/2
L	H	H

Address of	A	B	C	D	A'	B'	C'	D'	W^{k}	W^{2k}	W^{3k}
AS =	0	1	2	3	0	1	2	3	8	9	10

03567C

Refer to Page 13-1 for Essential Information on Military Devices

TRANSFORM CHARACTERISTICS

- 16-Point (N = 16)
- RADIX-4
- DIF
- Normally ordered output data (Digit-reversed input data order)
- In-place
- Complex valued input data

FORWARD TRANSFORM

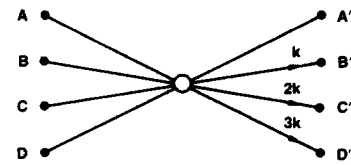
$A' = A + B + C + D$
$B' = (A - jB - C + jD)W^{k}$
$C' = (A - B + C - D)W^{2k}$
$D' = (A + jB - C - jD)W^{3k}$

INVERSE TRANSFORM

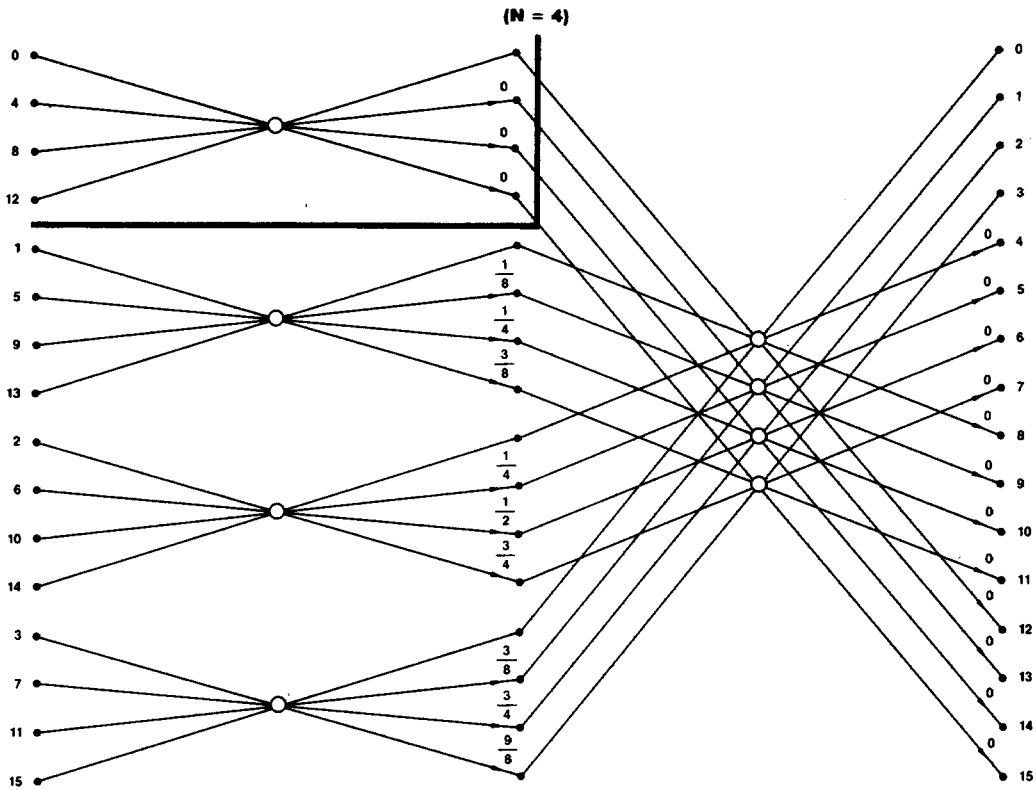
$A' = A + B + C + D$
$B' = (A + jB - C - jD)W^{-k}$
$C' = (A - B + C - D)W^{-2k}$
$D' = (A - jB - C + jD)W^{-3k}$

$W = e^{-j\pi}$

TYPICAL BUTTERFLY



DFR00510



DFR00500

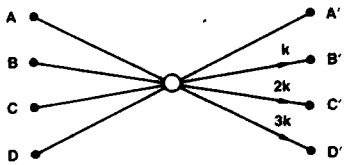
DIT/$\overline{\text{DIF}}$	$\overline{\text{PSD}}$	RADIX 4/$\overline{2}$
L	L	H

Address of	A	B	C	D	A'	B'	C'	D'	W^{k}	W^{2k}	W^{3k}
AS =	0	1	2	3	0	1	2	3	8	9	10

TRANSFORM CHARACTERISTICS

- 16-Point (N = 16)
- RADIX-4
- DIF
- Normally ordered input and output data (Non-digit reversing)
- Non-in-place
- Complex valued input data

TYPICAL BUTTERFLY



DFR00510

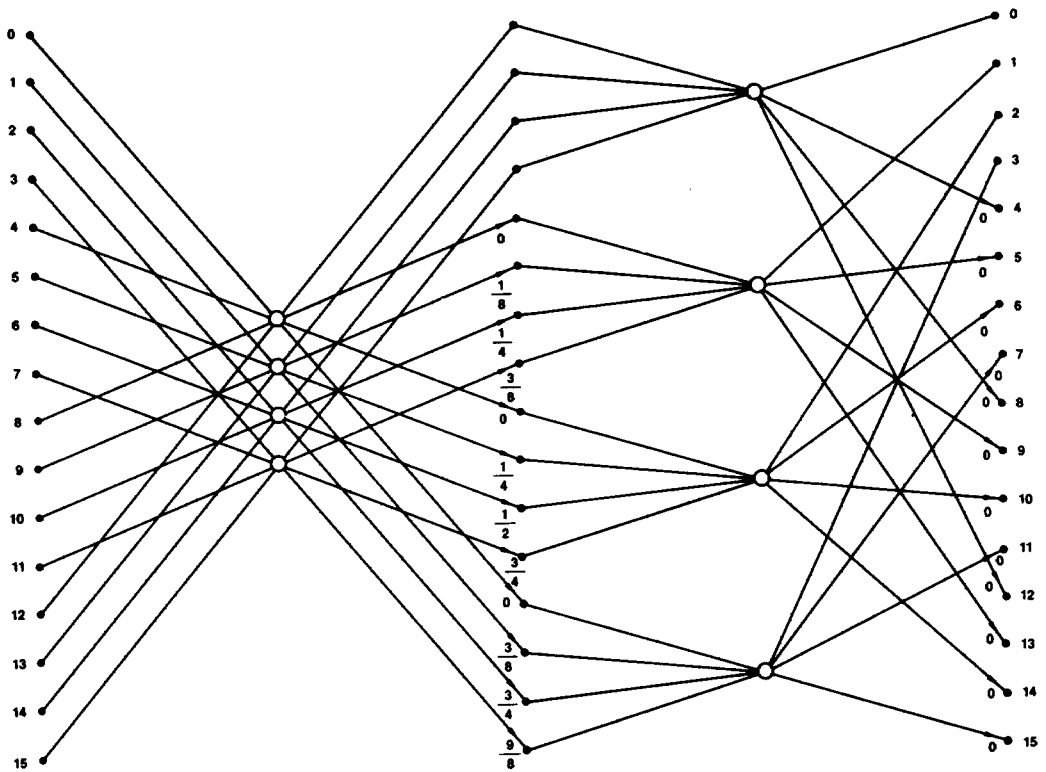
FORWARD TRANSFORM

$A' = A + B + C + D$
$B' = (A - jB - C + jD)W^{k}$
$C' = (A - B + C - D)W^{2k}$
$D' = (A + jB - C - jD)W^{3k}$

INVERSE TRANSFORM

$A' = A + B + C + D$
$B' = (A + jB - C - jD)W^{-k}$
$C' = (A - B + C - D)W^{-2k}$
$D' = (A - jB - C + jD)W^{-3k}$

$W = e^{-j\pi}$



DFR00580

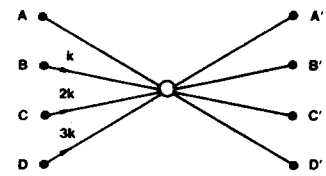
DIT/$\overline{\text{DIF}}$	$\overline{\text{PSD}}$	RADIX 4/$\overline{2}$
L	H	H

Address of	A	B	C	D	A'	B'	C'	D'	W^{k}	W^{2k}	W^{3k}
AS =	0	1	2	3	4	5	6	7	8	9	10

TRANSFORM CHARACTERISTICS

- 16-Point (N = 16)
- RADIX-4
- DIT
- Normally ordered input data (Digit-reversed output data order)
- In-place
- Complex valued input data

TYPICAL BUTTERFLY



DFR00530

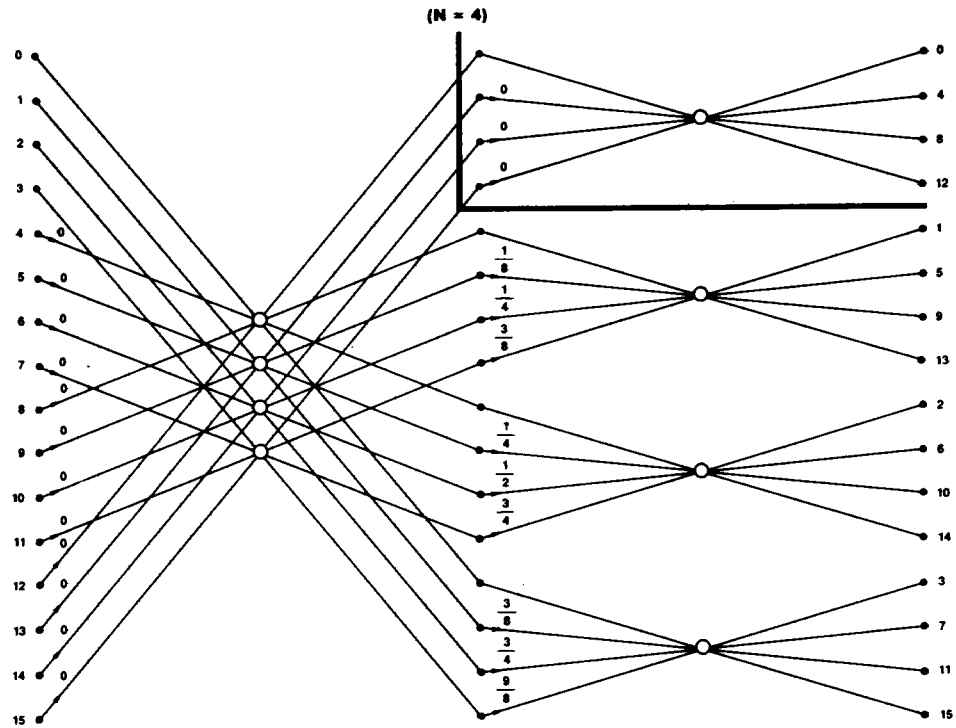
FORWARD TRANSFORM

$$A' = A + BW^{k} + CW^{2k} + DW^{3k}$$
$$B' = A - jBW^{k} - CW^{2k} + jDW^{3k}$$
$$C' = A - BW^{k} + CW^{2k} - DW^{3k}$$
$$D' = A + jBW^{k} - CW^{2k} - jDW^{3k}$$

INVERSE TRANSFORM

$$A' = A + BW^{-k} + CW^{-2k} + DW^{-3k}$$
$$B' = A + jBW^{-k} - CW^{-2k} - jDW^{-3k}$$
$$C' = A - BW^{-k} + CW^{-2k} - DW^{-3k}$$
$$D' = A - jBW^{-k} - CW^{-2k} + jDW^{-3k}$$

$$W = e^{-j\pi}$$



DFR00540

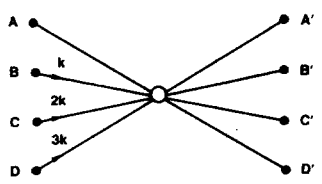
DIT/$\overline{\text{DIF}}$	$\overline{\text{PSD}}$	RADIX 4/$\overline{2}$
H	H	H

Address of	A	B	C	D	A'	B'	C'	D'	W^{k}	W^{2k}	W^{3k}
AS =	0	1	2	3	0	1	2	3	8	9	10

TRANSFORM CHARACTERISTICS

- 16-Point (N = 16)
- RADIX-4
- DIT
- Normally ordered output data (Digit-reversed input data order)
- In-place
- Complex valued input data

TYPICAL BUTTERFLY



DFR00530

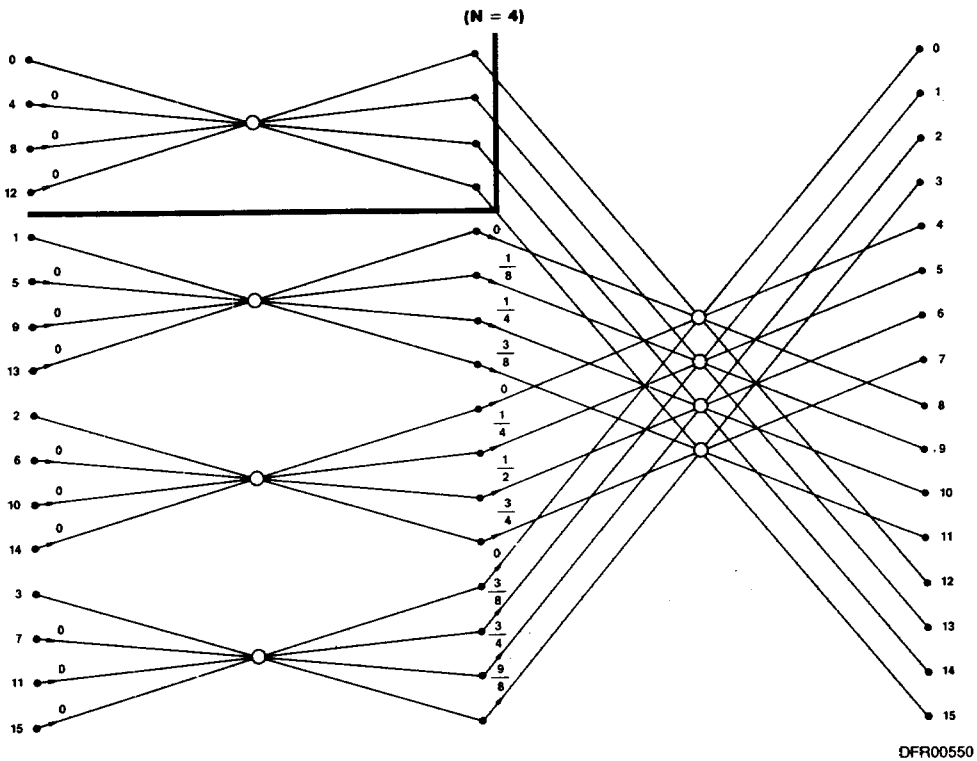
FORWARD TRANSFORM

$$A' = A + BW^{k} + CW^{2k} + DW^{3k}$$
$$B' = A - jBW^{k} - CW^{2k} + jDW^{3k}$$
$$C' = A - BW^{k} + CW^{2k} - DW^{3k}$$
$$D' = A + jBW^{k} - CW^{2k} - jDW^{3k}$$

INVERSE TRANSFORM

$$A' = A + BW^{-k} + CW^{-2k} + DW^{-3k}$$
$$B' = A + jBW^{-k} - CW^{-2k} - jDW^{-3k}$$
$$C' = A - BW^{-k} + CW^{-2k} - DW^{-3k}$$
$$D' = A - jBW^{-k} - CW^{-2k} + jDW^{-3k}$$

$$W = e^{-j\pi}$$



DFR00550

DIT/$\overline{DIF}$	$\overline{PSD}$	RADIX 4/$\overline{2}$
H	L	H

Address of	A	B	C	D	A'	B'	C'	D'	W^{k}	W^{2k}	W^{3k}
AS =	0	1	2	3	0	1	2	3	8	9	10

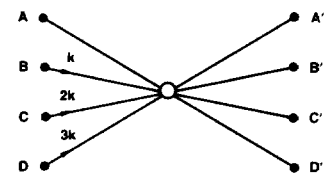
03567C

Refer to Page 13-1 for Essential Information on Military Devices

TRANSFORM CHARACTERISTICS

- 16-Point (N = 16)
- RADIX-4
- DIT
- Normally ordered input and output data (Non-digit reversing)
- Non-in-place
- Complex valued input data

TYPICAL BUTTERFLY



DFR00530

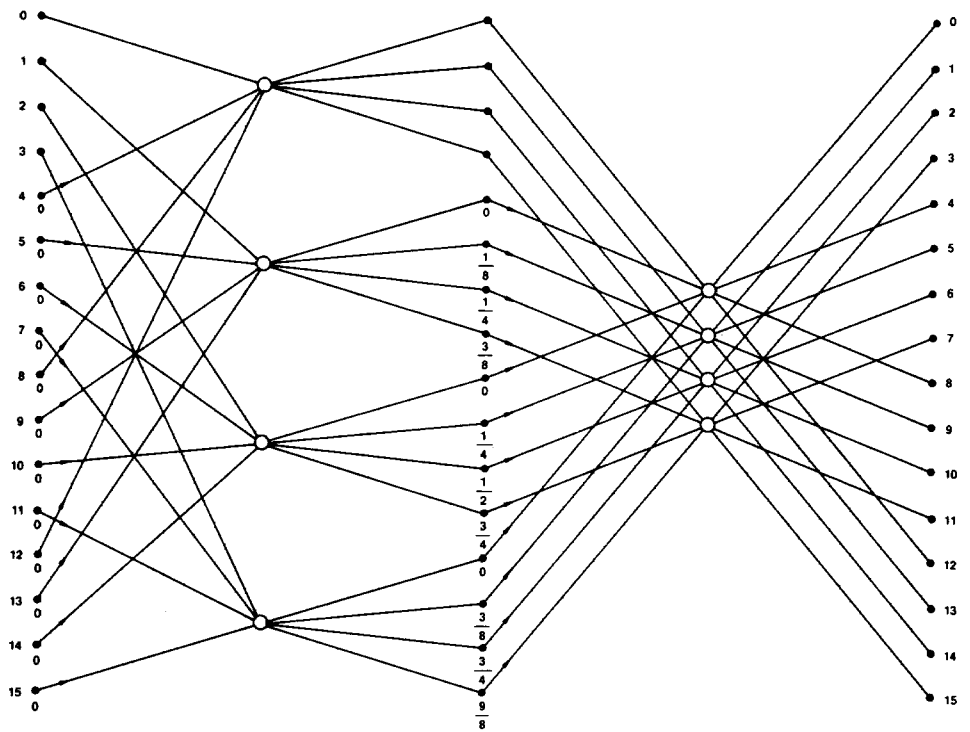
FORWARD TRANSFORM

$$A' = A + BW^{k} + CW^{2k} + DW^{3k}$$
$$B' = A - jBW^{k} - CW^{2k} + jDW^{3k}$$
$$C' = A - BW^{k} + CW^{2k} - DW^{3k}$$
$$D' = A + jBW^{k} - CW^{2k} - jDW^{3k}$$

INVERSE TRANSFORM

$$A' = A + BW^{-k} + CW^{-2k} + DW^{-3k}$$
$$B' = A + jBW^{-k} - CW^{-2k} - jDW^{-3k}$$
$$C' = A - BW^{-k} + CW^{-2k} - DW^{-3k}$$
$$D' = A - jBW^{-k} - CW^{-2k} + jDW^{-3k}$$

$$W = e^{-j\pi}$$



DFR00520

DIT/$\overline{\text{DIF}}$	$\overline{\text{PSD}}$	RADIX 4/2
H	L	H

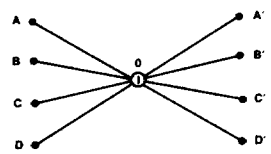
Address of	A	B	C	D	A'	B'	C'	D'	W^{k}	W^{2k}	W^{3k}
AS =	4	5	6	7	0	1	2	3	8	9	10

TRANSFORM CHARACTERISTICS

- 16-Point (N = 16)
- RADIX-2
- Normally ordered output data (Unique input data order)
- DIF
- In-place
- Real valued output data
- Inverse Transform

TYPICAL BUTTERFLIES

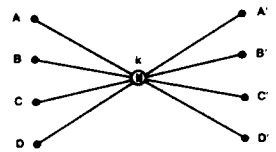
$KNZ/\overline{KZ}$ = LOW
(k = 0)



DFR00600

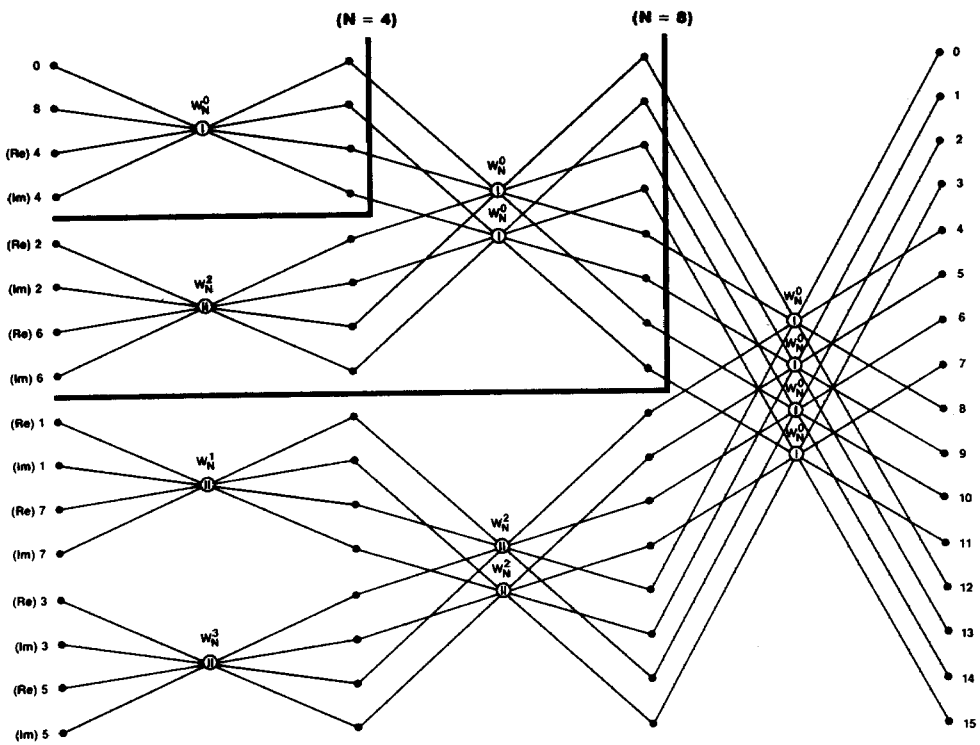
$A' = Re\ [A + jB + C - jD]$
$B' = Im\ [A + jB + C - jD]$
$C' = Re\ [(A + jB - C + jD)W_N^0]$
$D' = Im\ [(A + jB - C + jD)W_N^0]$
$W_N = ej^{2\pi/N}$

$KNZ/\overline{KZ}$ = HIGH
(k = 0)



DFR00610

$A' = Re\ [A + jB + C - jD]$
$B' = Re\ [(A + jB - C + jD)W_N^k]$
$C' = Im\ [A + jB + C - jD]$
$D' = Im\ [(A + jB - C + jD)W_N^k]$
$W_N = ej^{2\pi/N}$



DFR00480

DIT/$\overline{DIF}$	$\overline{PSD}$	RADIX 4/$\overline{2}$
L	L	L

Address of	A	B	C	D	A'	B'	C'	D'	W_N^k
AS =	12	13	14	15	12	13	14	15	8

03567C

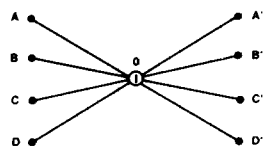
Refer to Page 13-1 for Essential Information on Military Devices

TRANSFORM CHARACTERISTICS

- 16-Point (N = 16)
- RADIX-2
- DIT
- Normally ordered input data (Unique output data order)
- In-place
- Real Valued Input (RVI) data
- Forward Transform

TYPICAL BUTTERFLIES

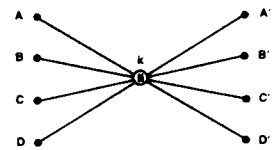
KNZ/$\overline{KZ}$ = LOW
(k = 0)



DFR00600

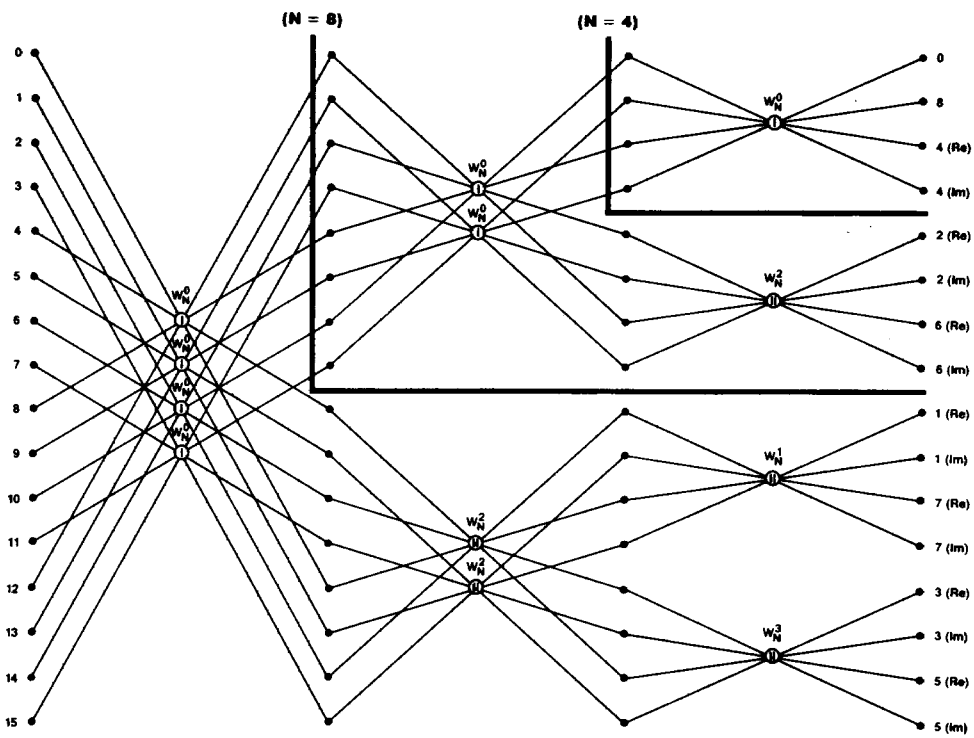
$A' = Re\ [A + jB + (C + jD)W_N^0]$
$B' = Im\ [A + jB + (C + jD)W_N^0]$
$C' = Re\ [A + jB - (C + jD)W_N^0]$
$D' = Im\ [-A - jB + (C - jD)W_N^0]$
$W_N = e^{\frac{-j2\pi}{N}}$

KNZ/$\overline{KZ}$ = HIGH
(k ≠ 0)



DFR00610

$A' = Re\ [A + jC + (B + jD)W_N^k]$
$B' = Im\ [A + jC + (B + jD)W_N^k]$
$C' = Re\ [A + jC - (B - jD)W_N^k]$
$D' = Im\ [-A - jC + (B + jD)W_N^k]$
$W_N = e^{\frac{-j2\pi}{N}}$



DFR00490

DIT/$\overline{DIF}$	$\overline{PSD}$	RADIX 4/$\overline{2}$
H	H	L

Address of	A	B	C	D	A'	B'	C'	D'	W_N^k
AS =	12	13	14	15	12	13	14	15	8