Document Title

256K X 8 OTP CMOS EPROM

Revision History

Rev. No.	History	Issue Date	Remark
0.0	Initial issue	March 10, 2005	Preliminary
0.1	Modify the program power supply	June 16, 2005	

A27020A Series

Preliminary — 256K X 8 OTP CMOS EPROM

Features

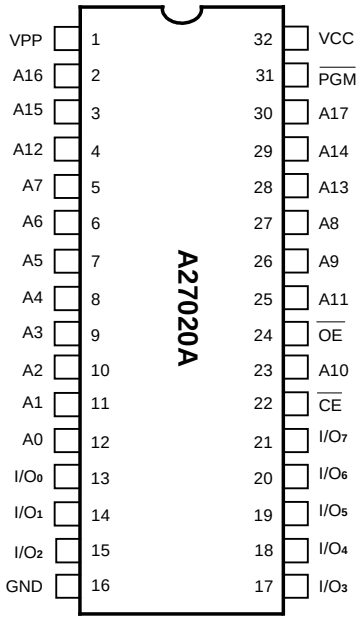
- 262,144 X 8 bit organization
- Programming voltage: 12.25V
- Access time: 55/70 ns (max.)
- Current: Operating: 30mA (max.) at 5MHz
  Standby: 100μA (max.)
- All inputs and outputs are directly TTL-compatible
- Available in 32-pin DIP and 32-pin PLCC packages

General Description

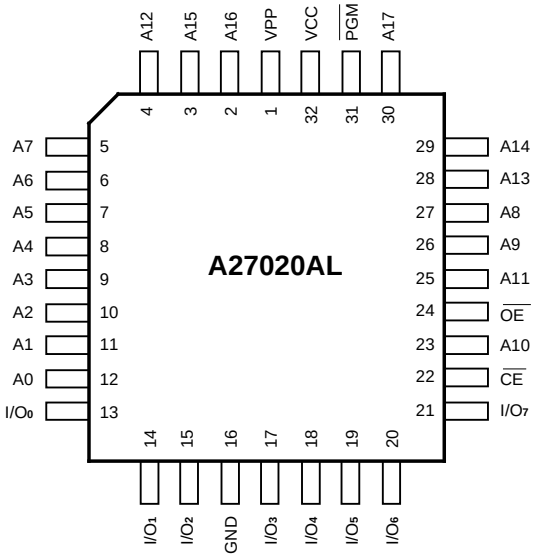
The A27020A chip is a high-performance 2,097,152 bit one-time programmable read only memory (OTP EPROM) organized as 256K by 8 bits. The A27020A requires only 5V power supply in normal read mode operation and any input signals are TTL levels. The A27020A is available in industry standard 32 pin dual-in-line and 32 pin PLCC packages.

Pin Configurations

■ **DIP**



■ **PLCC**



Pin Configurations

Pin Name	Function
A0-A17	Address Inputs
I/O_7-I/O_0	Data Inputs / Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{PGM}$	Program Strobe
VPP	Program Power Supply
VCC	Power Supply
GND	Ground

Operating Modes and Truth Table

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	A0	A1	A9	VPP	VCC	I/O_7-I/O_0
Read	V_{IL}	V_{IL}	X	X	X	X	VCC	VCC	Data Out
Output Disable	V_{IL}	V_{IH}	X	X	X	X	VCC	VCC	Hi-Z
Standby	V_{IH}	X	X	X	X	X	VCC	VCC	Hi-Z
Program	V_{IL}	V_{IH}	V_{IL} Pulse	X	X	X	12.25V	5.25V	Data In
Program Verify	V_{IL}	V_{IL}	V_{IH}	X	X	X	12.25V	5.25V	Data Out
Program Inhibit	V_{IH}	X	X	X	X	X	12.25V	5.25V	Hi-Z
Manufacturer Code(3)	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{ID}	VCC	VCC	37H
Device Code(3)	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{IL}	V_{ID}	VCC	VCC	64H
Continuation Code(3)	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{ID}	VCC	VCC	7FH

Notes:
1. X = Either V_{IH} or V_{IL}.
2. V_{ID} = 12V ± 0.5V.
3. A2 ~ A8 = A10 ~ A17 = V_{IL} (For auto identification)

Functional Description

Read Mode

The A27020A has two control functions, both of which must be logically active in order to obtain data at the outputs. $\overline{CE}$ is the power control and should be used for device selection. $\overline{OE}$ is the output control and should be used to data to the output pins, which is independent of device selection. Assuming that addresses are stable, address access time (t_{AA}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the output after a delay (t_{OE}) from the falling edge of $\overline{OE}$, as long as $\overline{CE}$ has been low and the addresses have been stable for at least $t_{ACC} - t_{OE}$.

Standby Mode

The A27020A has a standby mode which reduces the active current from 30mA to 100μA. The A27020A is placed in the standby mode by applying a CMOS high signal to $\overline{CE}$. When in the standby mode, the output are in a high impedance state, independent of the $\overline{OE}$.

Auto Identify Mode

The auto identify mode allows the reading out of a binary code from a EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm.

To activate the mode, the programming equipment must apply 12.0V ± 0.5V on address line A9 of the A27020A. Three identification code can be read from data output pin by toggling A0 and A1. The other addresses must be held at V_{IL} during this mode. Byte 0 (with A0 at V_{IL}, A1 at V_{IL}) represents the manufacturer code which is 37H. Byte 1 and Byte 2 represent the device code and continuation code, which is 64H and 7FH respectively. All identifiers for these codes will possess odd parity, with MSB (IO_7) defined the parity bit.

Absolute Maximum Ratings*

Ambient Operating Temperature (T_A) . . ..-10°C to +85°C
Storage Temperature Plastic Package (T_{STG}) . . . . . .
. . . . -55°C to 125°C
Applied Input Voltage (V_I):
All Pins Except A9, VPP and VCC . . . . . .
. . . . . -0.6V to VCC + 0.6V
A9, VPP . . . . . -0.6V to 12.5V
VCC . . . . . -0.6V to 7.0V
Output Voltage (V_O) . . . . . -0.6V to 6.0V (Note 1)

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

Notes:
1. During voltage transitions, the input may undershoot GND to -2.0V for periods less than 20 ns. Maximum DC voltage on input and I/O may overshoot to VCC + 2.0V for periods less than 20 ns.
2. When transitions, A9 and VPP may undershoot GND to -2.0V for periods less than 20 ns. Maximum DC input voltage on A9 and VPP is +12.5V which may overshoot to 12.7V for period less than 20 ns.

Read Mode DC Electrical Characteristics (Ta = 0°C to 70°C, VCC = 5V ± 10%, VPP = VCC)

Symbol	Parameter	Min.	Max.	Unit	Conditions
V_{OH}	Output High Voltage	2.4		V	I_{OH} = -400μA
V_{OL}	Output Low Voltage		0.4	V	I_{OL} = 2.1mA
V_{IH}	Input High Voltage	2.0	VCC + 0.5	V	
V_{IL}	Input Low Voltage	-0.5	0.8	V	
I_{LI}	Input Leakage Current	-1	+1	μA	VCC = max. Vin = 0V to VCC
I_{LO}	Output Leakage Current	-1	+1	μA	VCC = max. Vout = 0V to VCC
I_{CC}	VCC Read Operating Current		30	mA	VCC = max. $\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IL} Iout = 0mA, at 5MHz
I_{SB}	VCC Standby Current (TTL)		1	mA	VCC = max. $\overline{CE}$ = V_{IH}
I_{SB1}	VCC Standby Current (CMOS)		100	μA	VCC = max. $\overline{CE}$ = VCC - 0.2V
I_{PP}	VPP Current During Read		10	μA	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, VPP = VCC
I_{ID}	A9 Auto Select Current		100	μA	A9 = V_{ID}, VCC = max.

Capacitance (T_A = 25°C, f = 1.0MHz)

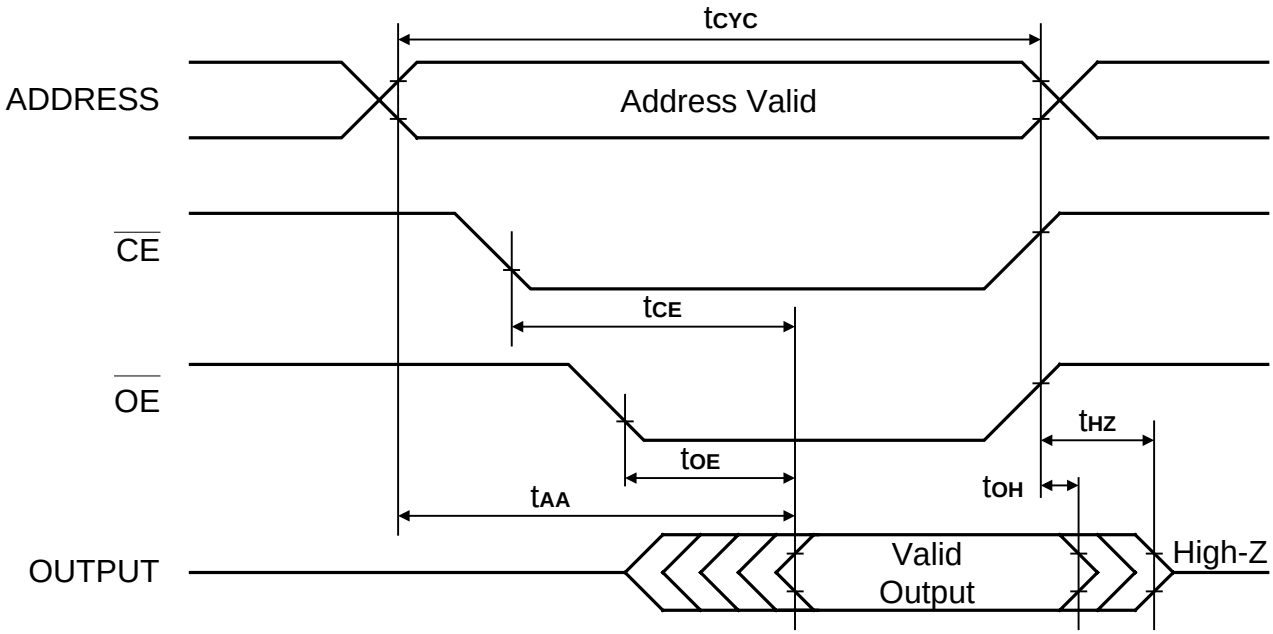
Symbol	Parameter	Min.	Max.	Unit	Conditions
C_{IN}	Input Capacitance		8	pF	V_{IN} = 0V
C_{out}	Output Capacitance		8	pF	V_{out} = 0V

* These parameters are sampled and not 100% tested.

Read Mode AC Characteristics (Ta = 0°C to 70°C, VCC = 5V ± 10%, VPP = VCC)

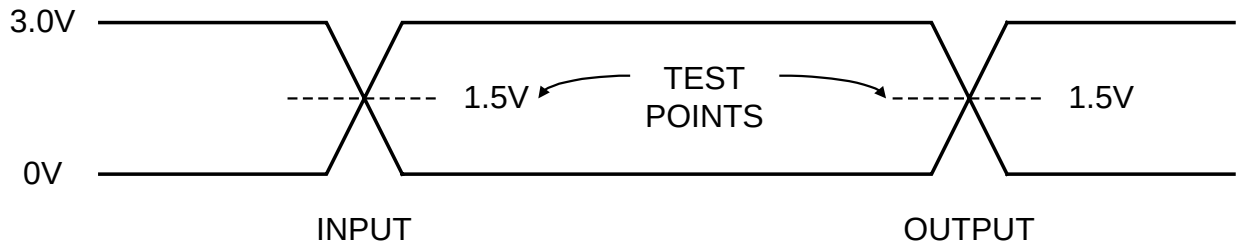
Symbol	Parameter	55ns		70ns		Unit
		Min.	Max.	Min.	Max.	
t_{CYC}	Cycle Time	55		70		ns
t_{AA}	Address Access Time		55		70	ns
t_{CE}	Chip Enable Access Time		55		70	ns
t_{OE}	Output Enable Access Time		30		35	ns
t_{OH}	Output Hold after Address, $\overline{CE}$ or $\overline{OE}$, whichever Occurred First	0		0		ns
t_{HZ}	Output High Z Delay		20		20	ns

Read Mode Switching Waveforms

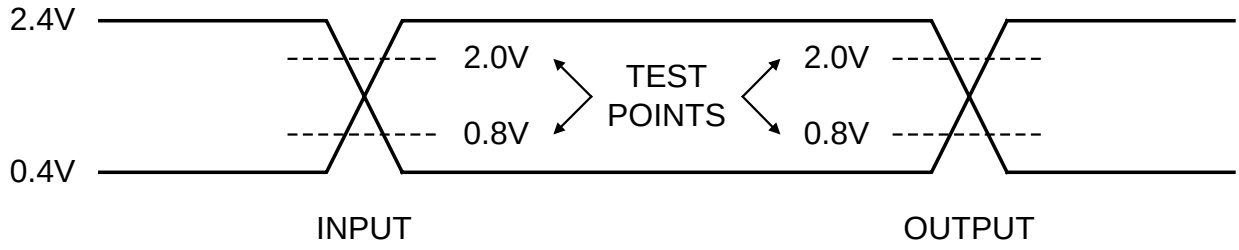


AC Measurement Conditions

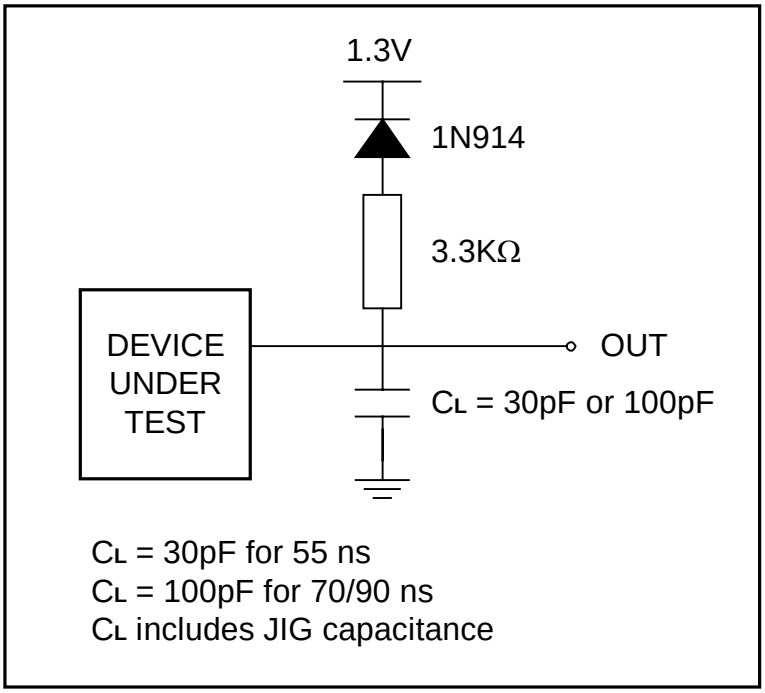
for 55 ns ① Input Rise and Fall Times ≤ 10 ns
② Input Pulse Voltage: 0V to 3Volt
③ Input and Output Timing Ref. Voltage: 1.5Volt



for 70 ns ① Input Rise and Fall Times ≤ 10 ns
② Input Pulse Voltage: 0.4V to 2.4Volt
③ Input and Output Timing Ref. Voltage: 0.8V to 2.0Volt



AC Testing Load Circuit



Programming and Program Verify

The programming flowchart is shown in Page 10.

The A27020A is shipped with all bits being set to "1". Programming causes relevant bits to be changed to "0". The programming mode is started by setting VCC to +5.25V and VPP to +12.25V, while $\overline{CE}$ and $\overline{PGM}$ are at V_{IL}, and $\overline{OE}$ is at V_{IH}. Data to be programmed can be directly input in the 8 bit format through the data bus.

The write programming algorithm reduces programming time by using 100μs pulse followed by a byte verification to determine whether the byte has been successfully programmed. If the data does not pass the verification, an additional pulse programming is applied for a maximum of 25 pulses. On completion of 1 byte programming and, The verified address is incremented. After the final address is completed, all bytes are verified again with VCC = 5.0 Volt.

Program Inhibit

This mode is used to program one of multiple A27020A whose $\overline{OE}$, $\overline{PGM}$, VPP, VCC, address bus and data bus are connected in parallel. When programming is performed, other A27020A can be inhibited from being programmed by setting their $\overline{CE}$ pins to V_{IH}.

Programming Mode DC Characteristics (Ta = 0°C to 70°C, VCC = 5.25V ± 0.25V, VPP = 12.25V ± 0.25V)

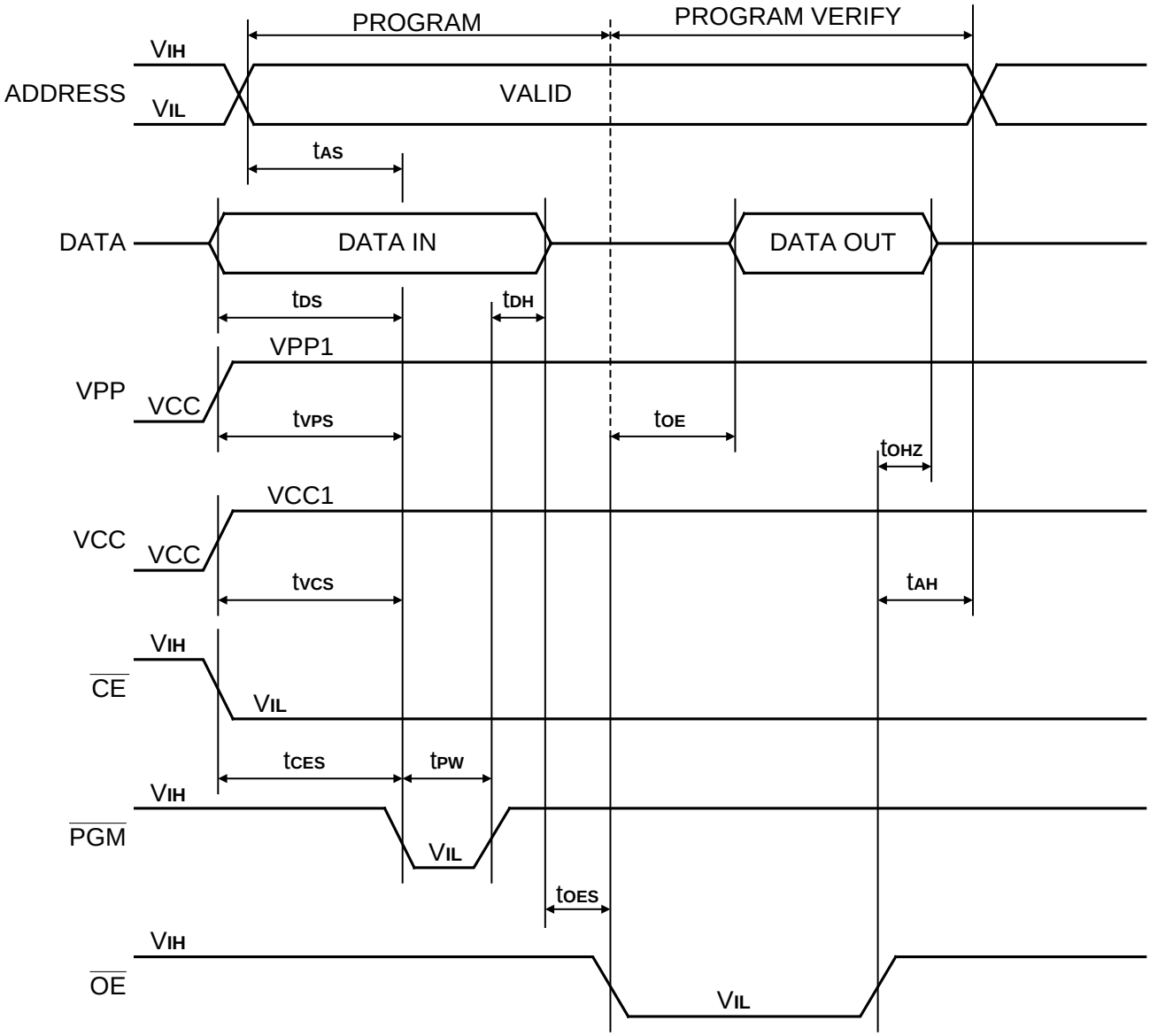
Symbol	Parameter	Min.	Max.	Unit	Test Conditions
V_{OH}	Output High Voltage	2.4		V	I_{OH} = -400μA
V_{OL}	Output Low Voltage		0.4	V	I_{OL} = 2.1mA
V_{IH}	Input High Voltage	2.0	VCC + 0.5	V	
V_{IL}	Input Low Voltage	-0.5	0.8	V	
I_{LI}	Input Leakage Current	-1	+1	μA	VCC = max. Vin = 0V to VCC
I_{CC}	VCC Current During Program		50	mA	
I_{PP}	VPP Current During Program		50	mA	$\overline{CE}$ = V_{IL}
V_{ID}	A9 Auto Select Voltage	11.5	12.5	V	A9 = V_{ID}
VCC1	Programming Supply Voltage	5.0	5.5	V	
VPP1	Programming Voltage	12.0	12.5	V	

Note: VCC must be applied simultaneously or before VPP and removed simultaneously or after VPP.

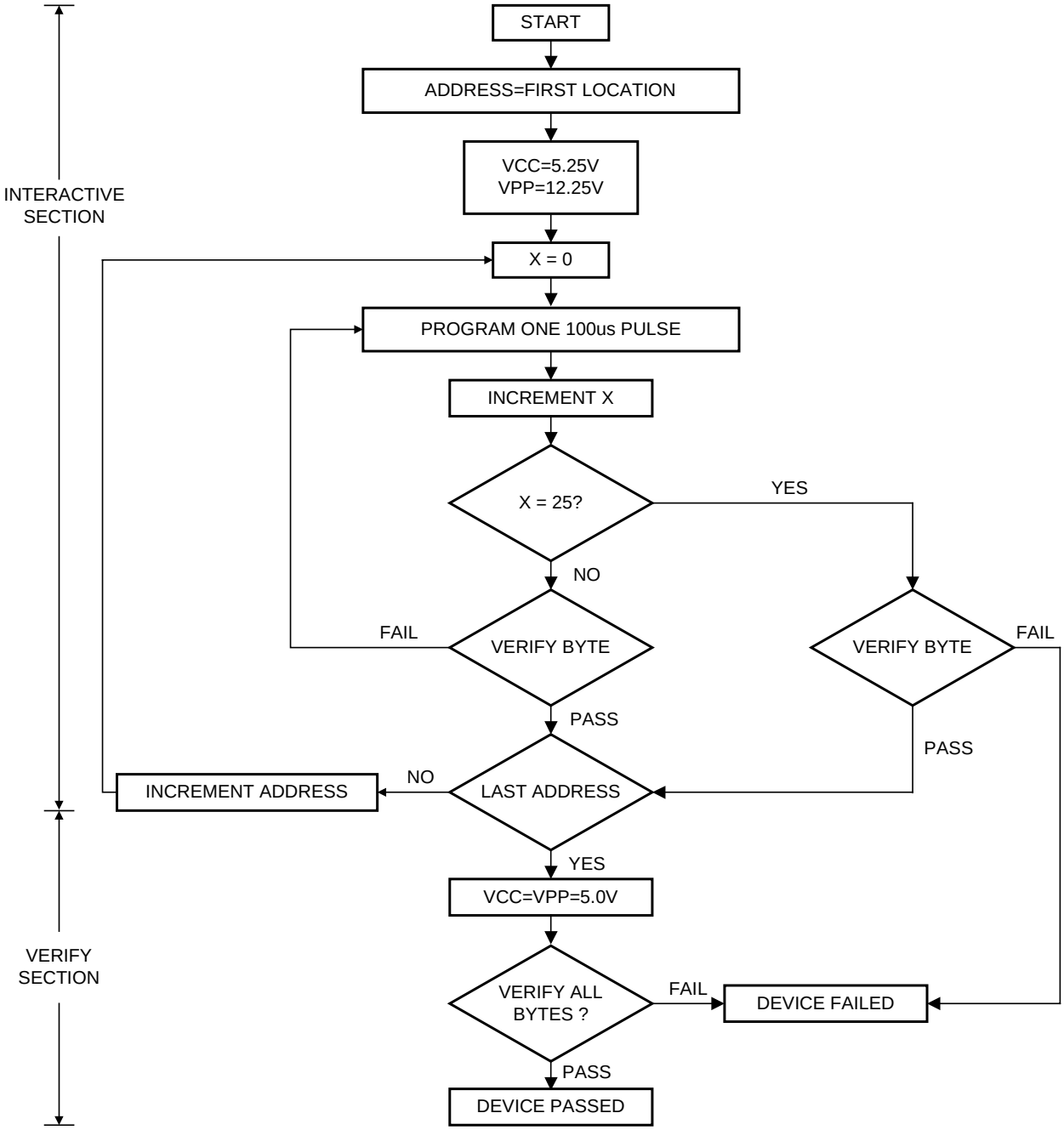
Programming Mode AC Characteristics (Ta = 0°C to 70°C, VCC= 5.25V ± 0.25V, VPP = 12.25V ± 0.25V)

Symbol	Parameter	Min.	Max.	Unit
t_{AS}	Address Valid to Program Low	2		µs
t_{DS}	Input Valid to Program Low	2		µs
t_{VPS}	VPP High to Program Low	2		µs
t_{VCS}	VCC High to Program Low	2		µs
t_{CES}	$\overline{CE}$ Low to Program Low	2		µs
t_{PW}	Program Pulse Width	95	105	µs
t_{DH}	Program High to Input transition	2		µs
t_{OES}	Input Transition to $\overline{OE}$ Low	2		µs
t_{OE}	$\overline{OE}$ Low to Output Valid		100	ns
t_{OHZ}	$\overline{OE}$ High to Output Hi-Z		130	ns
t_{AH}	$\overline{OE}$ High to Address Transition	0		ns

Programming and Verify Mode AC Waveforms



Programming Flowchart



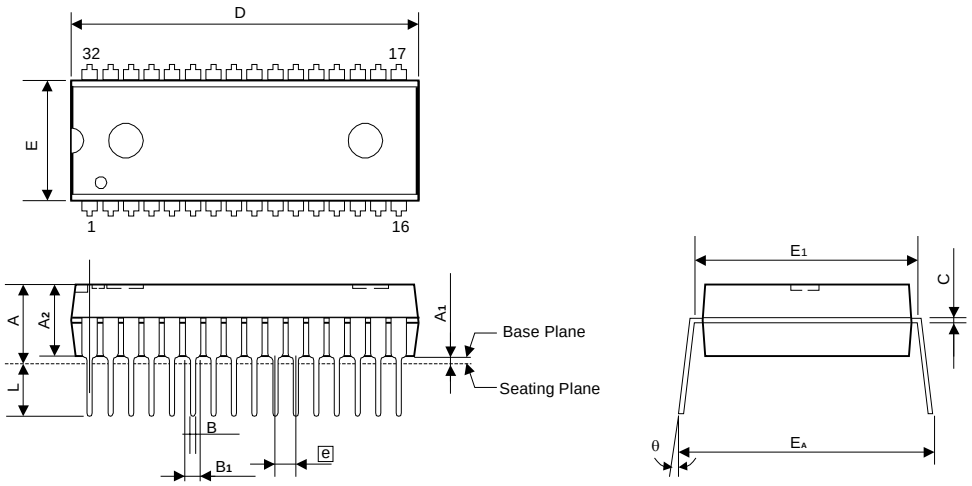
Ordering Information

Part No.	Access Time (ns)	Operating Current Max. (mA) at 5MHz	Standby Current Max. (μA)	Package
A27020A-55	55	30	100	32Pin DIP
A27020A-55F	55	30	100	32Pin Pb-Free DIP
A27020AL-55	55	30	100	32Pin PLCC
A27020AL-55F	55	30	100	32Pin Pb-Free PLCC
A27020A-70	70	30	100	32Pin DIP
A27020A-70F	70	30	100	32Pin Pb-Free DIP
A27020AL-70	70	30	100	32Pin PLCC
A27020AL-70F	70	30	100	32Pin Pb-Free PLCC

Package Information

P-DIP 32L Outline Dimensions

unit: inches/mm



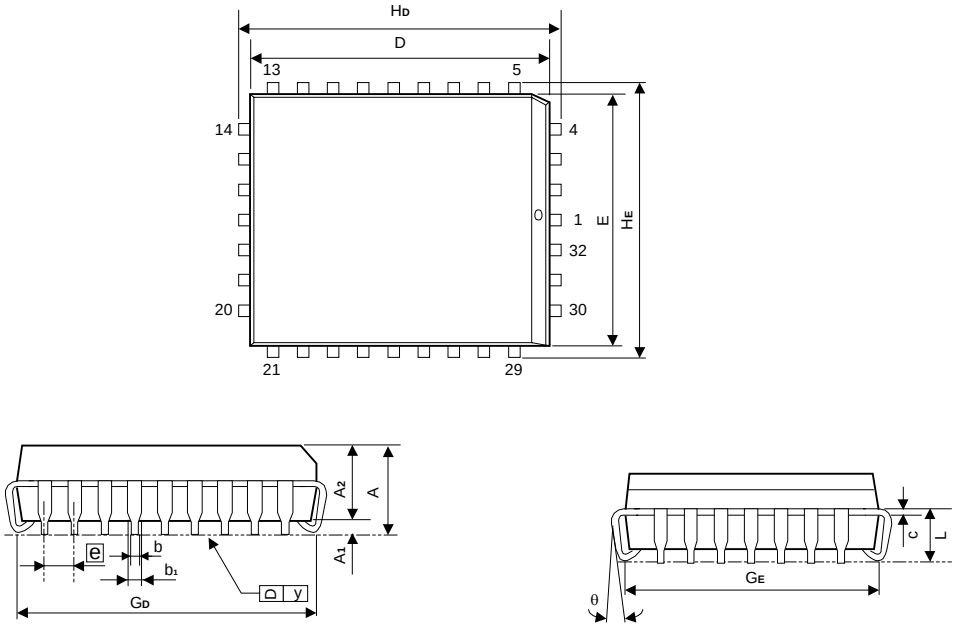
Symbol	Dimensions in inches			Dimensions in mm		
	Min	Nom	Max	Min	Nom	Max
A	-	-	0.210	-	-	5.334
A_1	0.015	-	-	0.381	-	-
A_2	0.149	0.154	0.159	3.785	3.912	4.039
B	-	0.018	-	-	0.457	-
B_1	-	0.050	-	-	1.270	-
C	-	0.010	-	-	0.254	-
D	1.645	1.650	1.655	41.783	41.91	42.037
E	0.537	0.542	0.547	13.64	13.767	13.894
E_1	0.590	0.600	0.610	14.986	15.240	15.494
E_A	0.630	0.650	0.670	16.002	16.510	17.018
e	-	0.100	-	-	2.540	-
L	0.120	0.130	0.140	3.048	3.302	3.556
θ	0°	-	15°	0°	-	15°

Notes:
1. The maximum value of dimension D includes end flash.
2. Dimension E does not include resin fins.

Package Information

PLCC 32L Outline Dimension

unit: inches/mm



Symbol	Dimensions in inches			Dimensions in mm		
	Min	Nom	Max	Min	Nom	Max
A	-	-	0.134	-	-	3.40
A_1	0.0185	-	-	0.47	-	-
A_2	0.105	0.110	0.115	2.67	2.80	2.93
b_1	0.026	0.028	0.032	0.66	0.71	0.81
b	0.016	0.018	0.021	0.41	0.46	0.54
C	0.008	0.010	0.014	0.20	0.254	0.35
D	0.547	0.550	0.553	13.89	13.97	14.05
E	0.447	0.450	0.453	11.35	11.43	11.51
e	0.044	0.050	0.056	1.12	1.27	1.42
G_D	0.490	0.510	0.530	12.45	12.95	13.46
G_E	0.390	0.410	0.430	9.91	10.41	10.92
H_D	0.585	0.590	0.595	14.86	14.99	15.11
H_E	0.485	0.490	0.495	12.32	12.45	12.57
L	0.075	0.090	0.095	1.91	2.29	2.41
y	-	-	0.003	-	-	0.075
θ	0°	-	10°	0°	-	10°

Notes:
1. Dimensions D and E do not include resin fins.
2. Dimensions G_D & G_E are for PC Board surface mount pad pitch design reference only.