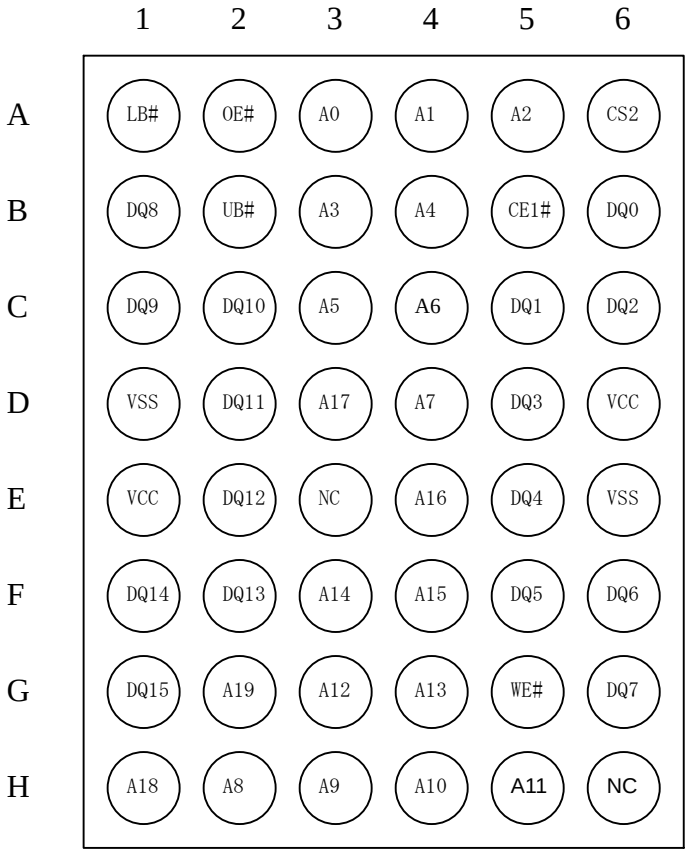
Features

- Memory cell : Dynamic memory(DRAM)
- Refresh: Completely free
- Power Down: Control by CS2(No Data Retention)
- Byte Control : Capable of single byte operation
- Power Consumption: 70 μ A(Standby Current)
- Operating Temperature Range: -30'C~+85'C
- Composition:1,048,576Word X 16 Bit
- Supply Power Voltage:2.70V to 3.30V
- Access Time: 70nS
- Access Time (Page Access Read): 30nS
- I/O Terminal :Input / Output Common 3-state output



Pin Description

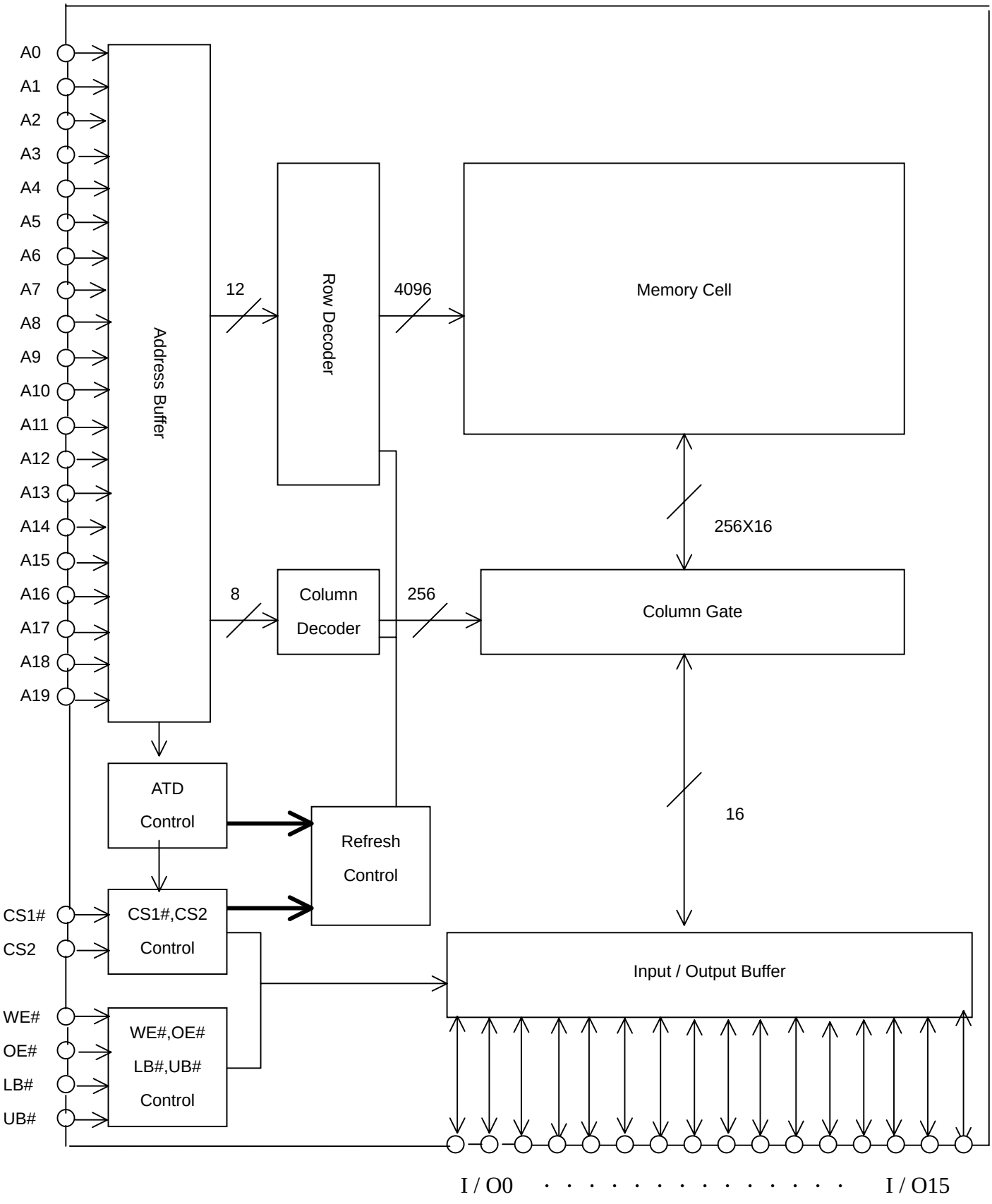
Pin Name	Description
CS1#	Chip select 1 (Low Active)
CS2	Chip select 2 (High Active)
WE#	Write enable (Low Active)
OE#	Output enable (Low Active)
A0 to A19	Address Input (A0 to A1 : Page Address)
IO0-7	Lower Byte Input / Output
IO8-15	Upper Byte Input / Output
LB#	Lower Byte Control (Low Active)
UB#	Upper Byte Control (Low Active)
VCC	Power Supply
VSS	Ground (0V)

Description

A64S06161 is a virtually static RAM, which uses DRAM type memory cells, but it has refresh transparency, so that you need not to imply refresh operation. Furthermore the interface is completely compatible to a low power Asynchronous type SRAM, you can operate as same as the Asynchronous SRAM.

A64S06161 is a 1,048,576 Words X 16 bit asynchronous random access memory on a monolithic CMOS chip with marvelous low power consumption technology. Its low power and also low noise makes it ideal for mobile applications.

Block Diagram



Functions

Truth Table

A0-19	CS1#	CS2	WE#	OE#	LB#	UB#	I/O0~7	I/O8~15	Mode
V	L	H	H	L	L	L	Data-Out	Data-Out	Read
V	L	H	H	L	L	H	Data-Out	High-Z	Read
V	L	H	H	L	H	L	High-Z	Data-Out	Read
V	L	H	H	X	H	H	High-Z	High-Z	Output Disable
V	L	H	H	H	X	X	High-Z	High-Z	Output Disable
V	L	H	L	H	L	L	Data-In	Data-In	Write
V	L	H	L	H	L	H	Data-In	High-Z	Write
V	L	H	L	H	H	L	High-Z	Data-In	Write
X	H	H	X	X	X	X	High-Z	High-Z	Standby
X	X	L	X	X	X	X	High-Z	High-Z	Power Down*1

V : Valid Address. X : High or Low .*1 No Data Retention

Read Operation

It is possible to control data width by LB# and UB# pins.

(1)Reading data from lower byte

Date can be read when the address is set while holding CS1#=L, CS2=H, OE #=L , WE #= H and LB #=L.

(2)Reading data from upper byte

Date can be read when the address is set while holding CS1#=L, CS2=H, OE #=L , WE #= H and UB #=L.

(3)Reading date from both bytes

Date can be read when the address is set while holding CS1#=L, CS2=H, OE #=L , WE #= H , LB #=L and UB #=L.

(4)Page access read

Date can be read by changing A0-A1 when A2-A19 is set while holding CS1#=L, CS2 #=H, WE #=H, OE #=L, LB #=L and UB #=L.

Writing Operation

(1) Writing data into lower byte (WE # control)

Data can be written by adding L pulse into WE # when the address is set while holding CS1#=L, CS2=H, OE #=H, LB #=L and UB #=H.

The data on lower byte are latched up into the memory cell during WE # =L and LB # =L.

(2) Writing data into lower byte (LB # control)

Data can be written by adding L pulse into LB # when the address is set while holding CS1#=L, CS2 =H, OE#=H, UB# =H and WE#=L.

The data on lower byte are latched up into the memory cell during WE# =L and LB# = L.

(3) Writing data into upper byte (WE # control)

Data can be written by adding L pulse into WE # when the address is set while holding CS1 #=L, CS2 =H, OE #=H, LB # =H and

UB #=L.

The data on upper byte are latched up into the memory cell during WE # =L and UB # = L.

(4) Writing data into upper byte (UB # control)

Data can be written by adding L pulse into UB # when the address is set while holding CS1 #=L, CS2 =H, OE #=H, LB # =H and WE #=L.

The data on upper byte are latched up into the memory cell during WE #=L and UB #=L.

(5) Writing data into both byte (WE # control)

Data can be written by adding L pulse into WE # when the address is set while holding CS1 #=L, CS2=H, OE #=H, LB #=L and UB #=L.

The data are latched up into the memory cell during WE #=L, LB #=L and UB #=L.

(6) Writing data into both byte (LB #, UB # control)

Data can be written by adding L pulse into LB# and UB# when the address is set while holding CS1#=L, CS2=H, OE #=H and WE #=L.

The data are latched up into the memory cell during WE #=L, LB #=L and UB #=L

Read or write with using both LB # and UB #, the timing edge of LB # and UB # must be same.

While I/O pins are in the output state, the data that is opposite to the output data should not be given.

Standby cycle

When CS1# is H, the device will be in the standby cycle. In this case data I/O pins are Hi-Z and all input pins are inhibited.

Power Down

When CS2 is L, the device will be in the power down. In this case, an internal refresh stops and the data might be lost.

ABSOLUTE MAXIMUM RATINGS (VSS=0V)

Parameter	Symbol	Ratings	Unit
Supply voltage	VCC	-0.5 to 3.6	V
Input voltage	VI	-0.5* to VCC+0.3	V
Input / Output voltage	V I/O	-0.5* to VCC+0.3	V
Input / Output voltage	PD	0.5	W
Operating temperature	Topr	-30 to 85	’C
Storage temperature	Tstg	-65 to 150	‘C

* If pulse width is less than 5ns it is – 1.0V

ELECTRICAL CHARACTERISTICS

DC Recommended Operating Conditions (Ta=-30~85’ C)

Parameter	Symbo1	Min	Max	Unit
Supply voltage	VCC	2.70	3.30	V
	VSS	0	0	V
Input voltage	VIH	VCC-0.3	VCC+0.3	V
	VIL	-0.3*	0.3	V

* If pulse width is less than 5ns it is －1.0V

DC ELECTRICAL CHARACTERISTICS

DC Characteristics (Ta=-30~85’C)

Parameter	Symbol	Condition	Min	Typ*1	Max	Unit
Input leakage current	ILI	VI=0V to VCC	-1	－	1	μA
Output leakage current	ILO	LB and UB=H or CS1=H or WE=L or OE=H or CS2=L VI/O=0V to VCC	-1	－	1	μA
High level output voltage	VOH	IOH=-0.5mA	Vcc-0.3	－	－	V
Low level output voltage	VOL	IOL=0.5mA	－	－	0.3	V
Power Down Current	IDDPD	CS2≦0.2V	－	－	25	μA
Standby Current	IDDS	VCC-0.2V≦CS1	－	50	70	μA
Operating current	IDDA1	I I/O=0mA, tcyc=70nS	－	15	20	mA
		I I/O=0mA, tcyc=1uS	－	2.5	3	mA

*1:Typical values are measured at Ta=25’C and VCC =3.0V

Terminal Capacitance

(Ta=25’C f=1MHz)

Parameter	Symbol	Conditions	Min	Max	Unit
Input Capacitance	CI	VI=0V	－	8	pF
I/O Capacitance	C I/O	V I/O=0V	－	10	pF

Note：This parameter is measured by sampling , not of all products.

AC Electrical Characteristics

Read Cycle (Ta = - 30 ~ 85'C)

Parameter	Symbol	Teat Conditions	Min	Max	Unit
Read cycle time	tRC	1	70	32000	nS
Page read cycle time	tRCP	1	30	32000	nS
Address access time	tACC	1	-	70	nS
Page address access time	tACCP	1	-	30	nS
CS1 # access time	tACS	1	-	70	nS
OE # access time	tOE	1	-	40	nS
LB # , UB # access time	tAB	1	-	25	nS
Address set up to OE L #	tASO	1	-5	-	nS
Address set up to CS1 # L	tASC	1	0	-	nS
Address hold time from CS1 #L	tAHC	1	0	-	nS
CS1# high pulse width	tC1H	1	30	-	nS
CS1 # output set time	tCLZ	2	0	-	nS
CS1 # output floating time	tCHZ	2	-	15	nS
LB # , UB # output set time	tBLZ	2	0	-	nS
LB # , UB # output floating tine	tBHZ	2	-	15	nS
OE # output set time	tOLZ	2	0	-	nS
OE # output floating time	tOHZ	2	-	15	nS
Output hold time	tOH	1	5	-	nS

Write Cycle (Ta= - 30~85'C)

Parameter	Symbol	Test Conditions	Min	Max	Unit
Write cycle time	tWC	1	70	32000	nS
Chip select time	tCW	1	60	-	nS
Address enable time	tAW	1	60	-	nS
Address set up to CS1 # L	tASC	1	0	-	nS
Address hold time from CS1 # H	tAHC	1	0	-	nS
Address set up time	tAS	1	0	-	nS
Write pulse width	tWP	1	40	-	nS
LB,UB select time	tBW	1	60	-	nS
Address hold time	tWR	1	0	-	nS
Data set up time	tDW	1	30	-	nS
Data hold time	tDH	1	0	-	nS

Power Down Cycle(Ta= - 30~85’ C)

Parameter	Symbol	Test Conditions	Min	Max	Unit
CS1 # H set up time for Power Down entry	tSSP	1	0	-	nS
CS1 # H hold time before Power Down exit	tSHP	1	0	-	nS
CS2 L pulse width	TC2LP	1	30	-	nS
CS1 # H hold time after Power Down exit	tHPD	1	300	-	µS

Power Up Timing Requirement(Ta= - 30~85’ C)

Parameter	Symbol	Test Conditions	Min	Max	Unit
CS1 # CS2 set up time after Power Up	tSHU	1	0	-	nS
Standby hold time after Power Up	tHPU	1	300	-	µS

Data Retention Timing Requirement(Ta= - 30~85’ C)

Parameter	Symbol	Test Conditions	Min	Max	Unit
A2 to A19 hold time during active	tBAH	1	0	-	nS
CS1# L hold time for A2 to A19 fix	tCSH	1	300	-	µS

Either tBAH or tCSH required for data retention.

Address Skew Timing Requirement(Ta= - 30~85’ C)

Parameter	Symbol	Test Conditions	Min	Max	Unit
Maximum address skew	tSKEW	1	-	10	nS

Configuration Register

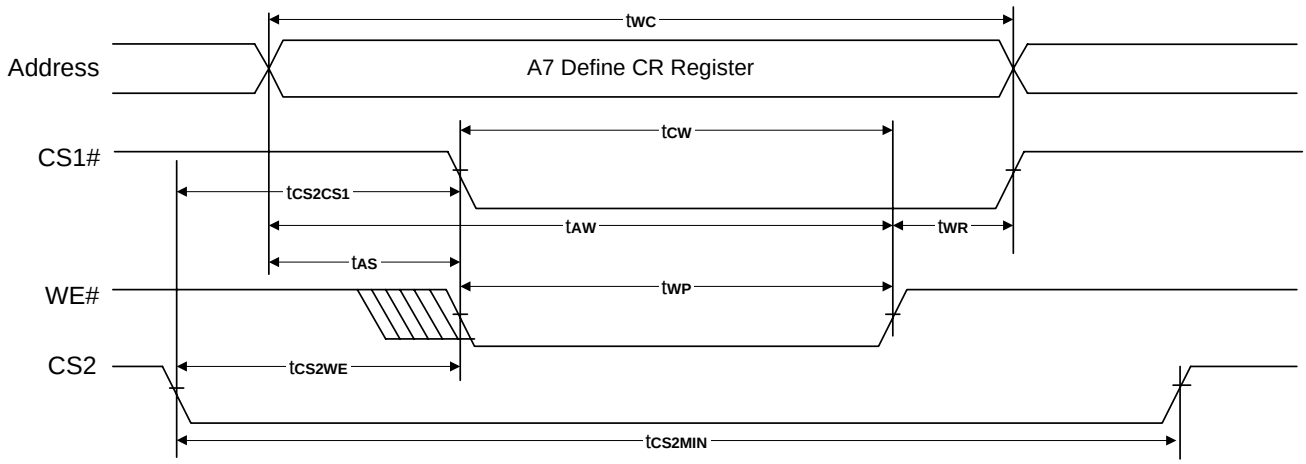
The configuration register (CR) defines how the A64S06161 operates and whether page mode read accesses are permitted. The register is automatically loaded with default setting during power on and can be updated anytime while the device is operating in a normal state.

CR Register Description

Reserved	PAGE	Reserved
A19 – A8	A7	A6 – A0

Bit(s)	Name	Reserved
A19 – A8, A6 – A0	Reserved	Reserved, All must be set to “0”
A7	Page Mode on/off	0 - Page Mode Disabled (Default) 1 - Page Mode Enabled

CR Register Update – Timing Waveform



CR register update–Timing waveform

Notes:

1. VIH(max) = VCCQ + 0.2V for pulse durations less than 20ns.
2. VIL(min) = -1V for pulse duration less than 20ns.
3. Overshoot and undershoot specifications are characterized and are not 100% tested.
4. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at VCC = VCC(typ.) and T_A = 25°C.

CR Register Timings

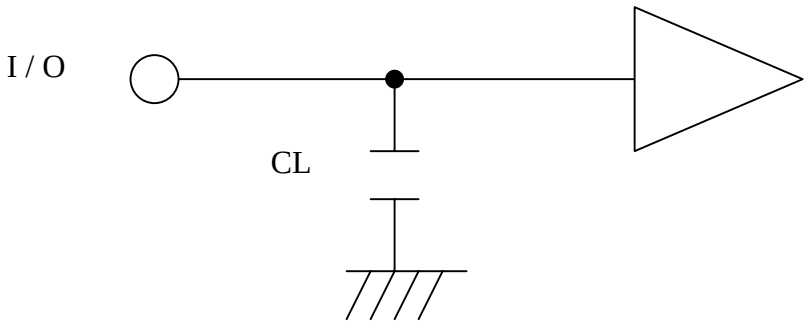
Parameter	Description	Min.	Max.	Unit
t_{CS2WE}	CS2 LOW to WE# LOW		1000	ns
t_{CS2MIN}	Deep Power Down Mode Time	32000		ns
t_{CS2CS1}	CS2 LOW to CE# LOW	0	1000	ns

TEST CONDITION 1

Input pulse voltage level	VCC – 0.3V / 0.3V
Input ascend / descend time	tr=tf=3nS
Input output timing reference level	1/2VCC
Output load	CL=50pF(Includes Jig capacity)+1TTL

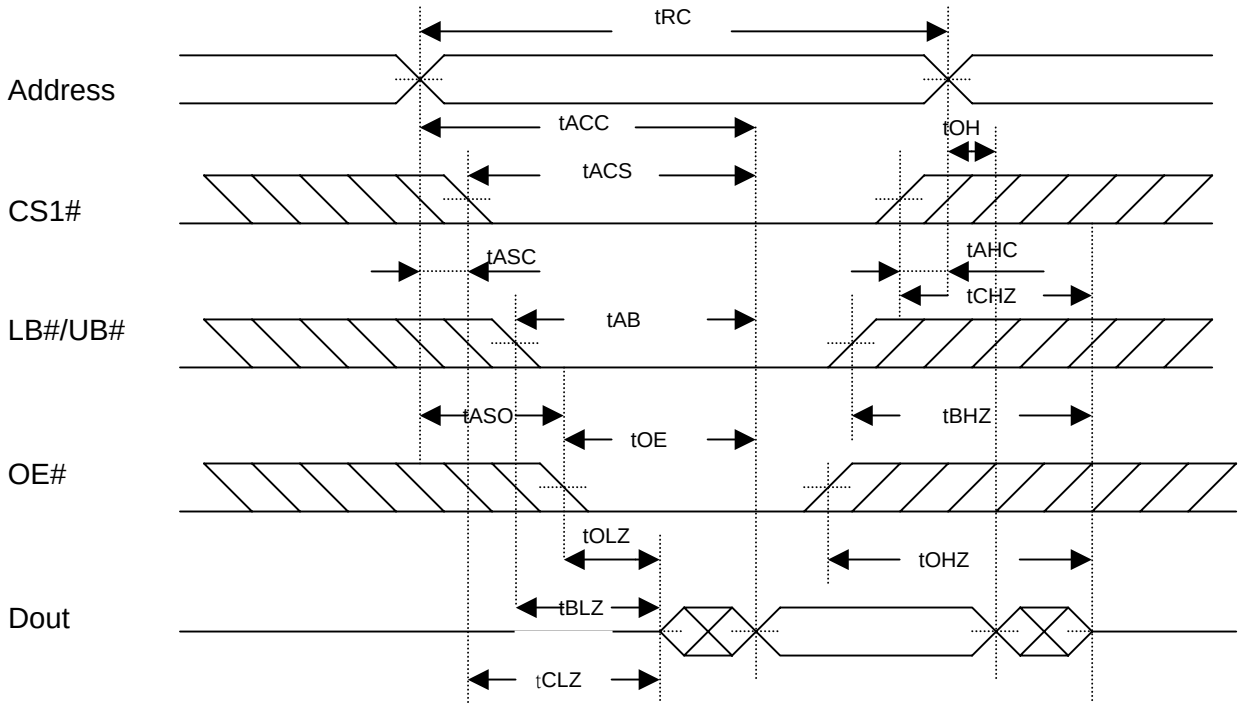
TEST CONDITION 2

Input pulse voltage level	VCC – 0.3V / 0.3V
Input ascend / descend time	tr=tf=3nS
Input output timing reference level	±100mV(The level change from stable voltage
Output load	CL=5pF(Includes Jig capacity)+1TTL



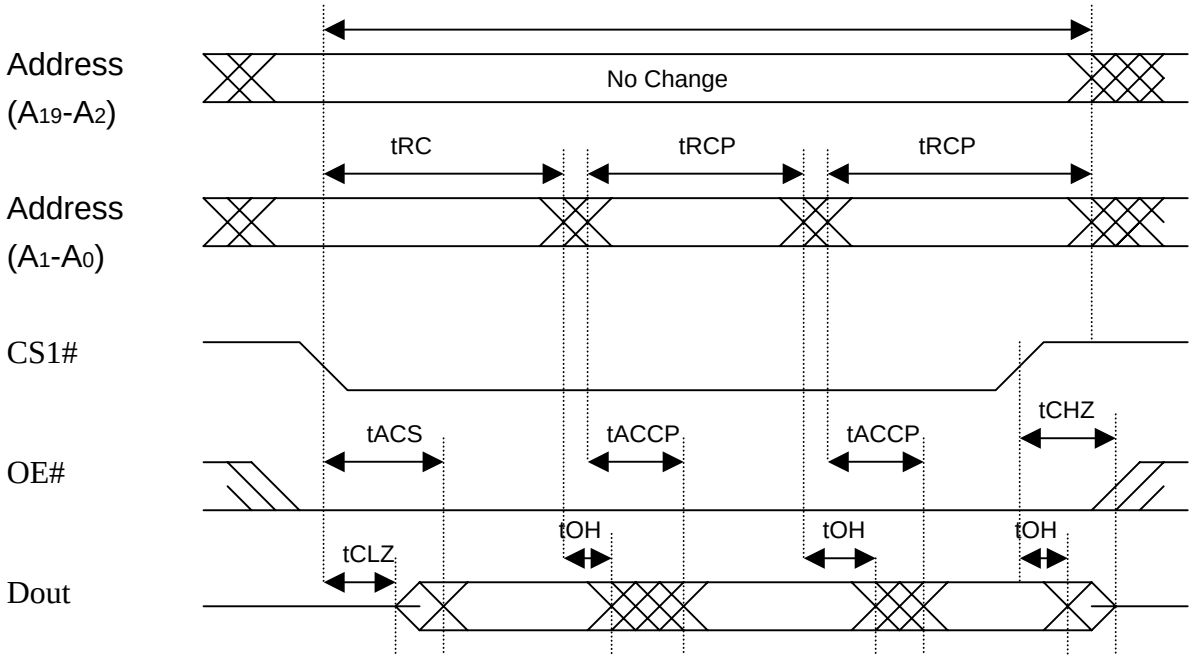
TIMING CHART

Read Cycle



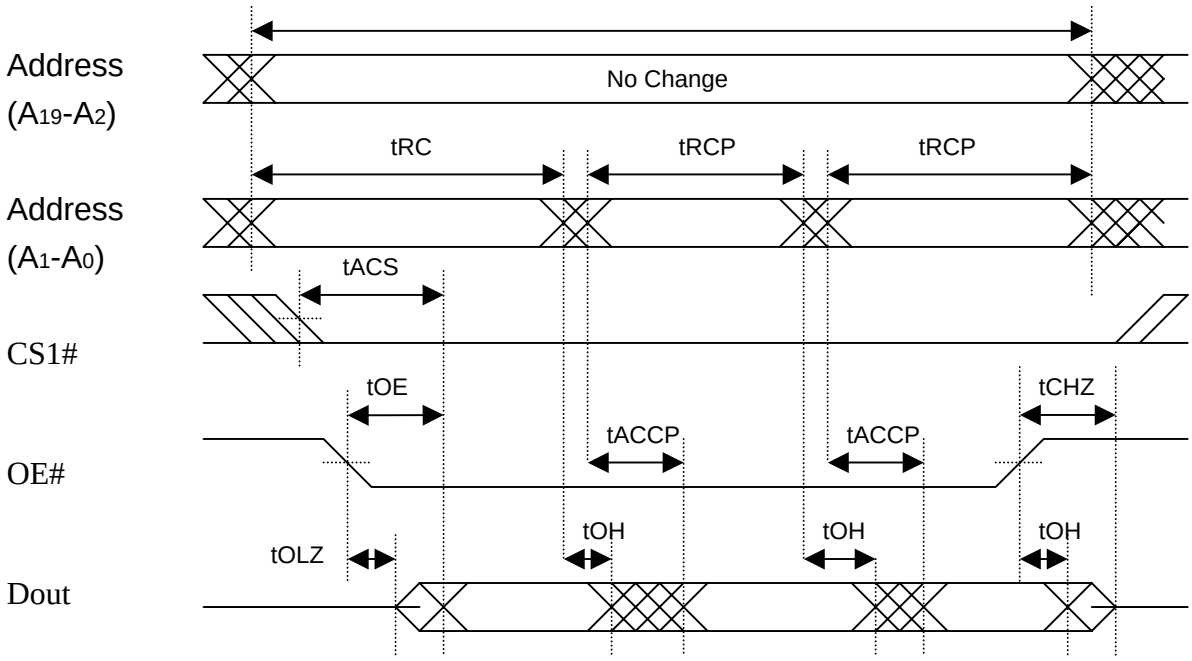
CS2 and WE # must be H level for entire read cycle.

Read Cycle (Page Access [1])



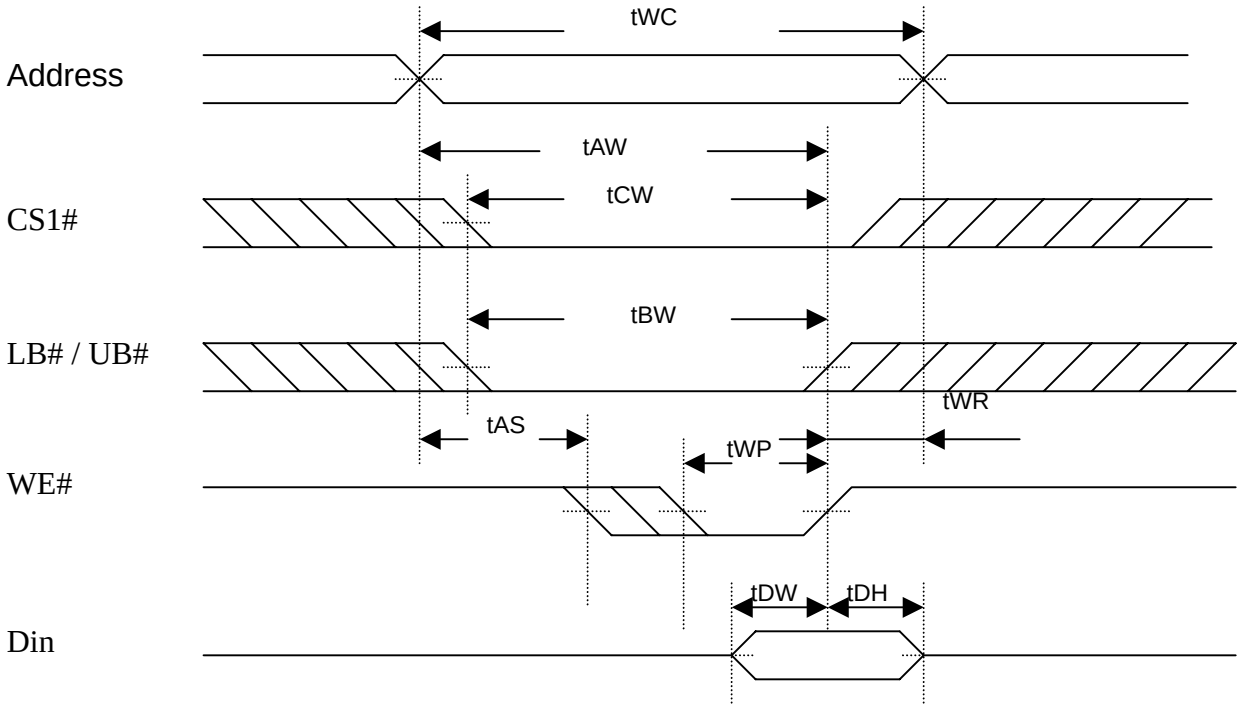
CS2 and WE # must be H level for entire read cycle.

Read Cycle (Page Access [2])



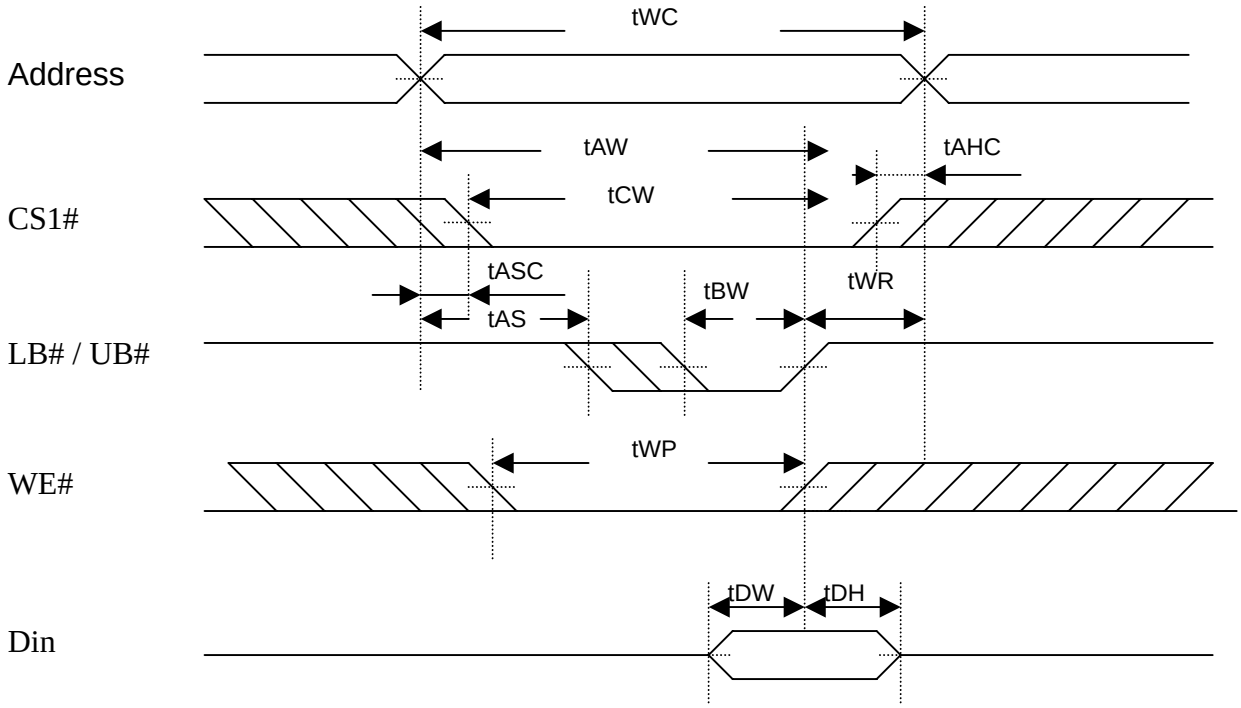
CS2 and WE # must be H level for entire read cycle.

Write Cycle (WE # Control)



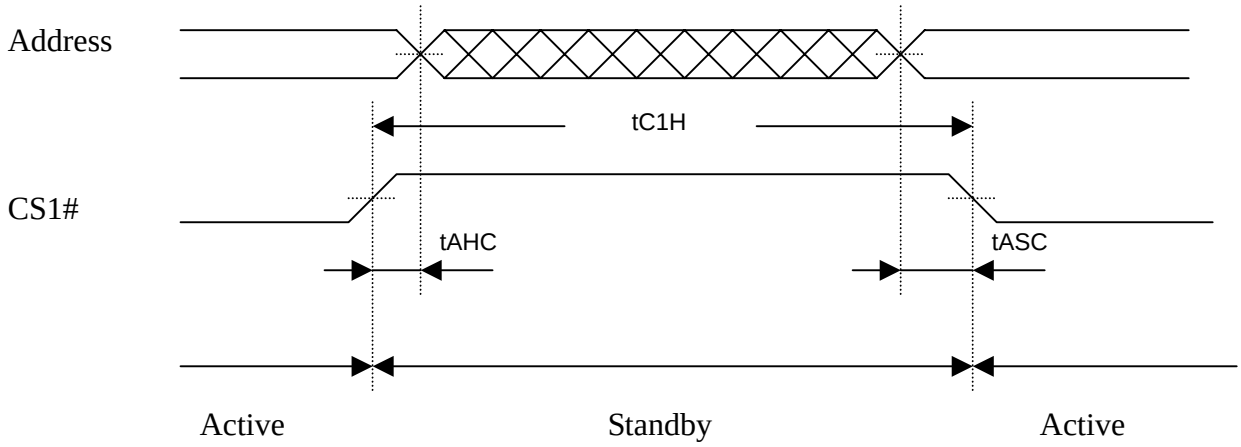
CS2 and OE # must be H level for entire read cycle.

Write Cycle (LB # / UB # Control)

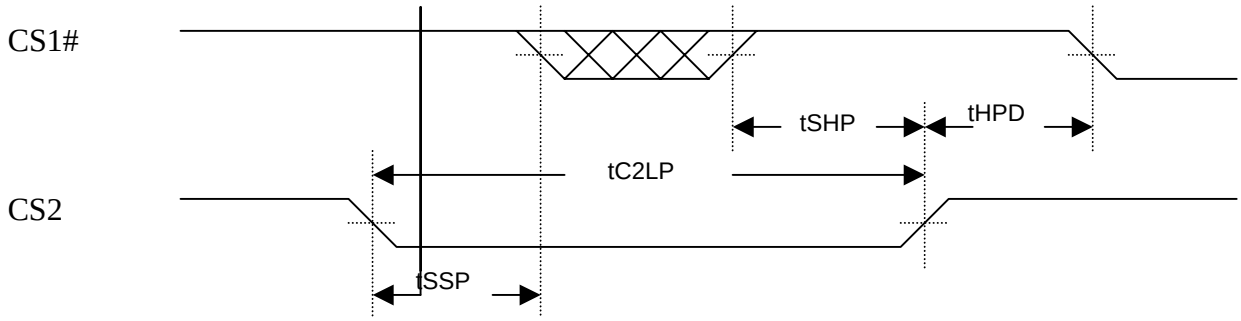


CS2 and OE # must be H level for entire read cycle.

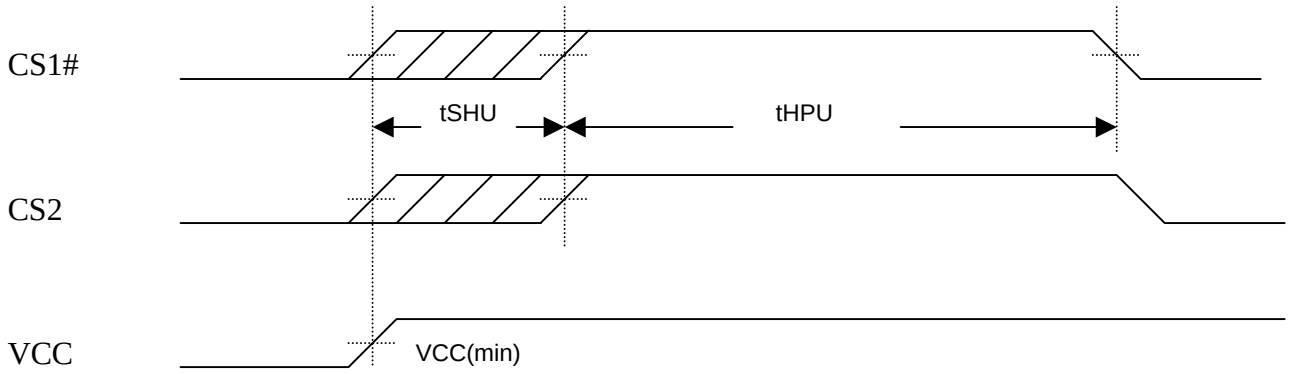
Standby



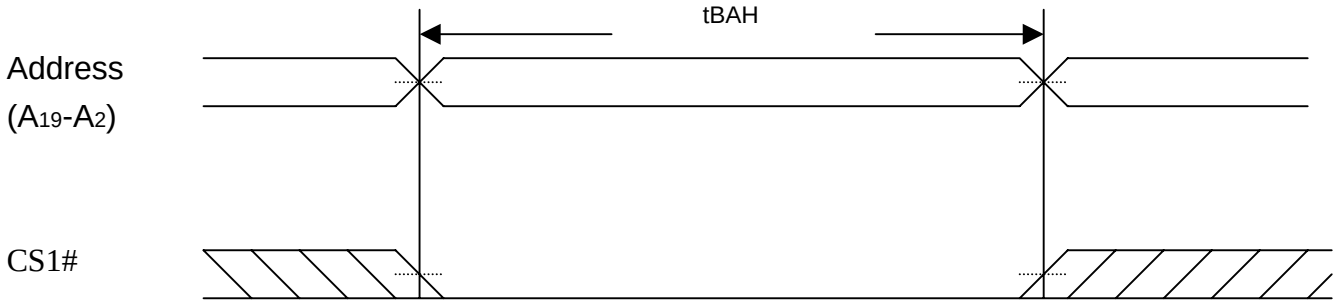
Power Down Mode Entry / Exit



Power Up

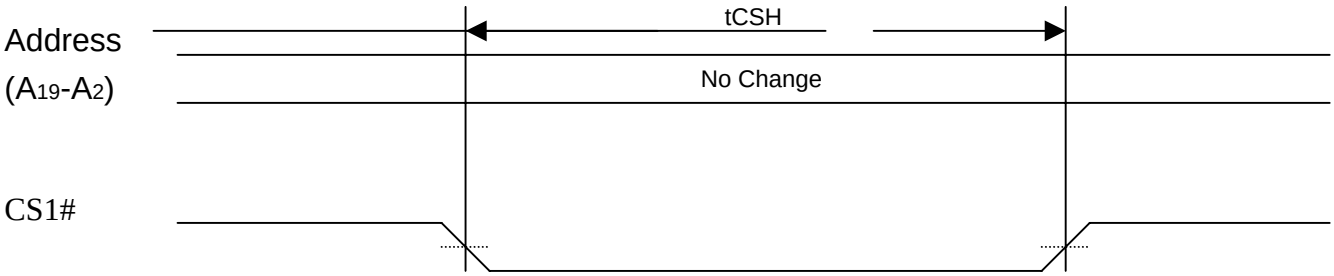


Data Retention(1)



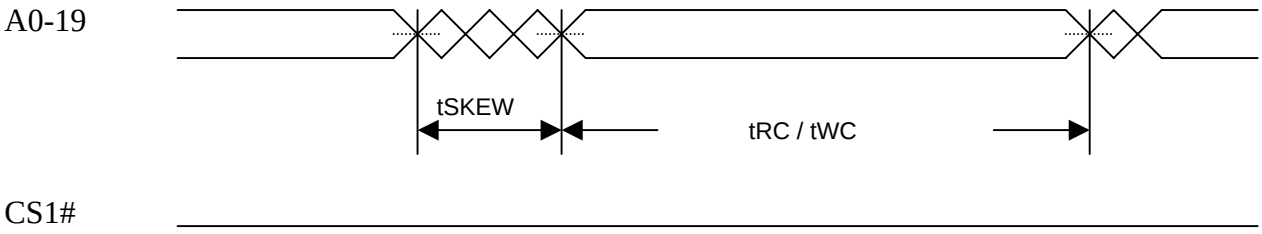
This applies for both read and write.

Data Retention (2)



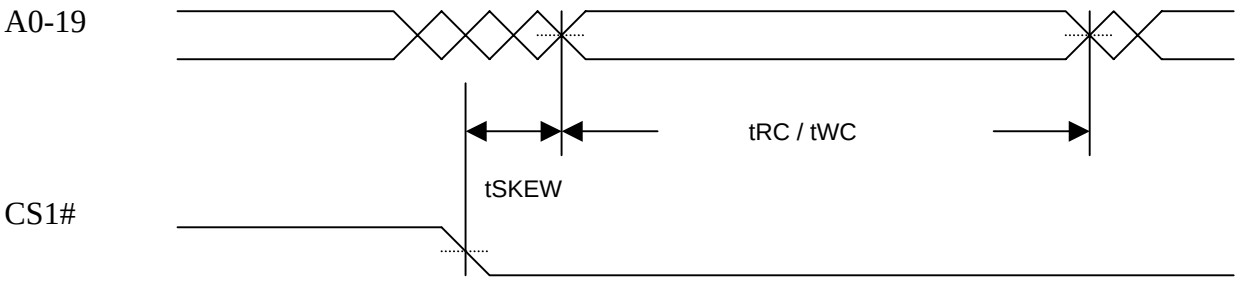
This applies for both read and write.

Address Skew(1)



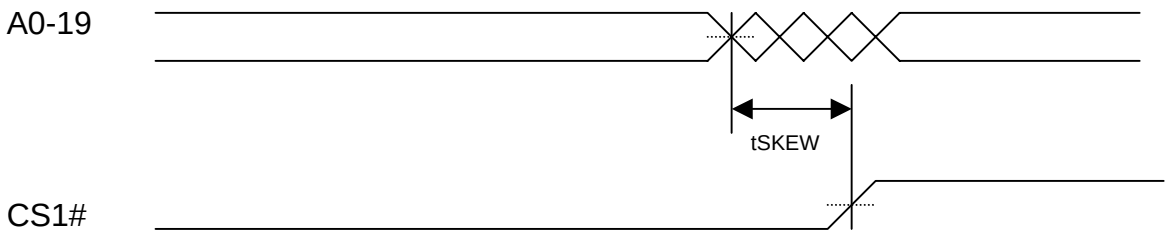
t_{SKEW} is from first address change to last address change

Address Skew(2)



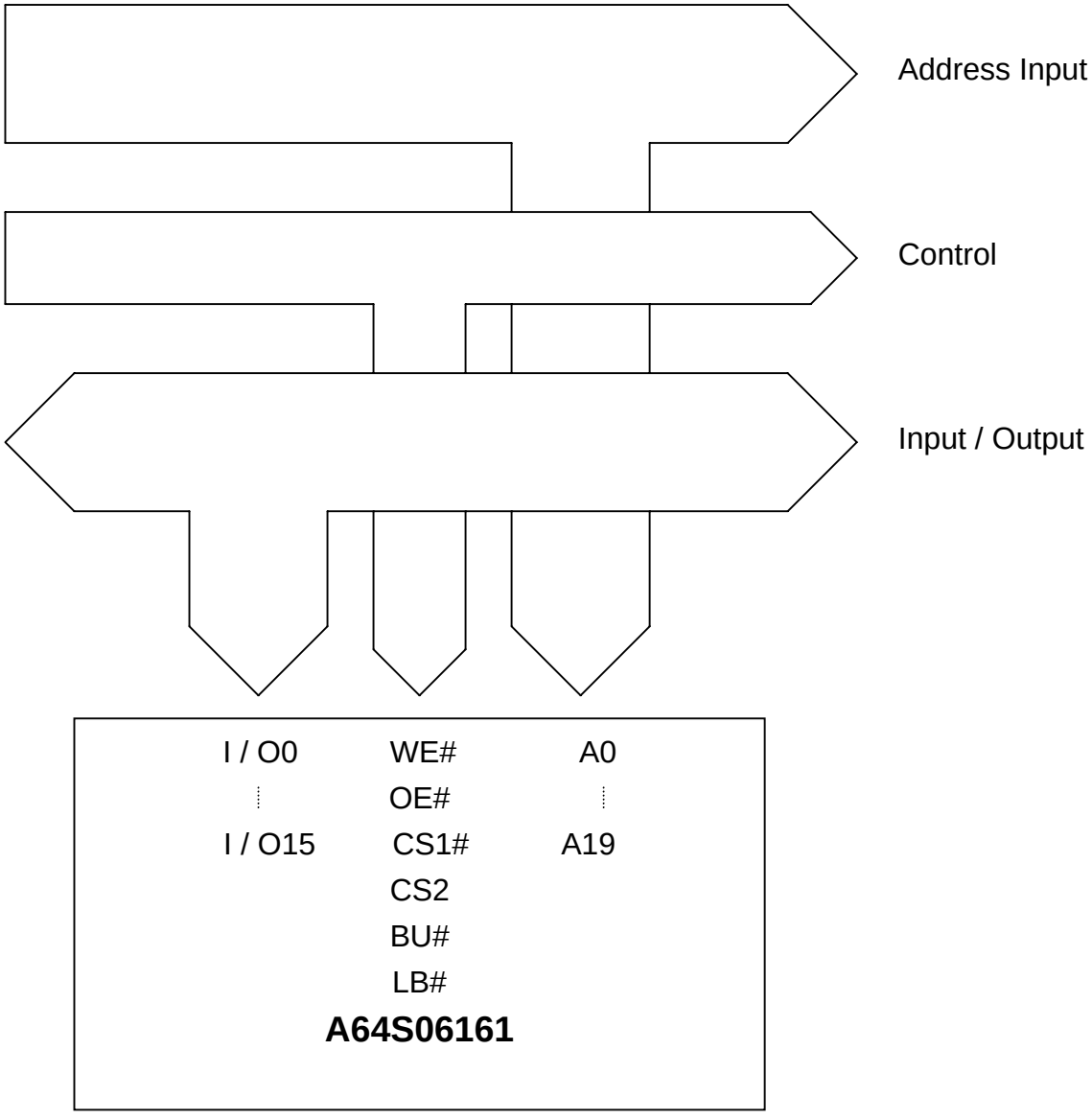
t_{SKEW} is from first address change to last address change

Address Skew(3)



t_{SKEW} is from first address change to stand-by

Reference External Wiring Diagram

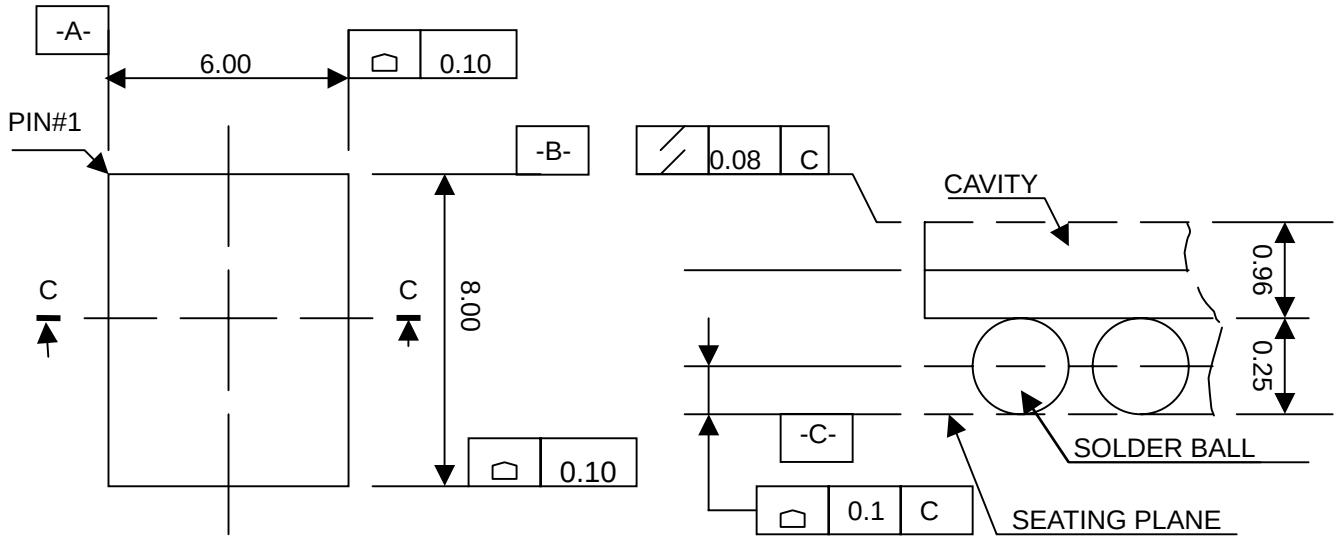


Ordering Information

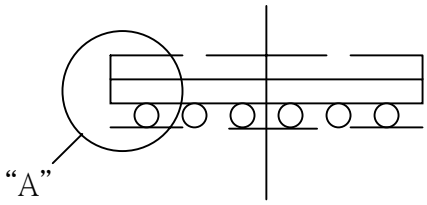
Part No.	Access Time (ns)	Operating Current Max. (mA)	Power Down Mode Standby Current Max. (μA)	Package
A64S06161G-70I	70	20	25	48 Pins FBGA

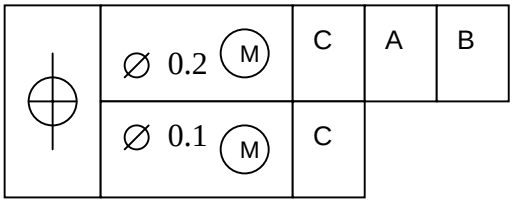
Note: -I is for industrial operating temperature range

48 Pins FBGA Package outline drawing

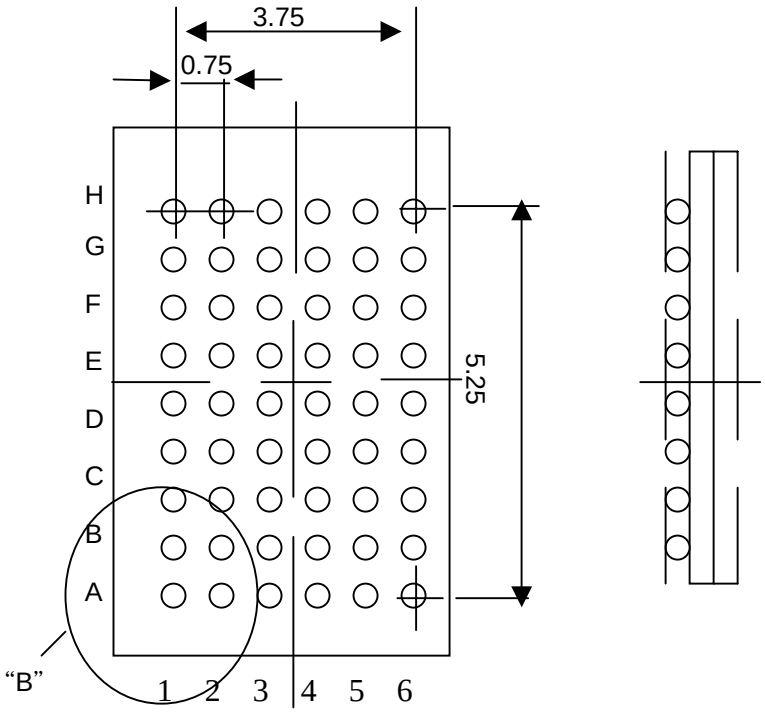


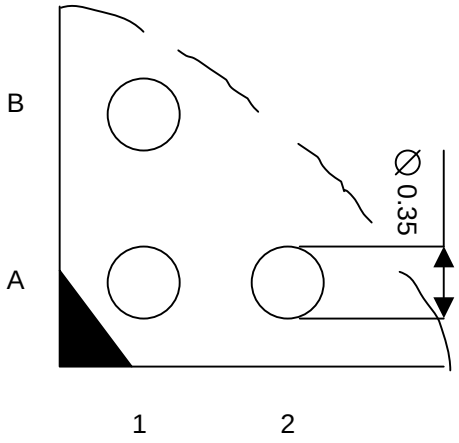
DETAIL : A





SECTION C-C





DETAIL : B