Making Memory Smarter™

5 Volt Asynchronous x9 First-In/First-Out Queue

Memory Configuration	Device	Memory Configuration	Device
8,192 x 9	FQ05	1,024 x 9	FQ02
4,096 x 9	FQ04	512 x 9	FQ01
2,048 x 9	FQ03	256 x 9	FQ00

Key Features:

- **Industry leading First-In/First-Out Queues (up to 50MHz)**
- **Independent Write and Read cycle time**
- **Asynchronous and simultaneous Read and Write**
- **5V power supply**
- **Fully expandable in both word depth and width**
- **Retransmit capability**
- **Full, Empty, and Half Full flag indicators**
- **Available packages: 28 - pin Plastic Dual In-line Package (PDIP), 28 - pin Plastic Thin Dual In-line Package (PTDIP), 28 - pin Small Outline Integrated Circuit (SOIC), 32 – pin Thin Quad Flat Pack (TQFP), 32 - pin Plastic Lead Chip Carrier (PLCC)**
- **(0°C to 70°C) Commercial operating temperature available for access time of 12ns and above**
- **(-40°C to 85°C) Industrial operating temperature available for access time of 25ns**
- **Pin-to-pin compatible with IDT (7200, 7201, 7202, 7203, 7204, 7205) and Cypress (CY7C419, CY7C421, CY7C425, CY7C429, CY7C433, CY7C460A)**

Product Description:

HBA's FlexQ™ Async FIFO offers industry leading 0.25um process technology and memory densities from 256 x 9 to 8,192 x 9. System designer has full flexibility of implementing deeper and wider queues using the depth and width expansion features. Full and Empty indicators allow easy handshaking between transmitters and receivers.

Independent Write and Read controls provide rate-matching capability. System designer can re-read data from the starting position by using Retransmit ($\overline{\text{RET}}$). Retransmit allows reset of the read pointer to its initial position. Half Full flag ($\overline{\text{HALF}}$) is available in the single device mode and width expansion mode, but not in depth expansion mode.

These FlexQ™ Async devices have low power consumption, hence minimizing system power requirements. In addition, industry standard 28 - pin PDIP, 28 – pin PTDIP, 28 – pin SOIC, 32 – pin TQFP and 32 - pin PLCC are offered to save system board space.

These queues are ideal for applications such as data communication, telecommunication, graphics, multiprocessing, test equipment, medical systems, network switching, etc.

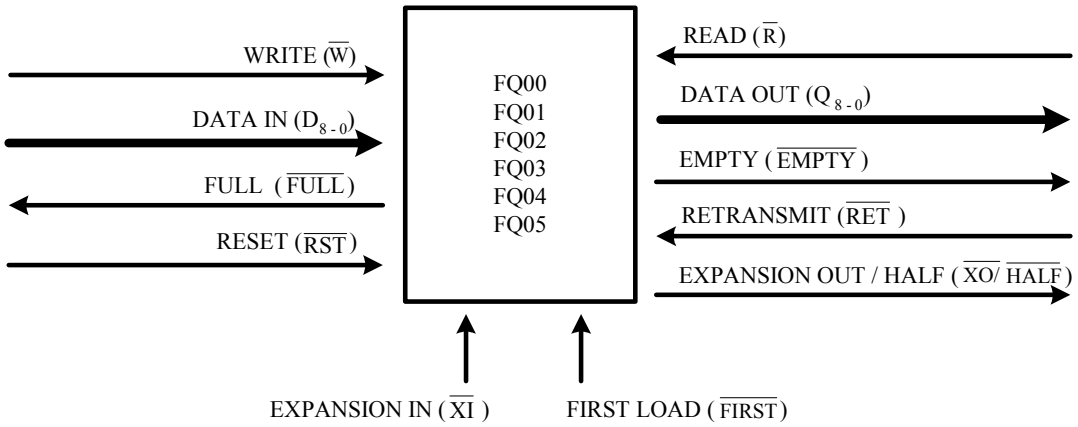


Figure 1. Single Device Configuration Signal Flow Diagram

Block Diagram of Single Asynchronous Queue
8,192 x 9 / 4,096 x 9 / 2,048 x 9 / 1,024 x 9 / 512 x 9 / 256 x 9

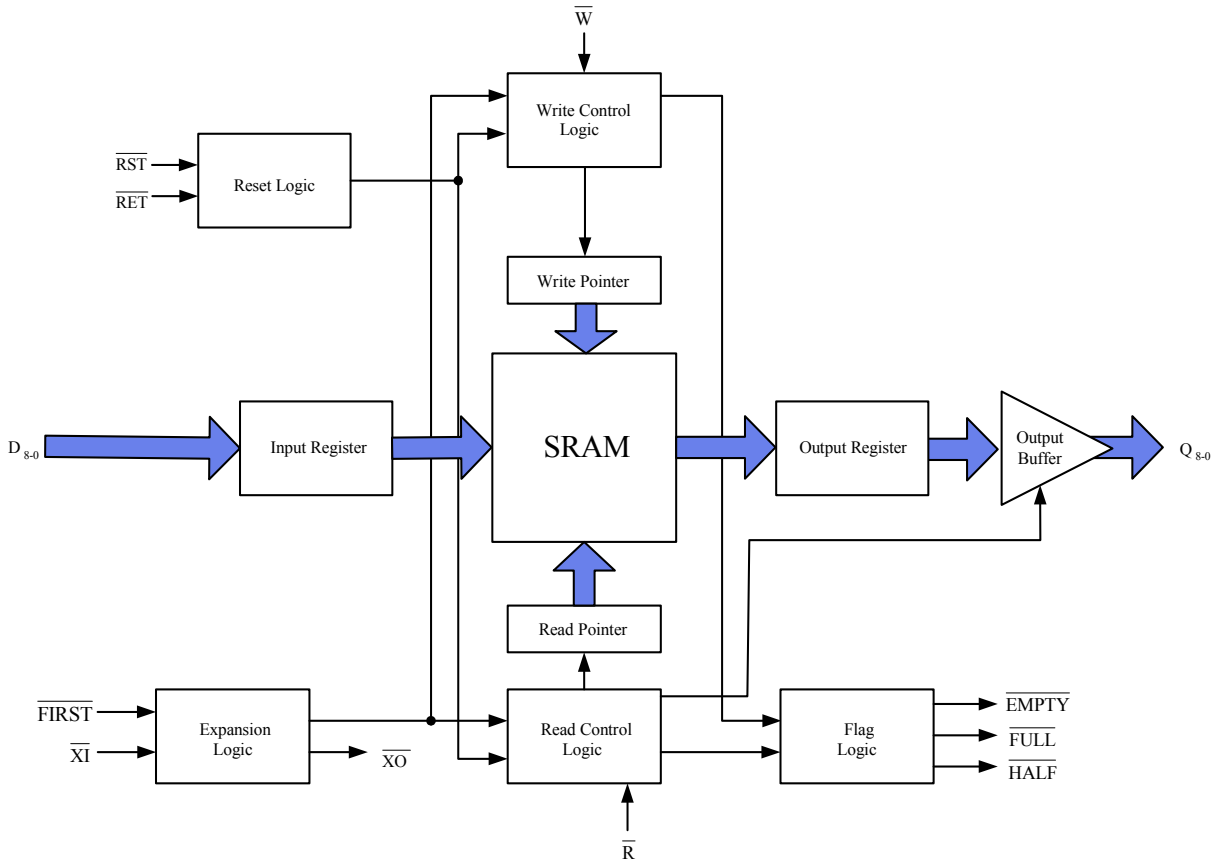
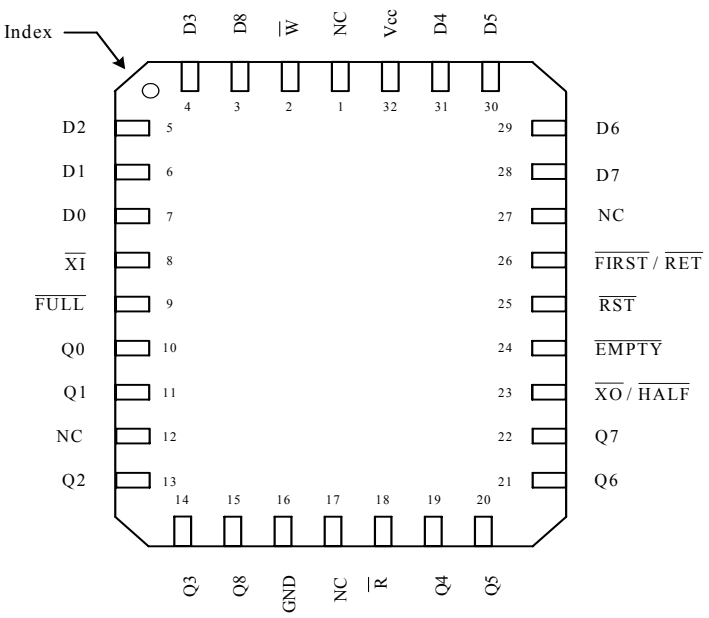
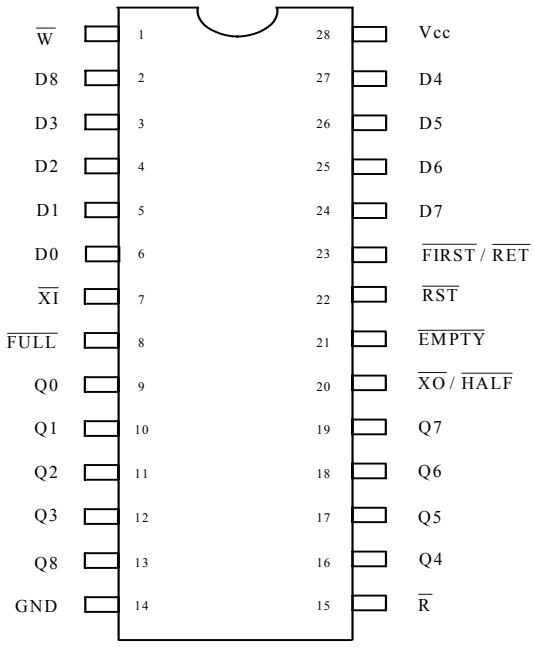


Figure 2. Device Architecture



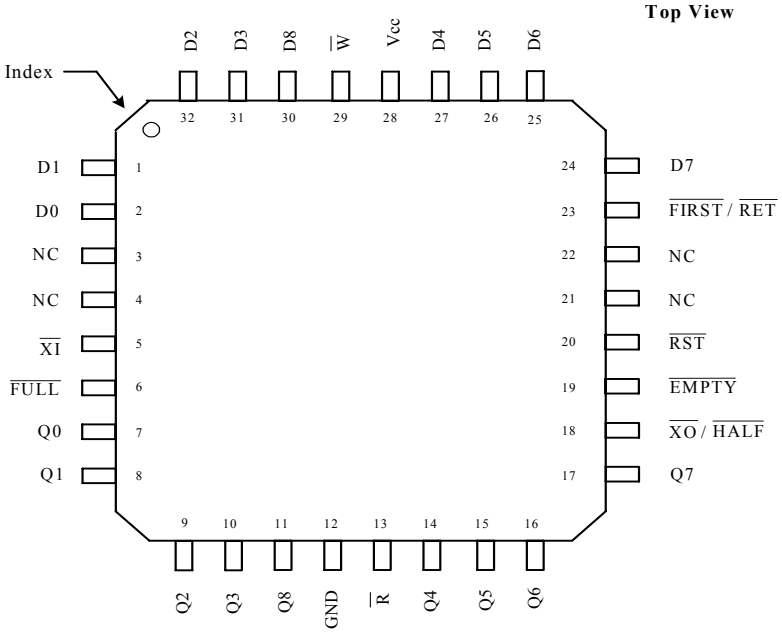
PLCC - 32 (Drw No: J-01A; Order code: J)

Top View



Plastic DIP - 28 (Drw No: P-01A; Order code: P)
Plastic Thin DIP - 28 (Drw No: TP-01A; Order code: TP)
SOIC - 28 (Drw No: SO-01A; Order code: SO)

Top View



TQFP - 32 (Drw No: PF-04A; Order code: PF)

Top View

Figure 3. Device Pin-Out

Pin # J	Pin # P, TP, SO	Pin # PF	Symbol	Name	Input/ Output	Description
25	22	20	$\overline{RST}$	Reset	Input	Reset is required to initialize Write and Read pointers to the first position of the queue by setting $\overline{RST}$ low. $\overline{FULL}$ will go high; $\overline{EMPTY}$ will go low.
2	1	29	$\overline{W}$	Write	Input	Writes data into queue during low to high transitions of $\overline{W}$ if queue is not full yet.
3, 4, 5, 6, 7, 28, 29, 30, 31	2, 3, 4, 5, 6, 24, 25, 26, 27	1, 2, 24, 25, 26, 27, 30, 31, 32	D_{8-0}	Data Inputs	Input	9 - bit wide input data bus.
18	15	13	$\overline{R}$	Read	Input	Reads data from queue during high to low transitions of $\overline{R}$ if queue is not empty.
10, 11, 13, 14, 15, 19, 20, 21, 22	9, 10, 11, 12, 13, 16, 17, 18, 19	7, 8, 9, 10, 11, 14, 15, 16, 17	Q_{8-0}	Data Output	Output	9 - bit wide output data bus.
26	23	23	$\overline{FIRST}$ / $\overline{RET}$	First Load/ Retransmit	Input	$\overline{FIRST}$ / $\overline{RET}$ is used differently depending on mode. In Depth Expansion Mode, the pin is grounded to indicate first load. In Single Device Mode, the pin acts as retransmit.
8	7	5	$\overline{XI}$	Expansion In	Input	$\overline{XI}$ is used to indicate operations in different modes. When the pin is grounded, it indicates an operation in the Single Device Mode. When it is tied to Vcc, it indicates an operation in Depth Expansion Mode.
9	8	6	$\overline{FULL}$	Full Flag	Output	Queue is full when $\overline{FULL}$ goes low. This prohibits further writes into the queue. The assertion of $\overline{FULL}$ is synchronous to the falling edge of $\overline{W}$ and the deassertion is synchronous to the rising edge of $\overline{R}$.
24	21	19	$\overline{EMPTY}$	Empty Flag	Output	Queue is empty when $\overline{EMPTY}$ goes low. This prohibits further reads from the queue. The assertion of $\overline{EMPTY}$ is synchronous to the falling edge of $\overline{R}$ and the deassertion is synchronous to the rising edge of $\overline{W}$.
23	20	18	$\overline{XO}$ / $\overline{HALF}$	Expansion Out / Half Full Flag	Output	$\overline{XO}$ / $\overline{HALF}$ is used differently depending on mode. In Depth Expansion Mode, $\overline{XI}$ is connected to the previous device's $\overline{XO}$ pin. When the previous device has reached the last location of memory, this pin will send pulses to the next device in the Daisy Chain. In Single Device Mode, when $\overline{XI}$ is grounded, this pin indicates queue is half-full.
32	28	28	Vcc	Power	N/A	5V power supply.
16	14	12	GND	Ground	N/A	0V Ground.
1, 12, 17, 27	N/A	3, 4, 21, 22	NC	No Connection	N/A	No connection.

Table 1. Pin Descriptions

Symbol	Rating	Com'l & Ind'l	Unit
V_{TERM}	Terminal Voltage with respect to GND	-0.5 to + 7	V
T_{STG}	Storage Temperature	-55 to +125	°C
I_{OUT}	DC Output Current	-50 to +50	mA

NOTES:
Absolute Max Ratings are for reference only. Permanent damage to the device may occur if extended period of operation is outside this range. Standard operation should fall within the Recommended Operating Conditions.

Table 2. Absolute Maximum Ratings

		FQ05, FQ04, FQ03, FQ02, FQ01, FQ00						
		Commercial t_A = 12ns, 25ns, 35ns, 50ns			Industrial t_A = 25ns			
Symbol	**Parameter**	**Min.**	**Typ.**	**Max.**	**Min.**	**Typ.**	**Max.**	**Unit**
Recommended Operating Conditions								
V_{CC}	Supply Voltage Com'l/Ind'l	4.5	5.0	5.5	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	0	0	0	V
V_{IH}	Input High Voltage Com'l/Ind'l	2.0	-	-	2.0	-	-	V
V_{IL}	Input Low Voltage Com'l/Ind'l	-	-	0.8	-	-	0.8	V
T_A	Operating Temperature	0	-	70	-40	-	85	°C
DC Electrical Characteristics								
I_{LI}(1)	Input Leakage Current (any input)	-10	-	10	-10	-	10	µA
I_{LO}	Output Leakage Current	-10	-	10	-10	-	10	µA
V_{OH}	Output Logic "1" Voltage, I_{OH}=-2mA	2.4	-	-	2.4	-	-	V
V_{OL}	Output Logic "0" Voltage, I_{OL} = 8mA	-	-	0.4	-	-	0.4	V
Power Consumption								
$I_{CC}1$(2,3,4)	Active Power Supply Current	-	-	80	-	-	80	mA
$I_{CC}2$(2,5)	Standby Current	-	-	5	-	-	5	mA

Capacitance at 1.0MHz Ambient Temperature (25°C)				
Symbol	**Parameter**	**Conditions**	**Max.**	**Unit**
C_{IN}(6)	Input Capacitance	V_{IN}= 0V	8	pF
C_{OUT}(6)	Output Capacitance	V_{OUT}= 0V	8	pF

NOTES:
1. Measurement with 0.4<=V_{IN}<=Vcc
2. Tested with outputs open (I_{OUT}=0)
3. Tested at f=20MHz
4. Typical Icc1=15+2*fs+0.02*C_L*fc (in mA) with Vcc=5V, t_A=25°C, fs=WCLK frequency=RCLK frequency (in MHz, using TTL levels), data switching at fs/2, C_L=Capacitive load (in PF)
5. All inputs = Vcc-0.2V or GND+0.2V and ($\overline{R}$=$\overline{W}$=$\overline{RST}$=$\overline{FIRST}$/$\overline{RET}$=V_{IH})
6. Design simulated, not tested.

Table 3. DC Specifications

Symbol	Parameter	Commercial & Industrial								Unit
		FQ05-12 FQ04-12 FQ03-12 FQ02-12 FQ01-12 FQ00-12		FQ05-25 FQ04-25 FQ03-25 FQ02-25 FQ01-25 FQ00-25		FQ05-35 FQ04-35 FQ03-35 FQ02-35 FQ01-35 FQ00-35		FQ05-50 FQ04-50 FQ03-50 FQ02-50 FQ01-50 FQ00-50		
		Min.	Max	Min.	Max	Min.	Max	Min.	Max	
f_S	Shift Frequency	-	50	-	28.5	-	22.2	-	15	MHz
t_{RC}	Read Cycle Time	20	-	35	-	45	-	65	-	ns
t_A	Access Time	-	12	-	25	-	35	-	50	ns
t_{RR}	Read Recovery Time	8	-	10	-	10	-	15	-	ns
t_{RPW}	Read Pulse Width	12	-	25	-	35	-	50	-	ns
t_{RLZ}	Read Pulse Low to Data Bus at Low Z (1)	3	-	3	-	3	-	3	-	ns
t_{WLZ}	Write Pulse High to Data Bus at Low Z (1,2)	3	-	5	-	5	-	5	-	ns
t_{DV}	Data Valid from Read Pulse High	5	-	5	-	5	-	5	-	ns
t_{RHZ}	Read Pulse High to Data Bus at High Z (1)	-	12	-	18	-	20	-	30	ns
t_{WC}	Write Cycle Time	20	-	35	-	45	-	65	-	ns
t_{WPW}	Write Pulse Width	12	-	25	-	35	-	50	-	ns
t_{WR}	Write Recovery Time	8	-	10	-	10	-	15	-	ns
t_{DS}	Data Set-up Time	9	-	15	-	18	-	30	-	ns
t_{DH}	Data Hold Time	0	-	0	-	0	-	5	-	ns
t_{RSTC}	Reset Cycle Time	20	-	35	-	45	-	65	-	ns
t_{RST}	Reset Pulse Width	12	-	25	-	35	-	50	-	ns
t_{RSTS}	Reset Set-up Time (1)	12	-	25	-	35	-	50	-	ns
t_{RSTR}	Reset Recovery Time	8	-	10	-	10	-	15	-	ns
t_{RETC}	Retransmit Cycle Time	20	-	35	-	45	-	65	-	ns
t_{RET}	Retransmit Pulse Width	12	-	25	-	35	-	50	-	ns
t_{RETS}	Retransmit Set-up Time (1)	12	-	25	-	35	-	50	-	ns
t_{RETR}	Retransmit Recovery Time	8	-	10	-	10	-	15	-	ns
t_{EFL}	Reset to Empty Flag Low	-	12	-	35	-	45	-	65	ns
t_{HFH}, t_{FFH}	Reset to Half-Full and Full Flag High	-	17	-	35	-	45	-	65	ns
t_{RETF}	Retransmit Low to Flags Valid	-	20	-	35	-	45	-	65	ns
t_{REMPTY}	Read Low to Empty Flag Low	-	12	-	25	-	30	-	45	ns
t_{RFULL}	Read High to Full Flag High	-	14	-	25	-	30	-	45	ns
t_{RPE}	Read Pulse Width after Empty Flag High	12	-	25	-	35	-	50	-	ns
t_{WEMPTY}	Write High to Empty Flag High	-	12	-	25	-	30	-	45	ns
t_{WFULL}	Write Low to Full Flag Low	-	14	-	25	-	30	-	45	ns
t_{WHALF}	Write Low to Half-Full Flag Low	-	17	-	35	-	45	-	65	ns
t_{RHALF}	Read High to Half-Full Flag High	-	17	-	35	-	45	-	65	ns
t_{WPF}	Write Pulse Width after Full Flag High	12	-	25	-	35	-	50	-	ns
t_{XOL}	Read/Write to $\overline{XO}$ Low	-	12	-	25	-	35	-	50	ns
t_{XOH}	Read/Write to $\overline{XO}$ High	-	12	-	25	-	35	-	50	ns
t_{XI}	$\overline{XI}$ Pulse Width	12	-	25	-	35	-	50	-	ns
t_{XIR}	$\overline{XI}$ Recovery Time	8	-	10	-	10	-	10	-	ns
t_{XIS}	$\overline{XI}$ Set-up Time	8	-	10	-	15	-	15	-	ns

NOTES:
1. Design simulated, not tested.
2. Only applies to read data flow-through mode.

Table 4. AC Electrical Characteristics

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	Refer to Figure 4

Table 5. AC Test Condition

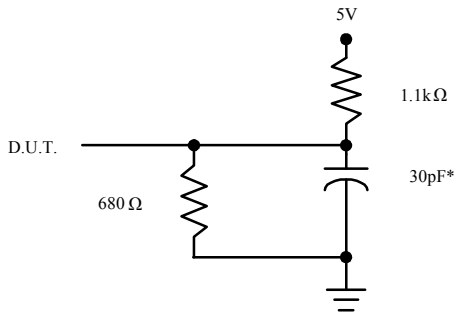
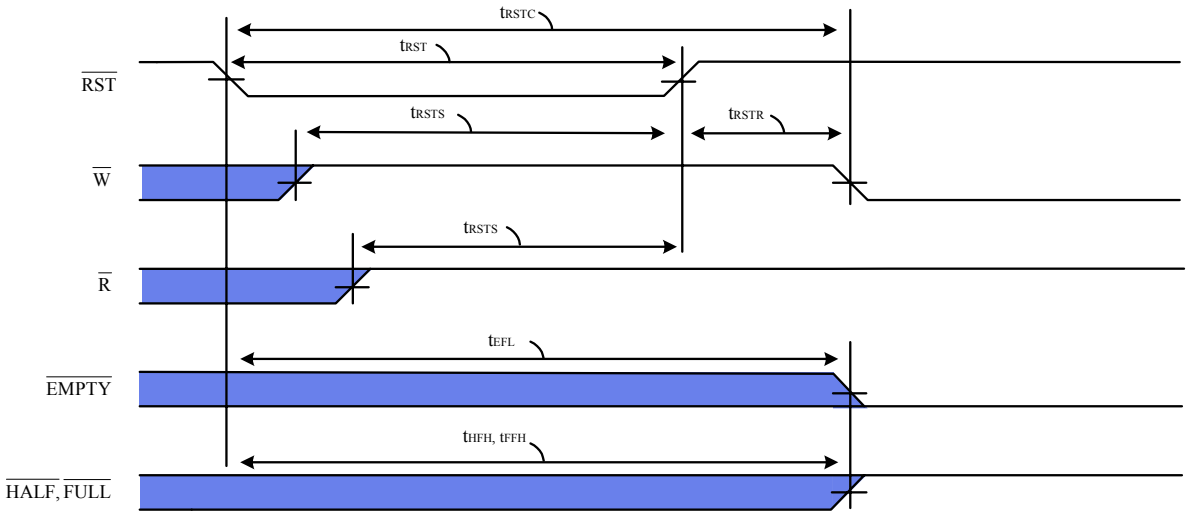


Figure 4. Output Load
*Includes jig and scope capacitances.

Timing Diagrams



NOTES:
1. EMPTY, FULL, and HALF may change status during Reset, but are valid at tRSTC.
2. W and R = VIH near rising edge of RST.

Diagram 1. Reset Timing

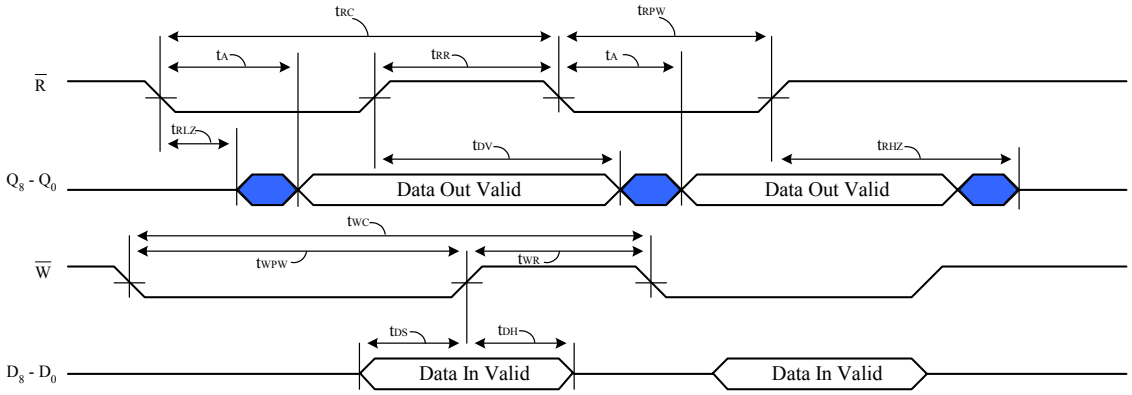


Diagram 2. Asynchronous Write and Read Operation

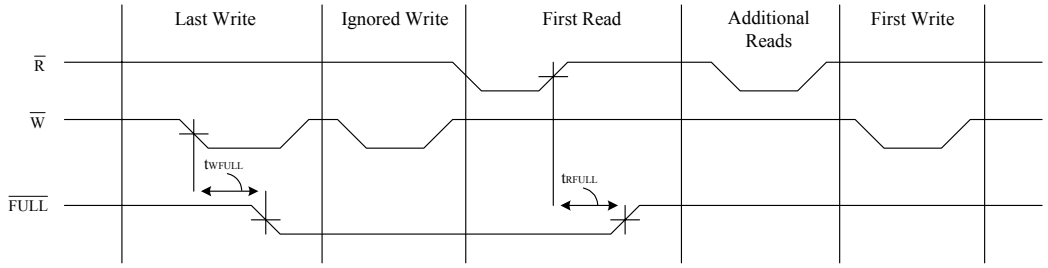


Diagram 3. Full Flag From Last Write to First Read

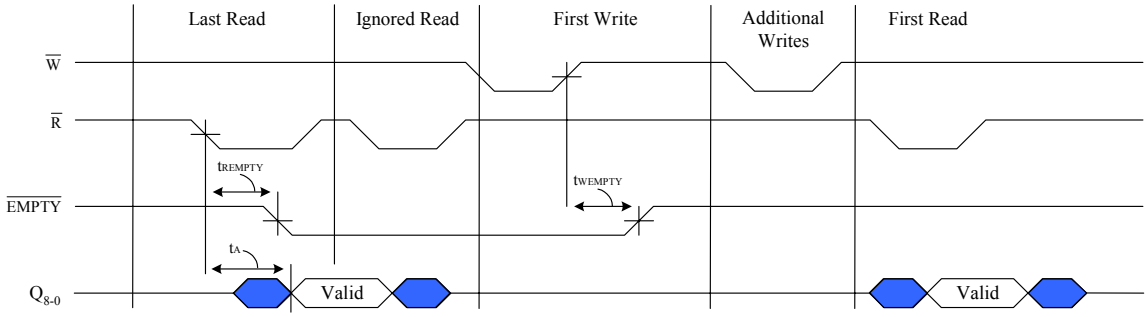


Diagram 4. Empty Flag From Last Read to First Write

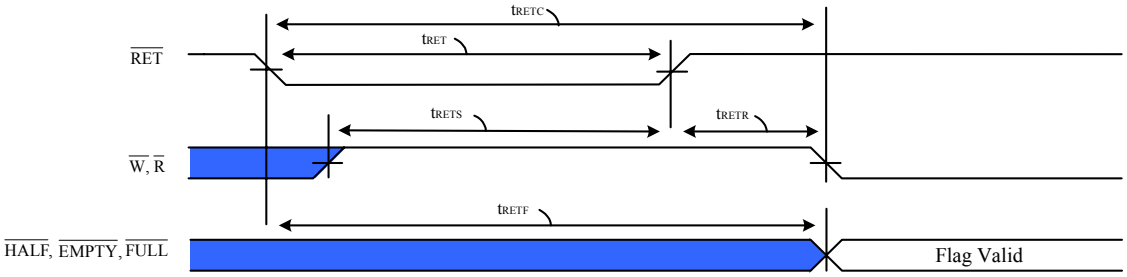


Diagram 5. Retransmit

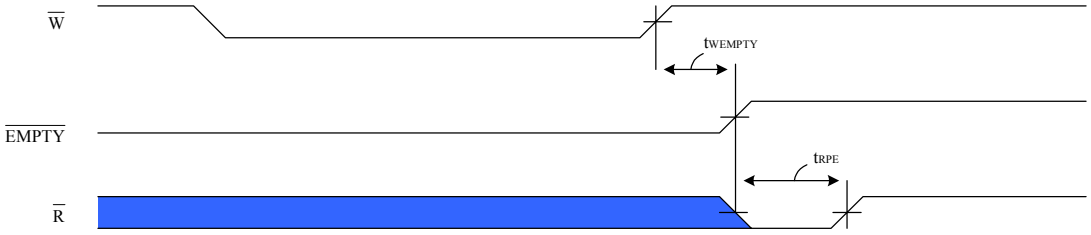


Diagram 6. Minimum Timing for an Empty Flag Coincident Read Pulse

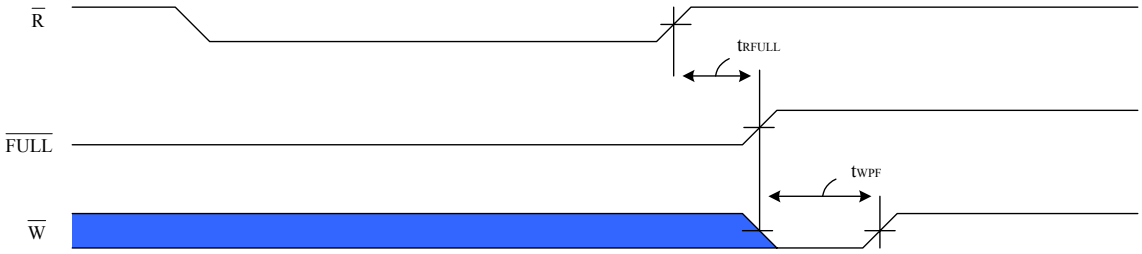


Diagram 7. Minimum Timing for a Full Flag Coincident Write Pulse

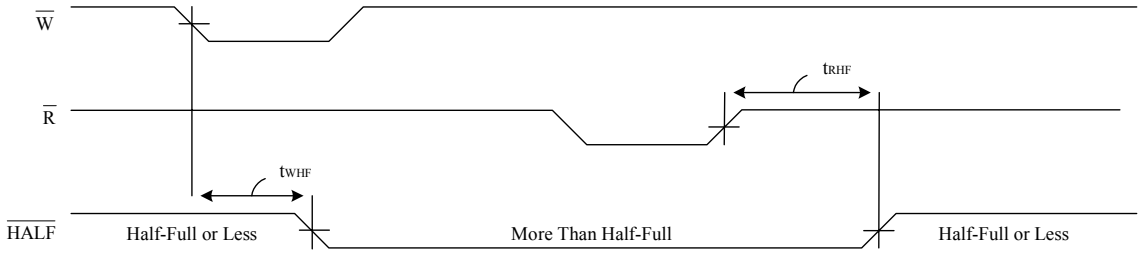


Diagram 8. Half-Full Flag Timing

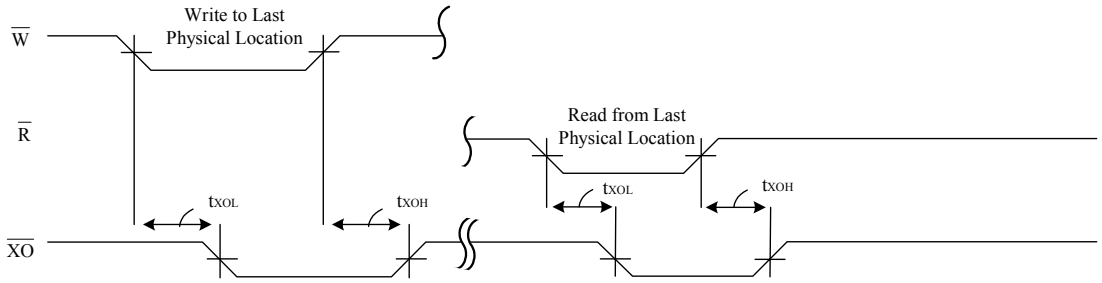


Diagram 9. Expansion Out

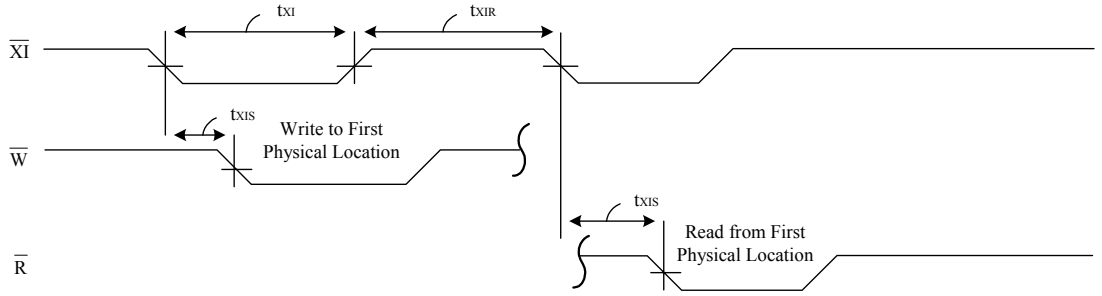


Diagram 10. Expansion In

Operating Modes

Single Device Mode: When application requirements are for 256/512/1,024/2,048/4,096/8,192 words or less, a single device may be used. These devices are in Single Device Mode when Expansion In ($\overline{XI}$) is grounded.

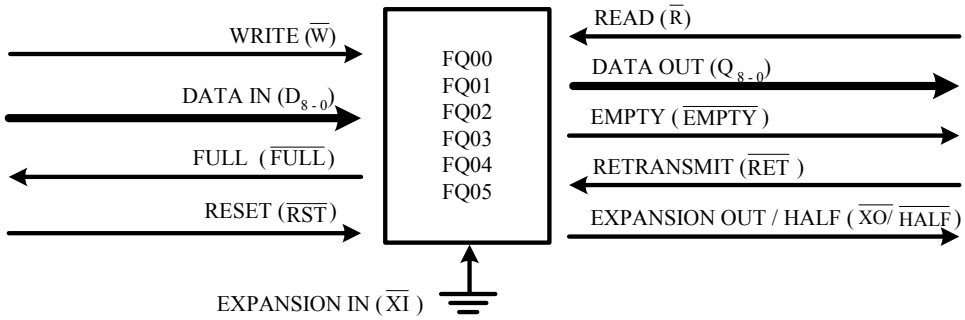


Figure 5. Single Device Mode

Depth Expansion Mode: When application requirements are greater than 256/512/1,024/2,048/4,096/8,192 words, multiple devices may be used for Depth Expansion. These devices are in Depth Expansion Mode when the following conditions are met:

1. The first device's First Load ($\overline{FIRST}$) pin must be grounded.
2. All other devices' First Load ($\overline{FIRST}$) pin must be tied to HIGH
3. All devices' Expansion Out ($\overline{XO}$) pin must be tied to the next devices' Expansion In ($\overline{XI}$) pin.
4. Retransmit ($\overline{RET}$) and Half-Full Flag ($\overline{HALF}$) are non-functional in Depth Expansion Mode.
5. An external logic is required to generate a composite Full Flag ($\overline{FULL}$) and Empty Flag ($\overline{EMPTY}$). This requires the ORing of all Empty and Full Flags.

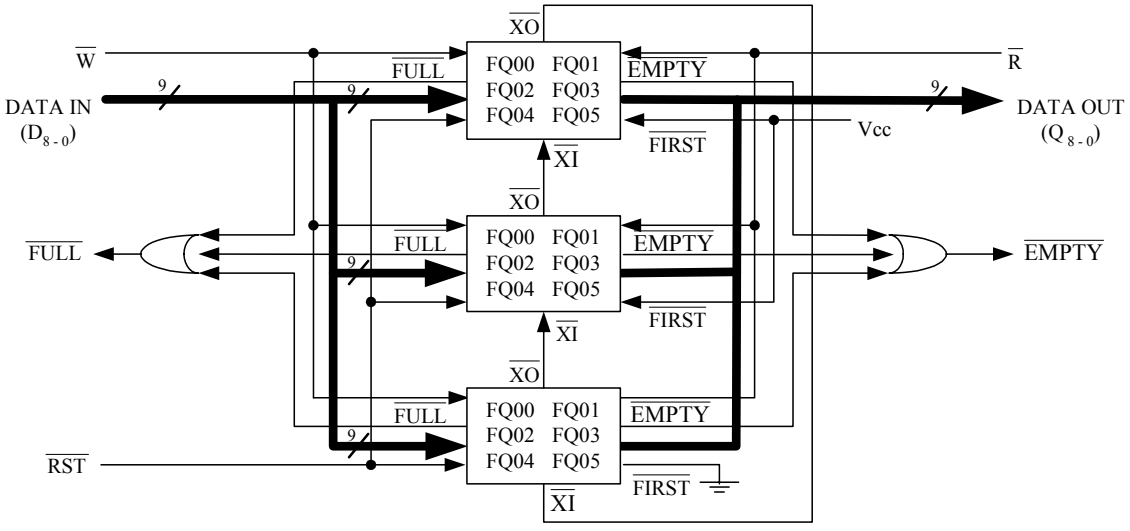


Figure 6. Depth Expansion Mode

Usage Modes

Width Expansion Mode: When applications require increased word width, multiple devices may be used for Width Expansion Mode. These devices are in Width Expansion Mode when the same signals from multiple devices are connected. Any word width may be achieved by connecting additional devices. Status flags are functional for any one device.

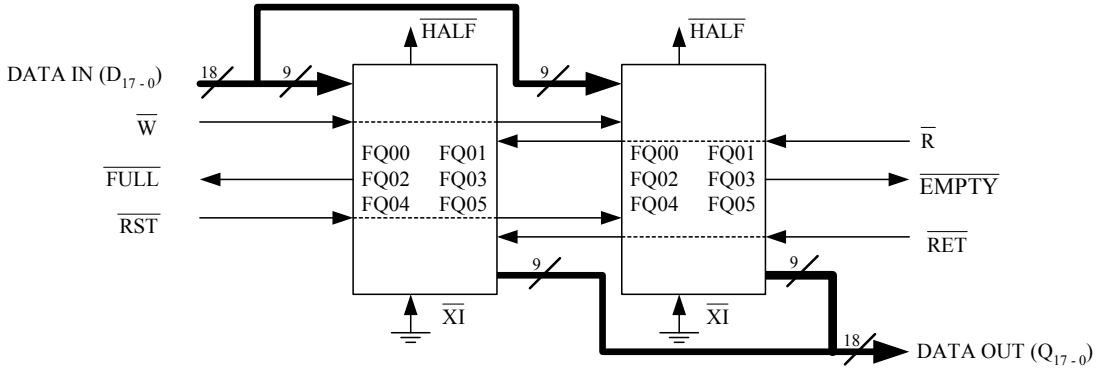


Figure 7. Width Expansion Mode

Bidirectional Mode: When applications require data buffering between two systems that are capable of Read and Write operations, a pair of devices may be used for Bidirectional Mode. Both Depth Expansion and Width Expansion may be used in this mode.

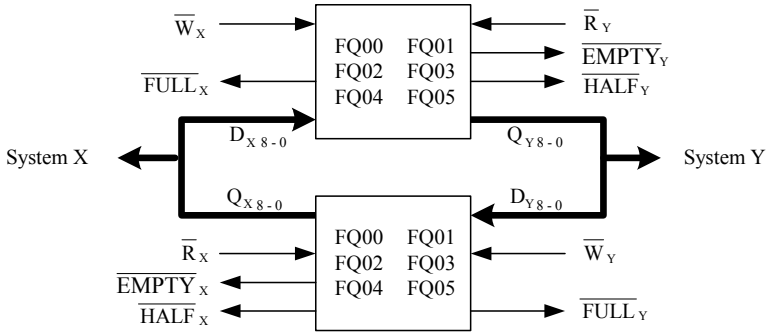


Figure 8. Bidirectional Mode

Data Flow-Through Mode: There are two types of flow-through modes, read flow-through and write flow-through. In the read flow-through mode, the device allows a single word to be read after one word of data has been written into an empty FIFO. The data is enabled on the bus after the rising edge of $\overline{W}$, and remains on the bus until $\overline{R}$ goes from Low to High. Then the bus goes into a three-state mode. $\overline{EMPTY}$ will have a pulse showing temporary deassertion and then would be asserted. In the write flow-through mode, the device allows a single word to be written after one word of data has been read from a full FIFO. $\overline{R}$ causes $\overline{FULL}$ to be deasserted but a Low $\overline{W}$ causes it to be asserted again for the new data word. The new word goes into the FIFO on the rising edge of $\overline{W}$. $\overline{W}$ must be toggled when $\overline{FULL}$ is not asserted to write new data into the FIFO and to increment the write pointer.

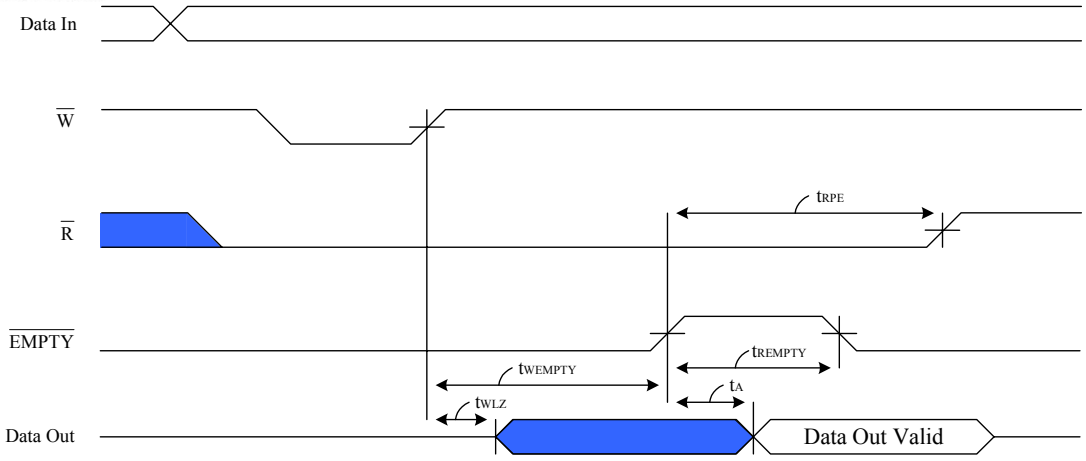


Diagram 11. Read Data Flow-Through Mode

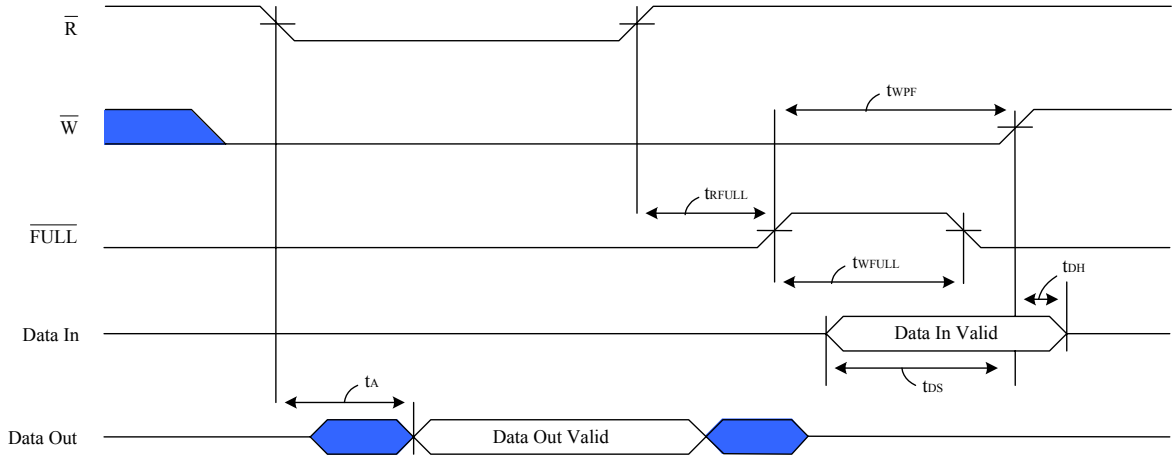


Diagram 12. Write Data Flow-Through Mode

Compound Expansion Mode: Compound Expansion Mode is a combination of Depth and Width Expansion Modes to achieve large FIFO arrays.

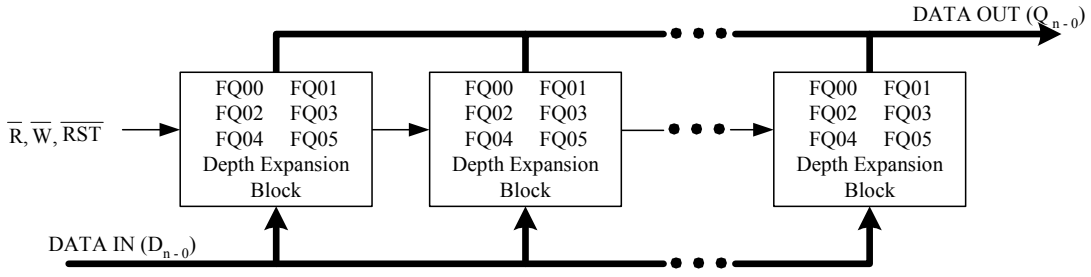


Figure 9. Compound Expansion Mode

Order Information:

HBA Device Family	Device Type	Power	Speed (ns)*	Package**	Temperature Range
XX	XX	X	XX	X	X
FQ	**05** (8,192 x 9)	Low	**12** – 50 MHz	**J**	Blank – Commercial (0°C to 70°C)
	04 (4,096 x 9)		**25** – 29 MHz	**P**	**I** – Industrial (-40° to 85°C) †
	03 (2,048 x 9)		**35** – 22 MHz	**TP**	
	02 (1,024 x 9)		**50** – 15 MHz	**SO**	
	01 (512 x 9)			**PF**	
	00 (256 x 9)				

***Speed** – Slower speeds available upon request.
****Package** – 32 - pin Plastic Lead Chip Carrier (PLCC), 28 - pin Plastic Dual In-line Package (PDIP), 28 - pin Plastic Thin Dual In-line Package (PTDIP), 28 - pin Small Outline Integrated Circuit (SOIC), 32 – pin Thin Quad Flat Pack (TQFP)
†**Temperature** – Industrial only offered in 25ns

Example:

FQ05L12J (8k x 9, 12ns, PLCC, Commercial temp)
FQ00L25PFI (256 x 9, 25ns, TQFP, Industrial temp)

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