Low Cost 16-Bit Analog to Digital Converter

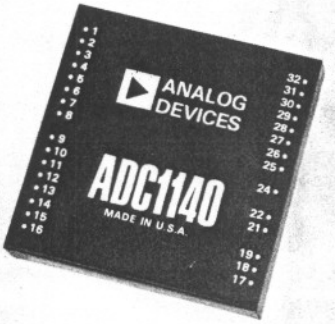
ADC1140

FEATURES

- Guaranteed Nonlinearity: ±0.003% FSR max
- 35μs Maximum Conversion Time
- Small Size 2″ × 2″ × 0.4″
- Wide Power Supply Operation: ±12V to ±17V
- Low Cost $149 (100s)

APPLICATIONS

- Process Control Data Acquisition
- Seismic Data Acquisition
- Nuclear Instrumentation
- Medical Instrumentation
- Pulse Code Modulation Telemetry
- Industrial Scales
- Robotics



GENERAL DESCRIPTION

The ADC1140 is a low cost 16-bit successive-approximation analog-to-digital converter having a 35μs maximum conversion time. This converter provides high accuracy, high stability and low power consumption all in a 2″ × 2″ × 0.4″ module.

High accuracy performance such as integral and differential nonlinearity of ±0.003% FSR max are both guaranteed. Guaranteed stability such as differential nonlinearity TC of ±2ppm/°C maximum, offset TC of ±30μV/°C maximum, gain TC of ±12ppm/°C maximum and power supply sensitivity of ±0.002% of FSR/% V_S are also provided by the ADC1140.

The ADC1140 makes extensive use of both integrated circuit and thin-film components to obtain excellent performance, small size and low cost. The internal 16-bit DAC incorporates Analog Devices' proprietary thin-film resistor technology and proprietary CMOS current-steering switches. A low noise reference, low power comparator and low power successive-approximation register are also used to optimize the ADC1140's design (shown in Figure 1).

The ADC1140 can operate with power supplies ranging from ±12V to ±17V and has provisions for a user supplied external reference. Four analog input voltage ranges are selectable via pin programming: ±5V, ±10V, 0 to +5V and 0 to +10V. Bipolar coding is provided in the offset binary and two's complement formats with unipolar coding displayed in true binary.

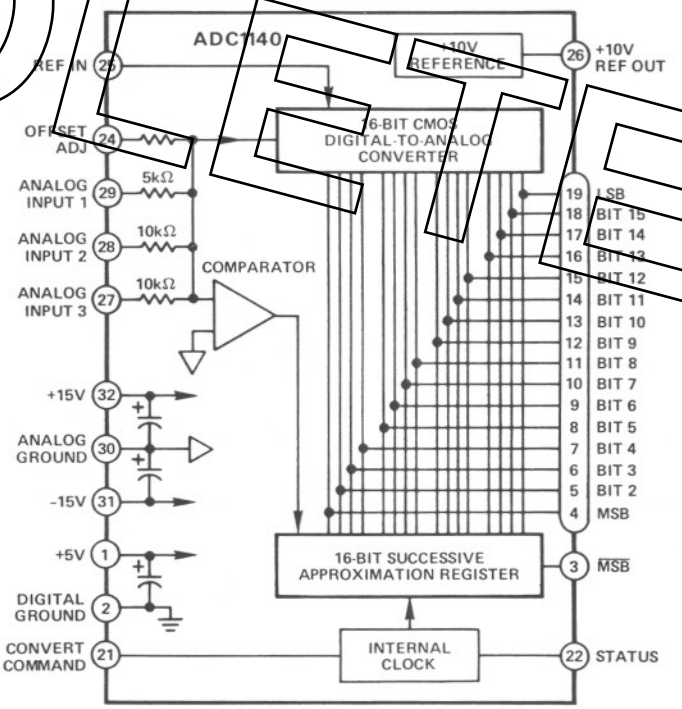


Figure 1. ADC1140 Functional Block Diagram

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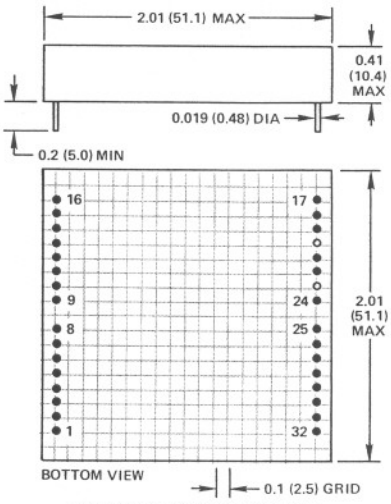
SPECIFICATIONS (typical @ +25°C $\pm V_S$ = ±15V, V_{CC} = +5V, V_{REF} = +10.0V unless otherwise specified)

Model	ADC1140
RESOLUTION	16 Bits
CONVERSION TIME	35µs max
ACCURACY[1]	
Nonlinearity Error	±0.003% FSR[2] max
Differential Nonlinearity Error	±0.003% FSR[2] max
STABILITY	
Differential Nonlinearity	±2ppm/°C max
Gain (with internal reference)	±12ppm/°C max
(without internal reference)	±4ppm/°C max
Unipolar Offset	±30µV/°C max
Bipolar Offset	±7ppm/°C max
POWER SUPPLY SENSITIVITY	±0.002% FSR/% V_S
ANALOG INPUT	
Voltage Ranges	
Bipolar	±5V, ±10V
Unipolar	0 to +5V, 0 to +10V
Input Resistance	
0 to +5V	2.5kΩ
0 to +10V, ±5V	5.0kΩ
±10V	10.0kΩ
External Reference Input[3]	
Voltage Range	0 to +12V
Input Resistance	2.5kΩ
DIGITAL INPUT	
Convert Command	Positive Pulse, 100ns Width min Negative Edge Triggered
Logic Loading	1TTL Load
DIGITAL OUTPUT	
Parallel Output Data	
Unipolar	Binary (BIN)
Bipolar	Offset Binary (OBIN) Two's Complement
Output Drive	1TTL Load
Status	Logic "1" During Conversion
Output Drive	1TTL Load
INTERNAL REFERENCE VOLTAGE	+10V, ±0.3%
External Load Current	
(Rated Performance)	2mA max
Temperature Stability	±8.5ppm/°C max
POWER REQUIREMENTS[4]	
Voltage (Rated Performance)	±15V ±3%, +5V ±3%
Voltage (Operating)	±12V to ±17V, +4.75V to +5.25V
Supply Current Drain ±15V	±25mA
+5V	150mA
TEMPERATURE RANGE	
Specified	0 to +70°C
Operating	–25°C to +85°C
Storage	–55°C to +85°C
SIZE	2" X 2" X 0.4" (51 X 51 X 10.4mm)
Weight	1.2 oz (33g)
PRICE	
(1–24)	$199
(25–99)	$169
(100+)	$149

[1] Offset and gain error are adjustable to zero by means of external potentiometers. See Figure 3 for proper connection.
[2] FSR means Full Scale Range.
[3] Rated performance is specified with +10.0V reference.
[4] Recommended Power Supply: Analog Devices Model 923.
Specifications subject to change without notice.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



TERMINAL PINS INSTALLED ONLY IN SHADED HOLE LOCATIONS.

MATING CONNECTORS

AC1577 (2 REQUIRED)

PIN DESIGNATIONS

PIN	FUNCTION	PIN	FUNCTION
1	+5V	32	+15V
2	DIGITAL GROUND	31	–15V
3	MSB	30	ANALOG GROUND
4	MSB	29	ANALOG IN 1
5	BIT 2	28	ANALOG IN 2
6	BIT 3	27	ANALOG IN 3
7	BIT 4	26	+10V REF OUT
8	BIT 5	25	REFERENCE IN
9	BIT 6	24	OFFSET ADJUST
10	BIT 7	23	NOT USED
11	BIT 8	22	STATUS
12	BIT 9	21	CONVERT COMMAND
13	BIT 10	20	NOT USED
14	BIT 11	19	LSB
15	BIT 12	18	BIT 15
16	BIT 13	17	BIT 14

OTHER HIGH RESOLUTION PRODUCTS FROM ANALOG DEVICES:

- 14-Bit/15-Bit Sampling A/D Converters; DAS1152/53
  - 25kHz (14-Bit)/20kHz (15-Bit) throughput rates
  - Second Source to A/D/A/M824 and A/D/A/M825 Modules
- 14-Bit/15-Bit Low Level Data Acquisition Systems: DAS1155/56
  - 25kHz (14-Bit)/20kHz (15-Bit) throughput rates
  - High Performance PGIA (1V/V–1000V/V), SHA and A/D Converter
- 14-Bit Sample-Hold Amplifier: SHA1144
  - Acquisition Time: 8µs max to ±0.003% (20V step)

OPERATION

For operation, the only connections necessary to the ADC1140 are the power supplies, the analog input, the convert command pulse and a connection between pins 25 and 26 in order to supply the internal precision reference voltage to the DAC (see Figure 2). For operation with an external reference see Figure 7.

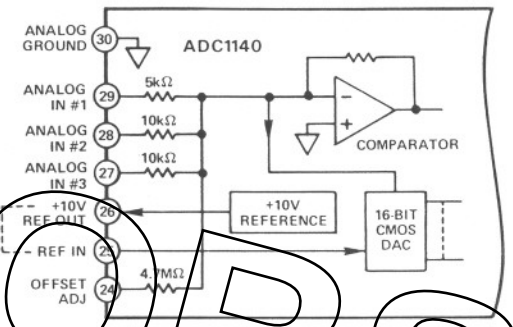


Figure 2. Analog Input Block Diagram

ANALOG INPUT PROGRAMMING

The analog input section consists of three analog input terminals. Analog input range selection is accomplished by pin programming as shown in Table 1.

In the unipolar mode, a 0 to +10V or a 0 to +5V input signal develops a 0 to +2mA current that is compared to the 0 to −2mA (shown in Figure 2) current output of the DAC.

In the bipolar mode, a +1mA offset current from the reference is applied to the comparator input via pin programming connections. The ADC1140 can then accept either ±5V or ±10V inputs. These inputs again will be converted to current and compared with the DAC's 0 to −2mA current output.

Input Signal Range	Coding	Connect Input Signal To Pin(s)	Connect Pin 26 To Pin*	Connect Pin 30 To Pin(s)
±10V	OBIN, Two's Comp	28	27	29, 2
±5V	OBIN, Two's Comp	29	27	28, 2
0 to +5V	BIN	27, 28, 29	Open	2
0 to +10V	BIN	27, 28	Open	29, 2

*If Internal Reference is used, Pins 25 and 26 must be connected together (see Figure 3 and the gain calibration section).

Table 1. Analog Input Voltage Pin Programming

OPTION OFFSET & GAIN CALIBRATION

Initial offset and gain errors can be adjusted to zero by potentiometers as shown in Figure 3. Proper offset and gain calibration requires great care and the use of an accurate and stable voltage reference. The voltage standard used as a signal source must be very stable. It should be capable of being set to within 1μV of the desired value at both ends of its range. The potentiometers selected should be of the good quality Cermet type. Multi-turn potentiometers having ten to fifteen turns and 100ppm/°C temperature coefficients will be adequate. The temperature coefficients contributed by these Cermet potentiometers will be less than 0.1ppm/°C.

By adjusting the offset first, gain and offset adjustments will remain independent of each other.

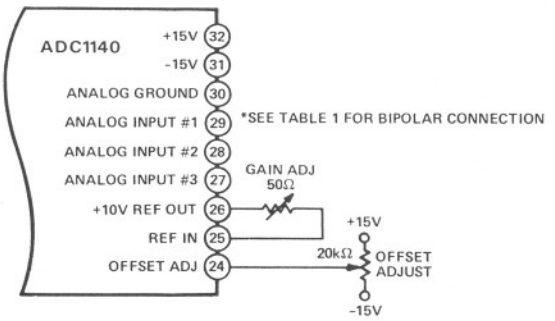


Figure 3. Offset and Gain Calibration

OFFSET CALIBRATION

For 0 to +10V range, set the input voltage precisely to +76μV; for 0 to +5V range, set it at +38μV. Adjust the zero potentiometer until the binary coded converter is just on the verge of switching from 000 . . . 00 to 000 . . . 01.

For ±5V range, set the input voltage precisely to −4.999924V; for ±10V range, set it at −9.999847V. Adjust the zero potentiometer until the offset binary coded units are just on the verge of switching from 000 . . . 00 to 000 . . . 01 and the two's comp. coded units are just on the verge of switching from 100 . . . 0 to 100 . . . 1.

GAIN CALIBRATION

Set the input voltage precisely at +9.99977V for 0 to +10V input range, +4.99977V for ±5V input range, +9.99954V for ±10V input range, or +4.99988V for 0 to +5V input range, adjust the gain potentiometer until binary and offset binary coded units are just on the verge of switching from 111 . . . 0 to 111 . . . 1 and two's comp. coded units are just on the verge of switching from 011 . . . 10 to 011 . . . 11. Note that these values are 1 1/2 LSBs less than nominal full scale.

POWER SUPPLY AND GROUNDING CONNECTIONS

The analog power ground (pin 30) and digital ground (pin 2) are not connected internally. The connection must be made externally. The choice of an optimum "star" point is an important consideration in avoiding ground loops and to minimize coupling between the analog and digital sections. One suggested approach is shown in Figure 4.

Because the ADC1140 contains high quality tantalum capacitors on each of the power supply inputs to ground, external bypass capacitors are not required.

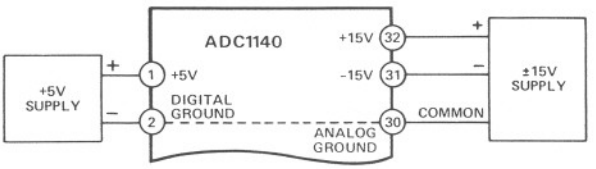


Figure 4. Power Supply and Grounding Techniques

ADC1140 TIMING

Conversion is initiated with the negative going edge of the Convert Command pulse as shown in Figure 5. The Convert Command pulse width must be a minimum of 100ns. Once the conversion process is initiated, it cannot be retriggered until after the end of conversion.

With the negative edge of the Convert Command pulse, all internal logic is reset. The MSB is set low with the remaining digitial outputs set to logic high state, and the status line is set high and remains high thru the full conversion cycle.

During conversion each bit, starting with the MSB, is sequentially switched low at the rising edge of the internal clock. The DAC output is then compared to the analog input and the bit decision is made. Each comparison lasts one clock cycle with the complete 16-bit conversion taking 35μs maximum. At this time, the STATUS line goes low signifying that the low conversion is complete.

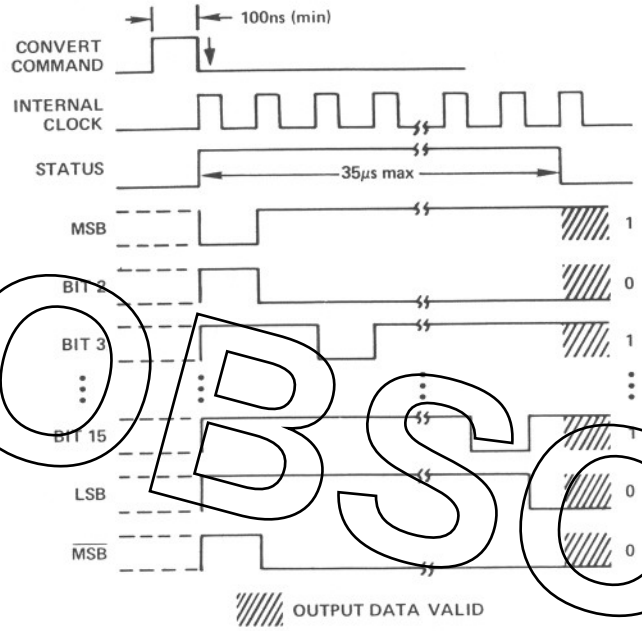


Figure 5. ADC1140 Timing Diagram

ANALOG INPUT/OUTPUT RELATIONSHIPS

The ADC1140 produces a true binary coded output when configured as a unipolar device. Configured as a bipolar device, it can produce either offset binary or two's complement output codes. The most significant bit (MSB) is displayed on pin 4 for the binary and offset binary codes or on pin 3 for the two's complement code. Table 2 shows the unipolar analog input/digital output relationships. Table 3 shows the bipolar analog input/digital output relationships for offset binary code and two's complement codes.

Analog Input 0 to +5V Range	Analog Input 0 to +10V Range	Digital Output Binary Code
+4.999924V	+9.99985V	1111 1111 1111 1111
+2.50000V	+5.00000V	1000 0000 0000 0000
+1.25000V	+2.50000V	0100 0000 0000 0000
+0.62500V	+1.25000V	0010 0000 0000 0000
+0.000076V	+0.000153V	0000 0000 0000 0001
+0.00000V	+0.00000V	0000 0000 0000 0000

Table 2. Unipolar Input/Output Relationships

Analog Input ±5V Range	Analog Input ±10V Range	Digital Output Offset Binary Code	Digital Output 2's Complement Code
+4.99985V	+9.99970V	1111 1111 1111 1111	0111 1111 1111 1111
+2.50000V	+5.00000V	1100 0000 0000 0000	0100 0000 0000 0000
+0.000153V	+0.000305V	1000 0000 0000 0001	0000 0000 0000 0001
+0.00000V	+0.00000V	1000 0000 0000 0000	0000 0000 0000 0000
−5.00000V	−10.00000V	0000 0000 0000 0000	1000 0000 0000 0000

Table 3. Bipolar Input/Output Relationships

HIGH RESOLUTION DATA ACQUISITION SYSTEM

Shown in Figure 6 is a high resolution data acquisition system. Here the SHA1144, a high resolution sample-hold amplifier, is used to drive the ADC1140. Conversion is initiated by the negative edge of the convert command pulse. At this time the STATUS pulse goes low causing the SHA1144 to go from the sample mode to the hold mode. When the conversion is complete, 35μs later, the STATUS pulse goes low, thus placing the SHA1144 in the sample mode.

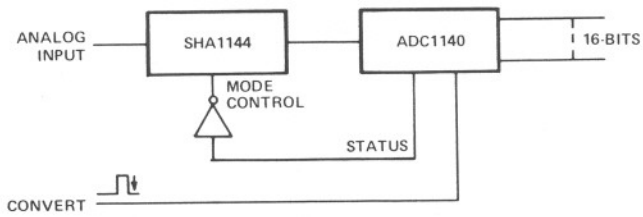


Figure 6. High Resolution Data Acquisition System

EXTERNAL REFERENCE

The ADC1140 is capable of operating with an external +10.0V reference. Simply disconnect the gain trim potentiometer from pin 26 and connect it to the external reference as shown in Figure 7. The external reference output must appear as a low impedance and must remain very stable during conversion to insure that accuracy is maintained. Gain error is adjusted as previously discussed in the gain calibration section.

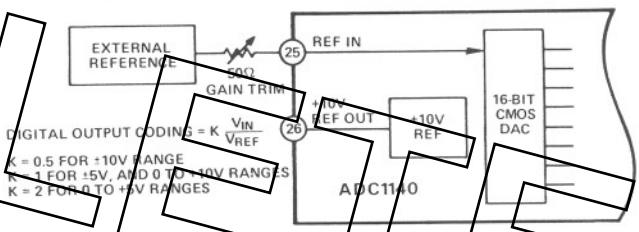


Figure 7. External Reference

The ADC1140 is factory tested and calibrated with the internal +10.0V reference voltage but nonstandard external voltages can be used with the digital output coding being determined by the formula shown in Figure 7.

PIA INTERFACE

The ADC1140 can be used with a PIA to interface directly to a microprocessor. As shown in Figure 8 the 16-bit output of the ADC1140 is split into two 8-bit bytes. Part A of the PIA is programmed to read the eight most-significant-bits while Part B reads the eight least-significant-bits. Output CB2 is used to start the ADC1140 conversion process. CB1, of the PIA, is used to sense the STATUS of the ADC1140 so that the end of conversions can be determined. The control bus, address bus, and data bus are then connected directly to the microprocessor.

With the use of PIAs, control of one or more ADC1140s can be accomplished in many different configurations.

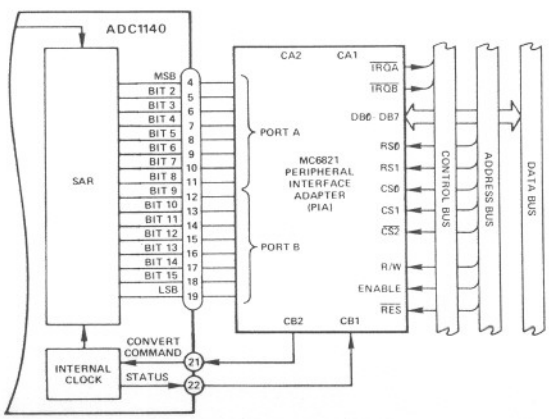


Figure 8. ADC1140 Interface to PIA