MCS9805
PCI to Single Parallel Controller
Datasheet

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1. General Description

The MCS9805CV-BA is a parallel port controller with PCI bus interface. Parallel Port interface in MCS9805CV-BA is an IEEE 1284 compliant SPP / PS2 / EPP / ECP Parallel Port that fully supports Centronics interface.

The MCS9805CV-BA is ideally suited for PC applications, such as Add-On Parallel Ports. It is available in 128-Pin QFP package & fabricated using an advanced submicron CMOS process to achieve low power drain and high-speed requirements.

MCS9805CV-BA is designed to be pin compatible with previous version of MCS9805CV. Existing designs of MCS9805CV can be migrated to MCS9805CV-BA without any modification to system design. Software compatibility is also maintained between MCS9805CV to MCS9805CV-BA.

2. Features

General

- 5V Operation
- Low Power
- Fully compliant with PCI Local Bus Specification 2.3
- Re-map function for Legacy Ports
- Microsoft WHQL Complaint Drivers
- 128 Pin QFP package, RoHS
- Commercial Grade, 0 to 70 deg C
- Advanced testability through scan addition

IEEE1284 Parallel Port

- Multi-mode IEEE1284 compliant controller (SPP, PS2, EPP, ECP)
- Faster data rates up to 1.5Mbytes/sec for Parallel Port

Miscellaneous

- Four -Wire SPI Interface for EEPROM
- EEPROM read through PCI

3. Applications

- Parallel / Printer Port based applications
- Add-On I/O Cards – Parallel
- Embedded systems – For I/O expansion

4. Ordering Information

- Part Number : MCS9805CV-BA
- 128 Pin QFP
- ROHS
- Commercial Grade, 0 to 70 deg C

5. Application Schematic

- PCI to 1 Parallel

6. Evaluation Board

- MCS98XXCV-BA EVB – Combo

7. Software Support

SW Driver Support

- Windows 95/98SE/ME
- Windows 32bit - 2000 /XP /NT /2003 Server
- Windows 64bit XP / 2003 Server
- Windows Vista / 2008 Server (32 & 64 bit)
- Windows 7 (32 & 64 bit)
- Linux Kernel 2.4.X / 2.6.X

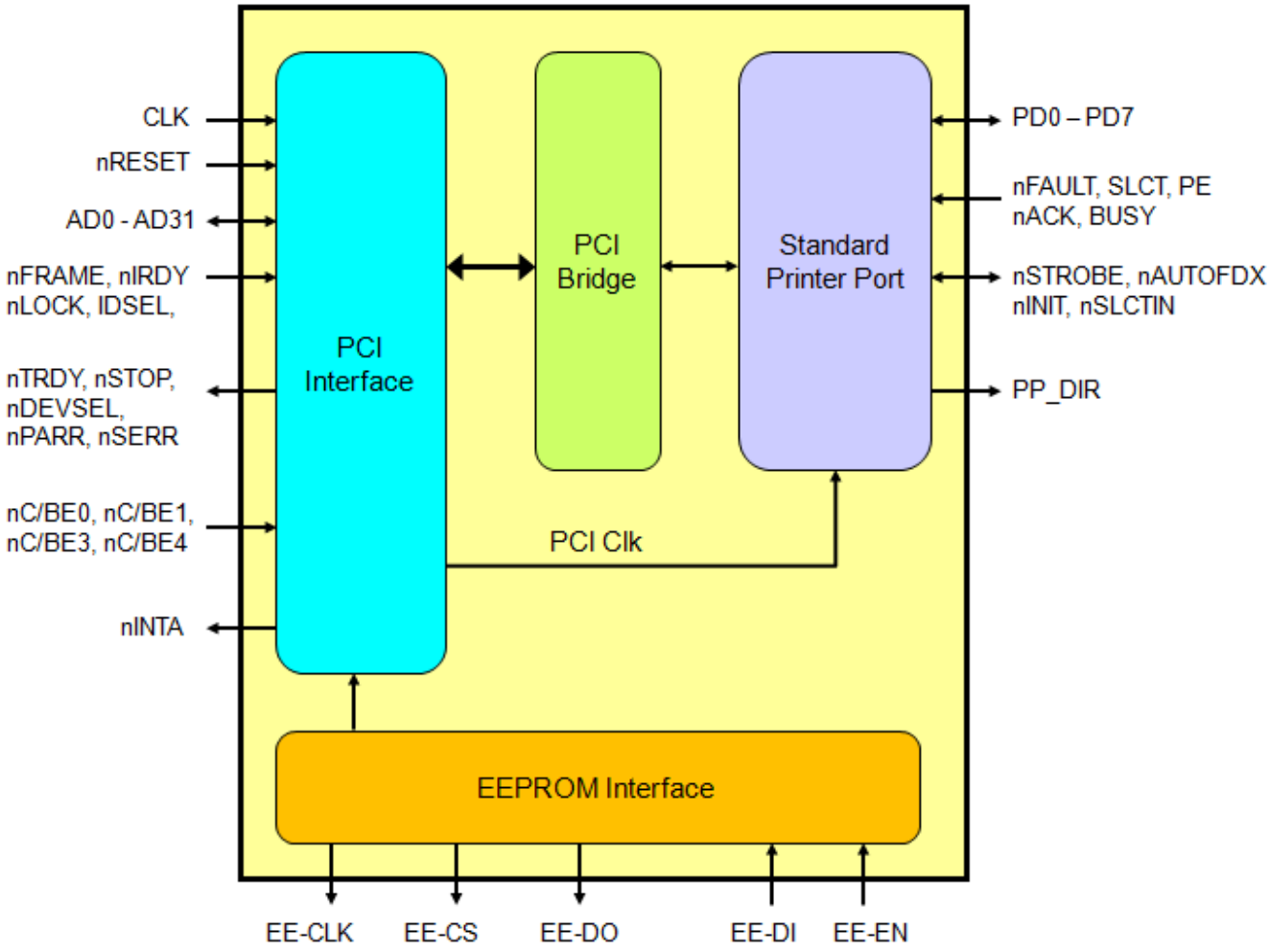
SW Utility Support

- Windows XP based Diagnostic Utility
- DOS based diagnostic Utility

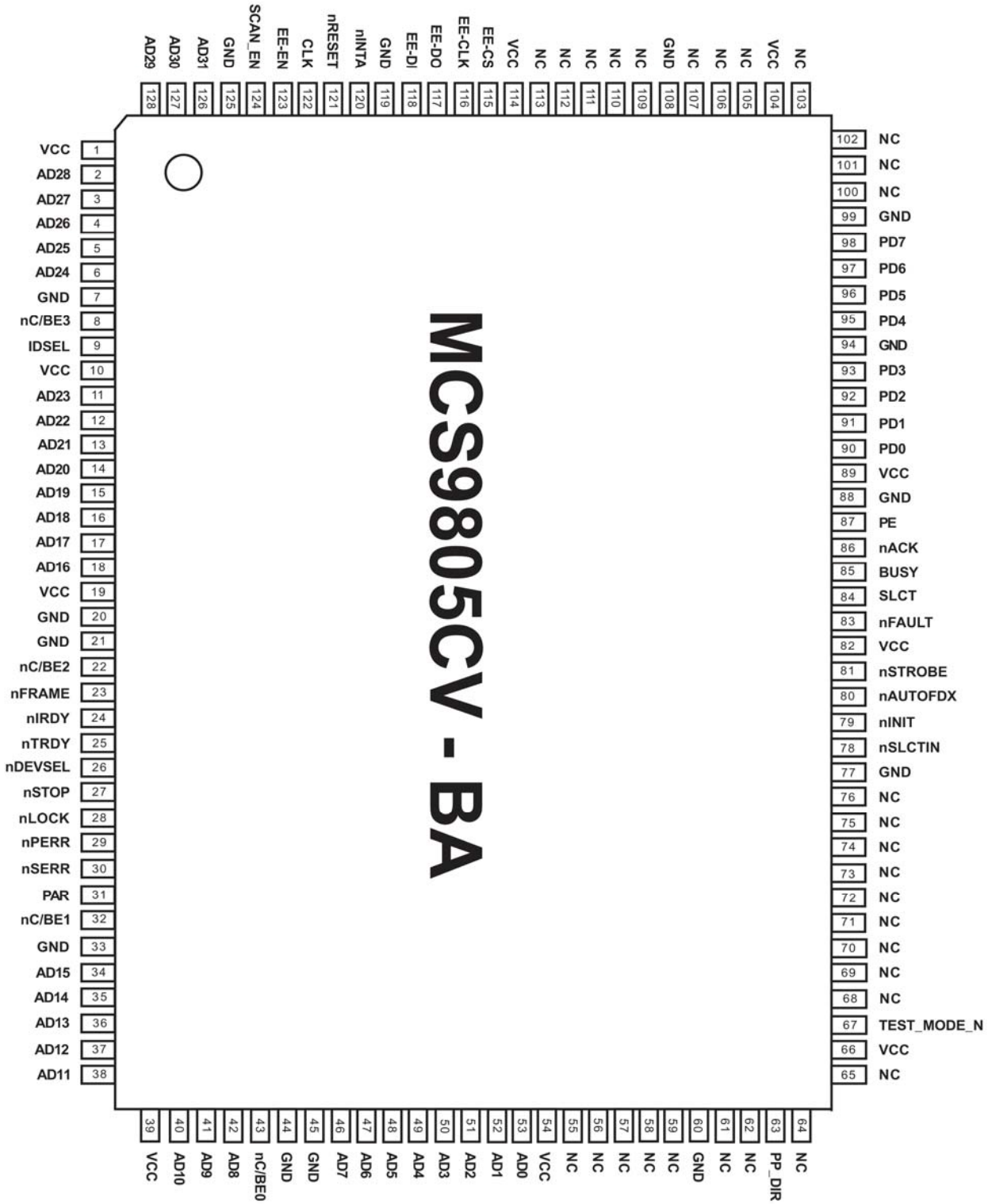
8. Certifications

- WHQL Certification of device drivers for Windows XP, Windows Vista & Windows 7 Operating Systems.

9. Block Diagram



10. Pin Diagram



11. Pin Descriptions

This section provides information on each Pin of MCS9805CV-BA

Name	Pin #	Direction	Drive Strength	Description
CLK	122	I		33 MHz PCI System Clock input.
nRESET	121	I(PU)		PCI system Reset (active low).Resets all internal registers, sequencers, and signals to a consistent state. During reset condition, AD[31-0] and nSERR are tri- stated.
AD[31-29]	126-128	I/O		Multiplexed PCI Address/Data bus. During the address phase, AD[31-0] contain a physical address. Data is stable and valid when nIRDY and nTRDY are asserted (active).
AD[28-24]	2-6	I/O		See AD[31-29] description.
AD[23-16]	11-18	I/O		See AD[31-29] description.
AD[15-11]	34-38	I/O		See AD[31-29] description.
AD[10-8]	40-42	I/O		See AD[31-29] description.
AD[7-0]	46-53	I/O		See AD[31-29] description.
nFRAME	23	I		nFRAME is asserted by the current Bus Master to indicate the beginning of an transfer. nFRAME remains active until the last Byte of the transfer is to be processed.
nIRDY	24	I		Initiator Ready. During a write, nIRDY asserted indicates that the initiator is driving valid data onto the data bus. During a read, nIRDY asserted indicates that the initiator is ready to accept data from the target device.
nTRDY	25	O		Target Ready (three-state). Asserted when the target is ready to complete the current data phase.
nSTOP	27	O		Asserted to indicate that the target wishes the initiator to stop the transaction in progress on the current data phase.

Name	Pin #	Direction	Drive Strength	Description
nLOCK	28	I		Indicates an atomic operation that may require multiple transactions to complete.
IDSEL	9	I		Initialization Device Select. Used as a chip select during configuration read and write transactions.
nDEVSEL	26	O		Device Select (three-state). Asserted when the target has decoded one of its addresses.
nPERR	29	I/O		Parity Error (three-state). Used to report parity errors during all PCI transactions except a special cycle. The minimum duration of nPERR is one clock cycle.
nSERR	30	O		System Error (open drain). This pin goes low when address parity errors are detected.
PAR	31	I/O		Parity. Even Parity is applied across AD31-0 and nC/BE3-0. PAR is stable and valid one clock after the address phase. For the data phase, PAR is stable and valid one clock after either nIRDY is asserted on a write transaction, or nTRDY is asserted on a read transaction.
nC/BE3	8	I		Bus Command and Byte Enable. During the address phase of a transaction, nC/BE3-0 defines the bus command. During the data phase, nC/BE3-0 are used as Byte Enables. nC/BE3 applies to Byte “3”.
nC/BE2	22	I		Bus Command and Byte Enable. During the address phase of a transaction, nC/BE3-0 defines the bus command. During the data phase, nC/BE3-0 is used as Byte Enables. nC/BE2 applies to Byte “2”.
nC/BE1	32	I		Bus Command and Byte Enable. During the address phase of a transaction, nC/BE3-0 defines the bus command. During the data phase, nC/BE3-0 are used as Byte Enables. nC/BE1 applies to Byte “1”.
nC/BE0	43	I/O		Bus Command and Byte Enable. During the address phase of a transaction, nC/BE3-0 defines the bus command. During the data phase, nC/BE3-0 are used as Byte Enables. nC/BE0 applies to Byte “0”.
nINTA	120	O		PCI active low interrupt output (open-drain). This signal goes low (active) when an interrupt condition occurs.

Name	Pin #	Direction	Drive Strength	Description
EE-CS	115	O	4mA	External EEPROM chip select (active high). After Power-On Reset, the EEPROM is read, and the read-only configuration registers are filled sequentially from the first 64 Bytes in the EEPROM.
EE-CLK	116	O	4mA	External EEPROM clock.
EE-DI	118	I		External EEPROM data input.
EE-DO	117	O	4mA	External EEPROM data output.
EE-EN	123	I(PU)		Enable EEPROM (active high, internal pull-up). The external EEPROM can be disabled when this pin is tied to GND or pulled low. When the EEPROM is disabled, default values for PCI configuration registers will be used.
SLCT	84	I(PU)		Peripheral/printer selected (internal pull-up). This pin is set high by peripheral/printer when it is selected.
PE	87	I(PU)		Paper Empty (internal pull-up). This pin is set high by Peripheral / Printer to indicate Paper Empty condition.
BUSY	85	I(PU)		Peripheral/printer Busy (internal pull-up). This pin is set high by peripheral/printer, when printer or peripheral is not ready to accept data.
nACK	86	I(PU)		Peripheral/printer data Acknowledge (internal pull-up). This pin is set low by peripheral/printer to indicate a successful data transfer has taken place.
nFAULT	83	I(PU)		Peripheral/printer Data Error (internal pull-up). This pin is set low by peripheral/printer during an error condition.
nSTROBE	81	OD_O (PU)	12mA	Peripheral/printer data Strobe (open drain, active low). When low, data is latched into the printer.
nAUTOFDX	80	OD_O (PU)	12mA	Peripheral/printer Auto Feed (open-drain, active low). Continuous auto fed paper is selected when this pin is set low.
nINIT	79	OD_O (PU)	12mA	Initialize the peripheral/printer (open drain, active low). When set low, the peripheral/printer starts its initialization routine.

Name	Pin #	Direction	Drive Strength	Description
nSLCTIN	78	OD_O (PU)	12mA	Peripheral/printer Select (open-drain, active low). Selects the peripheral/printer when it is set low.
PD[7-4]	98-95	I/O	12mA	Peripheral / Printer bi-directional data bus
PD[3-0]	93-90	I/O	12mA	Peripheral / Printer bi-directional data bus
Test_Mode_N	67	I(PU)		Reserved.
PP_DIR	63	O	4mA	For direction control, when used with External IEEE1284 transceivers. Leave it as “NC” if not used
SCAN_EN	124	I(PD)		Reserved.
NC	55,56,57, 58,59,61, 62,64,65, 68,69,70, 71,72,73, 74,75,76, 100,101, 102,103, 105,106, 107,109, 110,111, 112,113			No Connection
GND	7,20,21, 33, 44,45, 60,77,88, 94,99, 108,119, 125	Gnd		Power and Signal Ground.
Vcc	1,10,19, 39, 54,66, 82, 89, 104, 114	Pwr		Supply Voltage 5V

Note: -

I(PU) - Input – Internal Pull Up
I(PD) - Input – Internal Pull Down
O(PU) - Output – Internal Pull Up
OD_O (PU) - Open Drain Output – Internal Pull Up
I/O - - Bi-directional Signal
Pwr - Power
Gnd - Ground

12. Architectural overview

Architecture of MCS9805CV-BA is mainly divided into three blocks

- PCI core
- Parallel Port core
- EEPROM Interface

12.1 PCI Core

12.1.1 PCI Bus Operation

The execution of PCI Bus transactions take place in broadly five stages: address phase; transaction claiming; data phase(s); final data transfer; and transaction completion.

12.1.2 Address Phase

Every PCI transaction starts with an address phase, one PCI clock period in duration. During the address phase the initiator (also known as the current Bus Master) identifies the target device (via the address) and type of transaction (via the command). The initiator drives the 32-bit address onto the Address/Data Bus and a 4-bit command onto the Command/Byte-Enable Bus. The initiator also asserts the nFRAME signal during the same clock cycle to indicate the presence of valid address and transaction information on those buses. The initiator supplies the starting address and command type for one PCI clock cycle. The target generates the subsequent sequential addresses for burst transfers. The Address/Data Bus becomes the Data Bus, and the Command/Byte-Enable Bus becomes the Byte-Enable Bus for the remainder of the clock cycles in that transaction. The target latches the address and command type on the next rising edge of PCI clock, as do all other devices on that PCI bus. Each device then decodes the address and determines whether it is the intended target, and also decodes the command to determine the type of transaction.

12.1.3 Claiming the transaction

When a device determines that it is the target of a transaction, it claims the transaction by asserting nDEVSEL.

12.1.4 Data Phase(s)

The data phase of a transaction is the period during which a data object is transferred between the initiator and the target. The number of data Bytes to be transferred during a data phase is determined by the number of Command/Byte-Enable signals that are asserted by the initiator during the data phase. Each data phase is at least one PCI clock period in duration. Both initiator and target must indicate that they are ready to complete a data phase. If not, the data phase is extended by a wait state of one clock period in duration. The initiator and the target indicate this by asserting nIRDY and nTRDY respectively and the data transfer is completed at the rising edge of the next PCI clock.

12.1.5 Transaction Duration

The initiator, as stated earlier, gives only the starting address during the address phase. It does not tell the number of data transfers in a burst transfer transaction.

The target will automatically generate the addresses for subsequent Data Phase transfers. The initiator indicates the completion of a transaction by asserting nIRDY and de-asserting nFRAME during the last data transfer phase. The transaction does not actually complete until the target has also asserted the nTRDY signal and the last data transfer takes place. At this point the nTRDY and nDEVSEL are de-asserted by the target.

12.1.6 Transaction Completion

When all of nIRDY, nTRDY, nDEVSEL, and nFRAME are in the inactive state (high state), the bus is in idle state. The bus is then ready to be claimed by another Bus Master.

12.1.7 PCI Resource Allocation

PCI devices do not have “Hard-Wired” assignments for memory or I/O Ports like ISA devices do. PCI devices use “Plug & Play” to obtain the required resources each time the system boots up. Each PCI device can request up to six resource allocations. These can be blocks of memory (RAM) or blocks of I/O Registers. The size of each resource block requested can also be specified, allowing great flexibility. Each of these resource blocks is accessed by means of a Base-Address-Register (BAR). As the name suggests, this is a pointer to the start of the resource. Individual registers are then addressed using relative offsets from the Base-Address-Register contents. The important thing to note is: plugging the same PCI card into different machines will not necessarily result in the same addresses being assigned to it. For this reason, software (drivers, etc.) must always obtain the specific addresses for the device from the PCI System.

Each PCI device is assigned an entry in the PCI System’s shared “Configuration Space”. Every device is allocated 256 Bytes in the Configuration Space. The first 64 Bytes must follow the conventions of a standard PCI Configuration “Header”. There are several pieces of information the device must present in specific fields within the header to allow the PCI System to properly identify it. These include the Vendor-ID, Device-ID and Class-Code. These three fields should provide enough information to allow the PCI System to associate the correct software driver with the hardware device. Other fields can be used to provide additional information to further refine the needs and capabilities of the device.

As part of the Enumeration process (discovery of which devices are present in the system) the Base-Address-Registers are configured for each device. The device tells the system how many registers (etc.) it requires, and the system maps that number into the system’s resource space, reserving them for exclusive use by that particular device. No guarantees are made that any two requests for resources will have any predictable relationship to each other. Each PCI System is free to use its own allocation strategy when managing resources.

12.1.8 Multi-Function Devices

ASIX uses the Subsystem-ID field to indicate how many Serial Ports and Parallel Ports are provided by the current implementation. By changing the data in the Subsystem-ID field, and stuffing only the appropriate number of external components, the same board could be used for products with either one or two Ports. The least significant Hexadecimal digit of the Subsystem-ID field indicates the number of Serial Ports that are currently being provided by the device.

The next higher digit indicates the number of Parallel Ports being provided. The table below shows several different combinations and the types of Ports that would be enabled. Some ASIX devices provide Serial Ports, some provide Parallel Ports, and some provide both types of Ports. This field is used as an aid to the software Drivers, allowing them to easily determine how many of each Port type to configure.

Subsystem-ID	Parallel Ports	Serial Ports
0001	0	1
0010	1	0
0012	1	2

This use of the term “Multi-Function Device” should not be confused with the more generic use of that term by the PCI System. Each “Function” within a “Unit” (physical device) gets its own Configuration Space Header. ASIX’s devices do not need this extra layer of complexity, the six Base Address Registers provided by one PCI “Function” are more than adequate to allocate all of the desired resources.

12.1.9 PCI Configuration Space Header

Default values for several key fields are shown in the table below.

AD 31-24	AD 23-16	AD 15-8	AD 7-0	Offset(Hex)
Device ID (9805)		Vendor ID (9710)		00
Status		Command		04
Class Code (078000)			Revision ID (01)	08
BIST	Header Type	Latency Timer	Cache Size (08)	0C
Base Address Register (BAR) 0 – “Standard Registers” (Y)				10
Base Address Register (BAR) 1 –“Extended Registers” (W)				14
Reserved				18
Reserved				1C
Reserved				20
Reserved				24
Reserved				28
Subsystem ID (0010)		Subsystem Vendor ID (1000)		2C
Reserved				30
Reserved				34
Reserved				38
Max Latency (00)	Min Grant (00)	Interrupt Pin (01)	Interrupt Line	3C
Reserved		Loading Timers		40
EEPROM Register				44
raidreg2	raidreg1	4’h0	Test Bus Sel	16’h9710	48

Internal Address Select Configuration

The MCS9805 uses two Base Address Registers.
These essentially act as internal “Chip Select” logic.
Registers are addressed by using one of the Base Addresses plus an offset.

BAR	I/O Address offset	Function
0 (Y)	00-07	Standard Parallel Port Registers
1 (W)	00	Configuration Register A
1 (W)	01	Configuration Register B
1 (W)	02	Extended Control Register (ECR)

12.2 Parallel Port

In computing, a parallel port is a type of physical interface used in conjunction with a cable to connect separate peripherals in a computer system. In Parallel Port, binary information is transferred in parallel: each bit in a particular value is sent simultaneously as an electrical pulse across a separate wire, in contrast to a serial port, which requires each bit to be sent in series over a single wire. The number of wires and the type of connector on a parallel port can vary.

The IEEE 1284 standard, which is an extension of the legacy unidirectional parallel port, allows for faster throughput and bi-directional data flow with a theoretical maximum throughput of 4 Megabits per second, with actual around 2 Megabits per second depending on hardware. The parallel port, as implemented on the PC, consists of a connector with 17 signal lines and 8 ground lines. The signal lines are divided into three groups:

- Control (4 lines)
- Status (5 lines)
- Data (8 lines)

As originally designed, the Control lines are used for interface control and handshaking signals from the PC to the printer. The Status lines are used for handshake signals and as status indicators to do operations such as paper empty, busy indication and interface or peripheral errors. The data lines are used to provide data from the PC to the printer, in that direction only. Later implementations of the parallel port allowed for data to be driven from the peripheral to the PC also.

Parallel port implemented in MCS9805CV-BA is compliant to IEEE 1284 Standard Parallel Port and supports various IEEE 1284 modes through hardware. Following are the Parallel modes of operation supported.

- SPP / Centronics / Compatibility Mode
- Nibble Mode
- Byte Mode (PS/2)
- Enhanced Parallel Port (EPP 1.9)
- Extended Capability Port (ECP) with and without RLE

12.2.1 SPP/Centronics/Compatibility Mode

This mode operates in the forward direction only. The DIR bit is forced to “1” and PD[7:0] are always set to the output direction. All control signals are under software control. This mode operation is used in most standard parallel ports on PC’s, for data transfer to printer. Data is placed on the PD[7:0] pins and printer status is checked via the DSR register. If no error condition is flagged and the printer is not busy, software toggles the nSTROBE pin to latch the PD[7:0] data into the printer. The printer acknowledges data receipt pulsing the nACK and BUSY pins.

12.2.2 Nibble Mode

The Nibble mode is the most common way to get reverse channel data from a printer or peripheral. This mode is usually combined with the SPP mode to create a bi-directional channel. Printer status bits are used as nibble bits for the reverse channel data. The same status bits are used for each nibble, so special handshaking is required. When both nibbles have been received, the PC must combine them to form the intended byte if data.

Bits used for Nibble Mode:

Pin	Data Bit
BUSY	Bit-7
PE	Bit-6
SLCT	Bit-5
nFAULT	Bit-4
BUSY	Bit-3
PE	Bit-2
SLCT	Bit-1
nFAULT	Bit-0

12.2.3 Byte Mode (PS/2)

The Byte Mode protocol is used to transfer bi-directional data via the PD[7:0] Pins. The FIFO is not used in this mode. The direction of the port is controlled with the DIR bit in the DCR register. Byte Mode (PS/2) uses the same handshaking protocol as SPP Mode for data transfer.

12.2.4 Extended Capability Port(ECP)

ECP Mode is an advanced mode for communication with printers or peripherals. A 16-Byte FIFO provides a high performance bi-direction communication path. The following cycle types are provided in both the forward and reverse directions.

- Data Cycle
- Command Cycle
- Run-Length-Encoding(RLE)
- Channel Address

Run Length Encoding (RLE) provides data compression of up to 64:1. This is particularly useful for printers and peripherals that transfer raster images with long strings of identical data. In order for RLE to be enabled, both the Host and Peripheral must support this feature. Channel addressing supports multiple logical devices within a single physical unit, like Scanner / Fax / Printer in one physical Package.

12.2.5 Enhanced Parallel Port Mode(EPP)

In EPP Mode several control signals are used for different purposes than those described for the default SPP & PS/2 Modes. The nSLCTIN line is used as an “ADDRESS STROBE” and nAUTOFDX is used as the Data Strobe signal. The appropriate strobe signal is automatically generated when data is read or written to one of the EPP specific registers. The nSTROBE is re-defined to indicate whether the current transfer is a write or read cycle. Separate I/O addresses are defined for “Data” and “Address” access and when these locations are used, handshaking is performed automatically by the chip.

12.2.6 FIFO Test Mode

In this mode the FIFO can be written and read, but no data will be transmitted to the printer. Whatever data is in the FIFO may be output on the PD[7:0] Pins, but no control signal will be generated to signal a transfer is to take place. All the status flags are optional in this mode, so the complete operation of the FIFO can be observed without actually affecting the external device.

12.2.7 Config A/B Enable Mode

This mode must be selected whenever the Config-A or Config-B registers are accessed. The Config-A register uses the same I/O Address as the FIFO Register. Only allowing access to the Configuration Registers when this special Mode is selected prevents the two registers from interfering with each other.

12.2.8 Mode Changes

After hardware reset, PS/2 mode is selected as the default mode. When changing to a different mode, it
is necessary to select mode 000 or 001 first, then any other desired mode can be selected.

12.3. External EEPROM

Data is read from the EEPROM immediately after a Hardware Reset, and the values obtained are used to update the Configuration before the PCI System first sees the device on the Bus. This allows a OEM Customers to customize the vendor and product ID's in place of ASIX ID's. EEPROM can be used to arrive at different product combination by setting appropriate sub-system ID's. For this EE-EN (Pin#123) to be left as No Connect at system level.

If external EEPROM is disabled by connecting the EE-EN (Pin#123) to ground, after hardware reset default values of configuration are loaded by the ASIC.

Following are main features of Serial EEPROM Interface :

- Supports Serial EEPROM of 1K Bit Size with 16bit communication capability
- Configuration Space contents can be modified through EEPROM
- Changing configuration values, different modes can be selected
- Inter Character Gap in multiples of 1bit duration can be set for UART-A & UART-B

Following EEPROM types confirmed at ASIX with MCS9805 **:**

- Atmel AT93LC46B, AT93C46B
- MICROCHIP 93LC46B, 93AA46B, 93AA46C
- ST Micro Electronics M93C46-WMN

13. Extended Modes through EEPROM

Mode supported by MCS9805 configuration without using external EEPROM.

- PCI to 1 Parallel

Vendor ID and Product ID customizations can also be implemented in MCS9805, through external EEPROM. Any change of Vendor ID, Product ID information requires customized device driver.

Note : EEPROM need to be programmed in external EEPROM burner

14. EEPROM Contents

Contents of the EEPROM (16-bit), values shown below are for 1P Mode

EEPROM ADDRESS LOCATION	HEX Data (Word)	Description of Contents	EEPROM ADDRESS LOCATION	HEX Data (Word)	Description of Contents
0x00	9805	Device ID(changes according to mode)	0x20	0000	
0x01	0000		0x21	0000	
0x02	9710	Vendor ID	0x22	0000	
0x03	0000		0x23	0000	
0x04	0000	{Intr_mask_reg[15:8], icg_reg1[7:0]}	0x24	0000	
0x05	0000		0x25	0000	
0x06	0000		0x26	0000	
0x07	0000		0x27	0000	
0x08	0780	Class code(23-8)	0x28	0000	
0x09	0000		0x29	0000	
0x0A	0001	{class code (7-0), Revision ID }	0x2A	0000	
0x0B	0000		0x2B	0000	
0x0C	0000	Header	0x2C	0010	Subsystem ID (Changes according to mode)
0x0D	0000		0x2D	0000	
0x0E	0000		0x2E	1000	Subsystem Vendor ID
0x0F	0000		0x2F	0000	
0x10	0000	ICG_reg2[7:0]	0x30	0000	
0x11	0000		0x31	0000	
0x12	0000		0x32	0000	
0x13	0000		0x33	0000	
0x14	0000		0x34	0000	
0x15	0000		0x35	0000	
0x16	0000		0x36	0000	

EEPROM ADDRESS LOCATION	HEX Data (Word)	Description of Contents	EEPROM ADDRESS LOCATION	HEX Data (Word)	Description of Contents
0x17	0000		0x37	0000	
0x18	0000		0x38	0000	
0x19	0000		0x39	0000	
0x1A	0000		0x3A	0000	
0x1B	0000		0x3B	0000	
0x1C	0000		0x3C	0000	{Max_lat[7:0], Min_gnt [7:0]}
0x1D	0000		0x3D	0000	
0x1E	0000		0x3E	0100	Interrupt Pin
0x1F	0000		0x3F	0000	

EEPROM Data Configuration Values

Description	EEPROM Address Location	Word/Byte Data
Device ID	0x00	9805
Vendor ID	0x02	9710
Class code	0x08	0780
Class code Interface	0x0A (Most Significant Byte)	00
Revision ID	0x0A (Least Significant Byte)	01
Header	0x0C (Least Significant Byte)	00
Subsystem ID	0x2C	0012
Subsystem Vendor ID	0x2E	1000
Interrupt pin	0x3E (Most Significant Byte)	01
Icg_reg1[7:0] Inter Character Gap setting register for UART-A	0x04(Least Significant Byte)	00 (This value is used to put the delay between each character).
Icg_reg2[7:0] Inter Character Gap setting register for UART-B	0x10(Least Significant Byte)	00 (This value is used to put the delay between each character).
Intr_mask_reg[15:8]	0x04(Most Significant Byte)	00

Icg_reg1 & 2 : Inter Character Gap register is used to set Inter Character Gap in multiples of 1bit duration for UART-A & B Ports

Intr_mask_reg[15:0] : Interrupt Mask Register can be used to mask the interrupt from unused Serial or Paralle ports.

Register(bit)	Value(Default for 2S+ 1P)	Description
Intr_mask_reg[8]	0	UART-A Interrupt Mask register. By setting this bit to “1” interrupts can be disabled from this Port.
Intr_mask_reg[9]	0	UART-B Interrupt Mask register. By setting this bit to “1” interrupts can be disabled from this Port.
Intr_mask_reg[11]	0	Parallel Port Interrupt Mask register. By setting this bit to “1” interrupts can be disabled from this Port.

The EEPROM controller reads the least significant byte and then the most significant byte in the 16-bit format. Therefore, when writing to each address in the EEPROM, the least significant byte must be written first, followed by the most significant byte. For example, to write 9805 into address 0x00, the value would be written as 05 98, where 05 is the least significant byte and is written first.

15. Electrical Specifications

Absolute Maximum Ratings

Supply Voltage	6 Volts
Voltage at any pin	GND - 0.3 V to VCC + 0.3 V
Operating Temperature	0 °C to +70 °C
Storage Temperature	-40 °C to +150 °C
ESD HBM (MIL-STD 883E Method 3015-7 Class 2)	2000V
ESD MM (JEDEC EIA/JEDS22 A115-A)	200V
CDM (JEDEC JEDS22 C101-A)	500V
Latch up (JESD No. 78, March 1997)	200 mA, 1.5 x Vcc

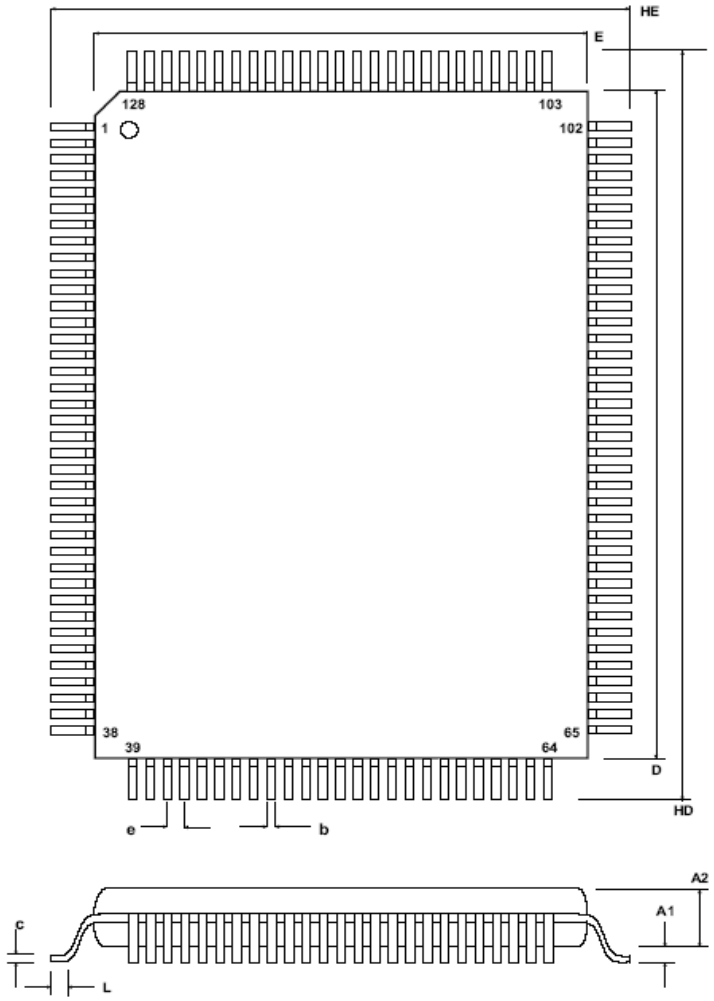
Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit	Condition
Vcc	Supply Voltage	4.75	5	5.25	V	
Vin	Input Voltage	0		Vcc		
Icc	Operating Current		70		mA	No Load

DC Electrical Characteristics: Ta = 0 to +70 °C, VCC = 4.75 to 5.25 V unless otherwise specified.

Symbol	Parameter	Min	Typ	Max	Unit	Condition
ViL	Input Voltage (Low)			0.3 *Vcc	V	CMOS
ViH	Input Voltage (High)	0.7 *Vcc			V	CMOS
ViL	Input Voltage (Low)			0.8	V	TTL
ViH	Input Voltage (High)	2.0			V	TTL
Vt-	Schmitt Trigger Negative-Going Threshold Voltage		1.84		V	CMOS
Vt+	Schmitt Trigger Positive-Going Threshold Voltage		3.22		V	CMOS
Vt-	Schmitt Trigger Negative-Going Threshold Voltage		1.10		V	TTL
Vt+	Schmitt Trigger Positive-Going Threshold Voltage		1.87		V	TTL
VoL	Output Voltage (Low)			0.4	V	IoL = 2 to 24 mA
VoH	Output Voltage (High)	3.5			V	IoH = 2 to 24mA
Ri	Input Pull-Up/Pull-Down Resistance		50		KΩ	ViL = 0V or ViH = Vcc

16. Mechanical Specifications – QFP 128



128-Pin QFP
Package Dimensions

Symbol	Millimeters		
	Min	Typ	Max
A1	0.10		0.30
A2	2.73		2.97
b	0.17		0.27
c	0.09		0.20
e		0.50	
L	0.70		1.03
HD	23.00		23.40
D	19.90		20.10
HE	17.00		17.40
E	13.90		14.10

Revision History

Revision	Date	Comment
0.1	09th May 2008	Initial release
1.0	1st May 2008	"Tentative Data Sheet" text removed in all pages & document version changed to 1.0
1.1	9th March 2010	SW Support updated for Windows 7 and & WHQL drivers availability
2.00	2011/08/05	1. Changed to ASIX Electronics Corp. logo, strings and contact information. 2. Added ASIX copyright legal header information. 3. Modified the Revision History table format. 4. Updated the block diagram in Section 9.

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