

# CHT-7408 DATASHEET

Revision: 03.3  
1-Oct-12  
(Last Modified Date)

## High-Temperature, Quad 2-Inputs AND Gate

### General Description

The CHT-7408 contains four independent 2-inputs AND gates, performing the Boolean function :

$$Y = A \cdot B$$

This circuit is designed assuring latchup-free operation for all supply and temperature conditions.

The CHT-7408 can operate with supply voltages from 3.3 to 5V ( $\pm 10\%$ ).

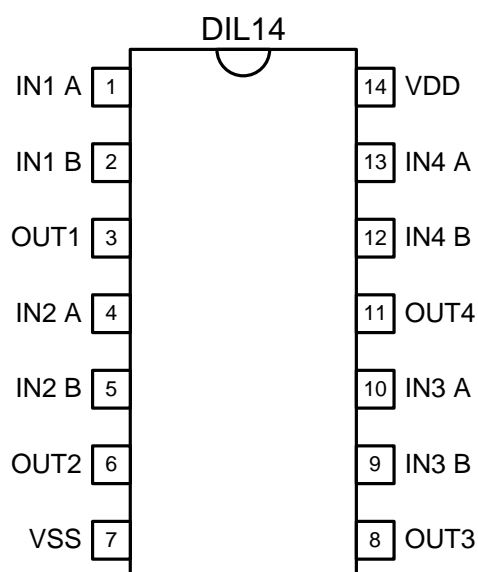
### Features

- Qualified from -55 to +225°C (Tj)
- 3.3 to 5V ( $\pm 10\%$ ) supply voltages
- Latchup-free at any supply and temperature condition
- Validated at 225°C for 30000 hours (CDIL14) and 20000 hours (CSOIC16) (and still on-going)
- Available in DIL14 and CSOIC16 hermetic standard package

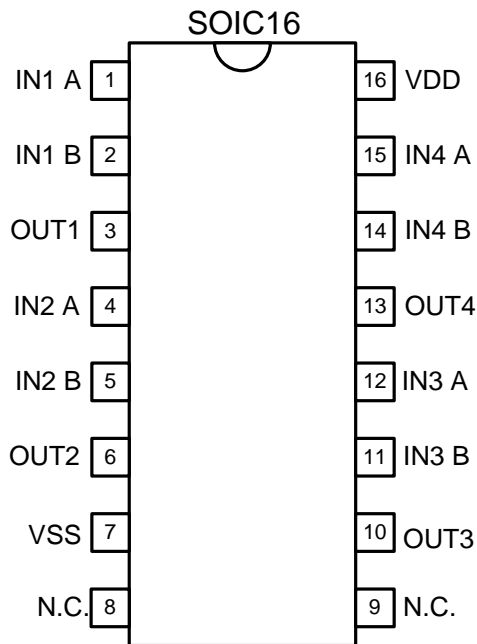
### Applications

- Well logging,
- Automotive, Aeronautics & Aerospace
- Harsh Environments

### Package and Pin Configuration



Pin	Symbol	Description
1	IN1 A	Input A of the AND gate number 1
2	IN1 B	Input B of the AND gate number 1
3	OUT1	Output of the AND gate number 1
4	IN2 A	Input A of the AND gate number 2
5	IN2 B	Input B of the AND gate number 2
6	OUT2	Output of the AND gate number 2
7	VSS	Circuit core ground terminal.
8	OUT3	Output of the AND gate number 3
9	IN3 B	Input B of the AND gate number 3
10	IN3 A	Input A of the AND gate number 3
11	OUT4	Output of the AND gate number 4
12	IN4 B	Input B of the AND gate number 4
13	IN4 A	Input A of the AND gate number 4
14	VDD	Circuit core power supply terminal.



Pin	Symbol	Description
1	IN1 A	Input A of the AND gate number 1
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3	OUT1	Output of the AND gate number 1
4	IN2 A	Input A of the AND gate number 2
5	IN2 B	Input B of the AND gate number 2
6	OUT2	Output of the AND gate number 2
7	VSS	Circuit core ground terminal.
8	N.C.	No connected terminal.
9	N.C.	No connected terminal.
10	OUT3	Output of the AND gate number 3
11	IN3 B	Input B of the AND gate number 3
12	IN3 A	Input A of the AND gate number 3
13	OUT4	Output of the AND gate number 4
14	IN4 B	Input B of the AND gate number 4
15	IN4 A	Input A of the AND gate number 4
16	VDD	Circuit core power supply terminal.

**Function Table**

INPUT		OUTPUT
A	B	Y
L	L	L
L	H	L
H	L	L
H	H	H

**Function and Logical Diagrams**

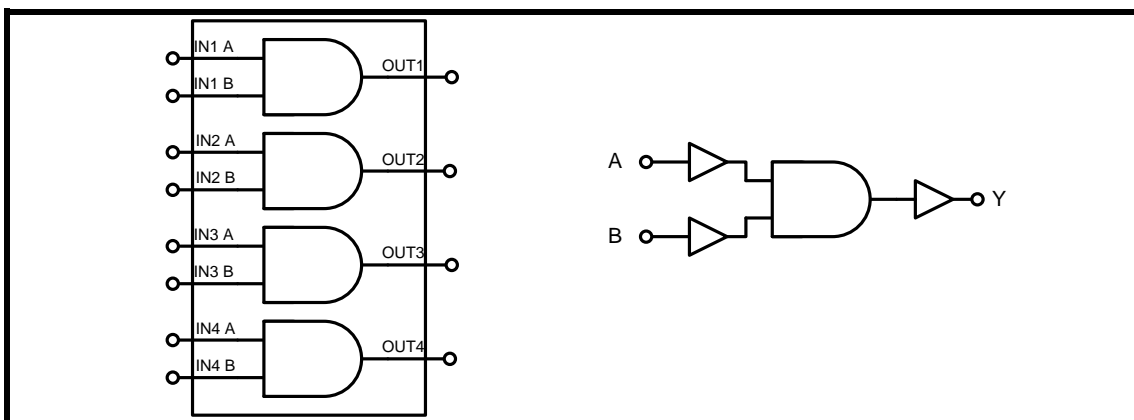


Figure 1. CHT-7408: simplified block diagram.

**Absolute Maximum Ratings**

 Supply Voltage  $V_{DD}$  to GND -0.7 to 6.0V  
 Voltage on any Pin to GND -0.5 to  $V_{DD}+0.5V$ 
**Operating Conditions**

 Supply Voltage  $V_{DD}$  to GND 3.3V to 5V ( $\pm 10\%$ )  
 Junction temperature -55°C to +225°C

**ESD Rating (expected)**

Human Body Model 1kV

**DC Electrical Characteristics**

 Unless otherwise stated:  $V_{DD}=5V$ ,  $T_j=25^\circ C$ . **Bold underlined** figures indicate values valid over the whole temperature range ( $-55^\circ C < T_j < +225^\circ C$ ).

Parameter	Condition	Min	Typ	Max	Units
Supply voltage $V_{DD}$		2.97		5.5V	V
Quiescent current $I_{DD}$	$V_{DD} = 3.3V$ , $T_j = -55^\circ C$			4	nA
	$V_{DD} = 5V$ , $T_j = -55^\circ C$			13	
	$V_{DD} = 3.3V$ , $T_j = 225^\circ C$			<b><u>2990</u></b>	
	$V_{DD} = 5V$ , $T_j = 225^\circ C$			<b><u>3500</u></b>	
Minimum HIGH level output voltage $V_{OH}$	$V_{DD} = 3.3V$ , $I_{OH} < 4mA$ (source)	<b><u>2.7</u></b>	3.04		V
	$V_{DD} = 5V$ , $I_{OH} < 4mA$ (source)	<b><u>4.6</u></b>	4.82		
Maximum LOW level output voltage $V_{OL}$	$V_{DD} = 3.3V$ , $I_{OL} < 4mA$ (sink)		0.28	<b><u>0.5</u></b>	V
	$V_{DD} = 5V$ , $I_{OL} < 4mA$ (sink)		0.20	<b><u>0.4</u></b>	
Minimum HIGH level input voltage $V_{IH}$	$V_{DD} = 3.3V$	<b><u>2.4</u></b>	2.10		V
	$V_{DD} = 5V$	<b><u>3.7</u></b>	3.49		
Maximum LOW level input voltage $V_{IL}$	$V_{DD} = 3.3V$		1.72	<b><u>1.5</u></b>	V
	$V_{DD} = 5V$		2.16	<b><u>2.0</u></b>	
Input leakage current (source / sink) $\pm I_i$	$V_i = V_{CC}$ or GND, $V_{DD} = 3.3V$		$\pm 1$	<b><u><math>\pm 35</math></u></b>	nA
	$V_i = V_{CC}$ or GND, $V_{DD} = 5V$		$\pm 2$	<b><u><math>\pm 37</math></u></b>	

## AC Electrical Characteristics

Unless otherwise stated: VDD=5V,  $T_i=25^\circ\text{C}$ . **Bold underlined** figures indicate values valid over the whole temperature range ( $-55^\circ\text{C} < T_i < +225^\circ\text{C}$ ).

Parameter	Condition	Temperature	Min	Typ	Max	Units
Propagation delay time from A or B to Y <sup>1</sup> $t_{PHL}$	$C_L=50\text{pF}$	$T_j=-55^\circ\text{C}$		9	16	ns
		$T_j=25^\circ\text{C}$		10	18	
		$T_j=225^\circ\text{C}$		14	<b><u>25</u></b>	
Propagation delay time from A or B to Y $t_{PLH}$	$C_L=50\text{pF}$	$T_j=-55^\circ\text{C}$		9	16	ns
		$T_j=25^\circ\text{C}$		10	18	
		$T_j=225^\circ\text{C}$		13	<b><u>23</u></b>	
Output transition time High to Low $t_{THL}$	$C_L=50\text{pF}$	$T_j=-55^\circ\text{C}$		13	17	ns
		$T_j=25^\circ\text{C}$		14	18	
		$T_j=225^\circ\text{C}$		17	<b><u>22</u></b>	
Output transition time Low to High $t_{TLH}$	$C_L=50\text{pF}$	$T_j=-55^\circ\text{C}$		19	25	ns
		$T_j=25^\circ\text{C}$		20	26	
		$T_j=225^\circ\text{C}$		23	<b><u>30</u></b>	

<sup>1</sup> Input A is 1% to 2% faster than input B.

### AC Electrical Characteristics (cntd)

Unless otherwise stated:  $V_{DD}=3.3V$ ,  $T_j=25^\circ C$ . **Bold underlined** figures indicate values valid over the whole temperature range ( $-55^\circ C < T_j < +225^\circ C$ ).

Parameter	Condition	Temperature	Min	Typ	Max	Units
Propagation delay time from A or B to Y $t_{PHL}$	$C_L=50pF$	$T_j=-55^\circ C$		16	28	ns
		$T_j=25^\circ C$		19	33	
		$T_j=225^\circ C$		23	<b><u>40</u></b>	
Propagation delay time from A or B to Y $t_{PLH}$	$C_L=50pF$	$T_j=-55^\circ C$		17	30	ns
		$T_j=25^\circ C$		19	33	
		$T_j=225^\circ C$		23	<b><u>40</u></b>	
Output transition time High to Low $t_{THL}$	$C_L=50pF$	$T_j=-55^\circ C$		20	26	ns
		$T_j=25^\circ C$		21	28	
		$T_j=225^\circ C$		27	<b><u>36</u></b>	
Output transition time High to Low $t_{TLH}$	$C_L=50pF$	$T_j=-55^\circ C$		23	30	ns
		$T_j=25^\circ C$		24	32	
		$T_j=225^\circ C$		26	<b><u>34</u></b>	

### AC Waveforms

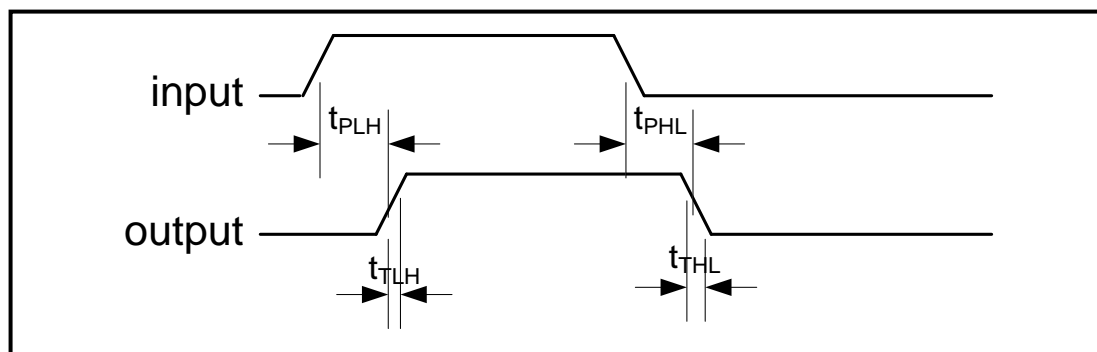
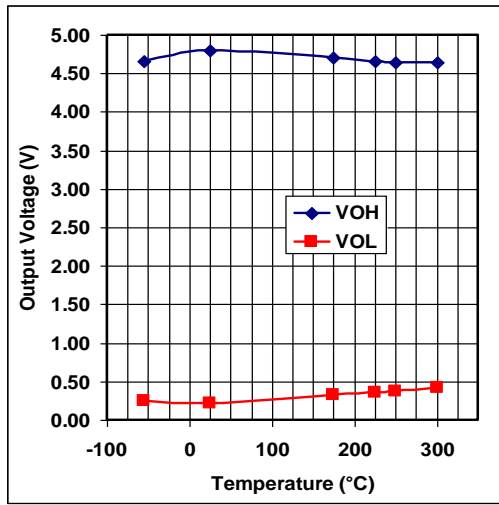
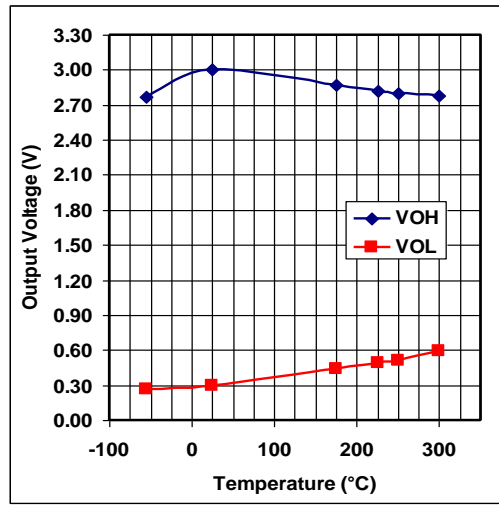


Figure 2. AC Waveforms

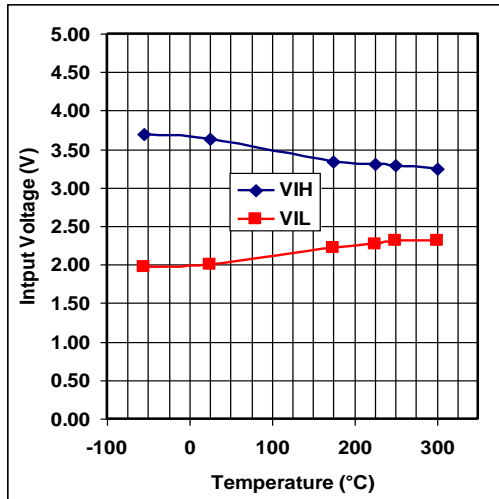
Typical Performance Characteristics



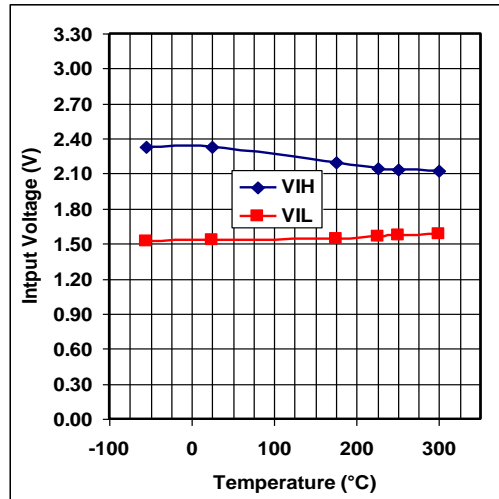
Output voltage levels versus temperature,  $V_{DD} = 5V$



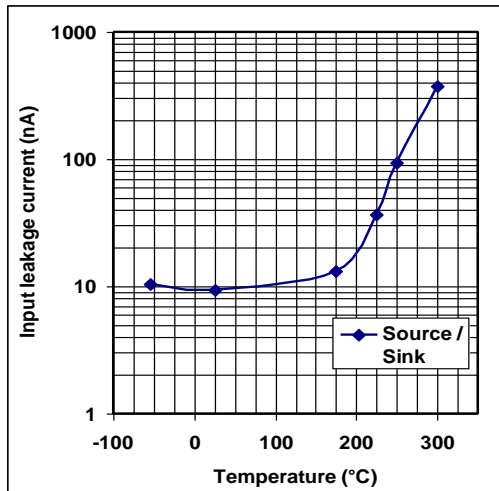
Output voltage levels versus temperature,  $V_{DD} = 3.3V$



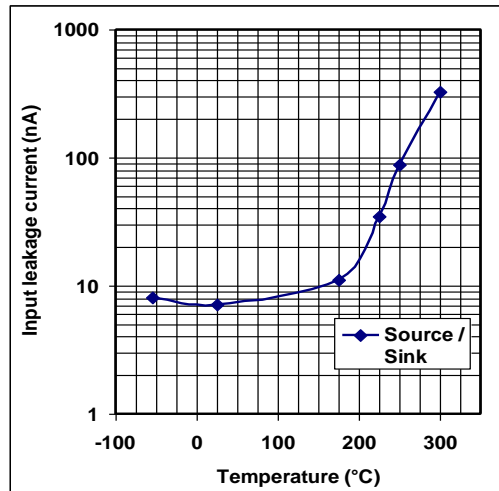
Input voltage levels versus temperature,  $V_{DD} = 5V$



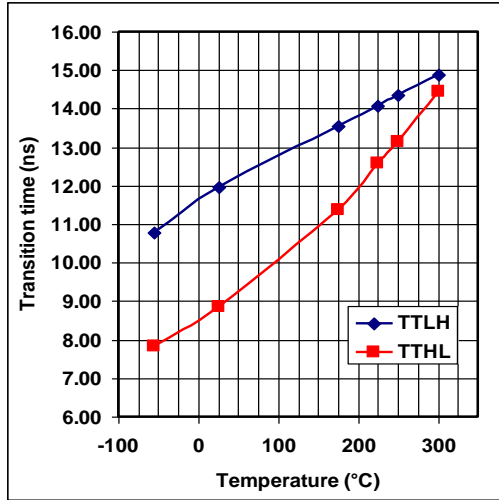
Input voltage levels versus temperature,  $V_{DD} = 3.3V$



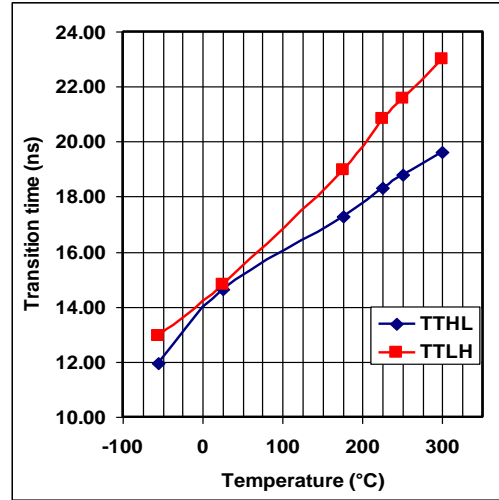
Input leakage current versus temperature,  $V_{DD} = 5V$



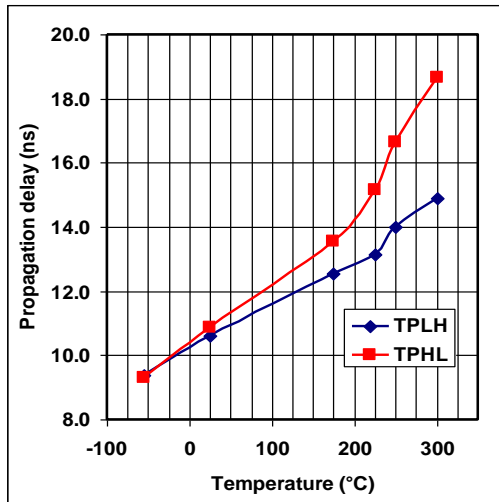
Input leakage current versus temperature,  $V_{DD} = 3.3V$



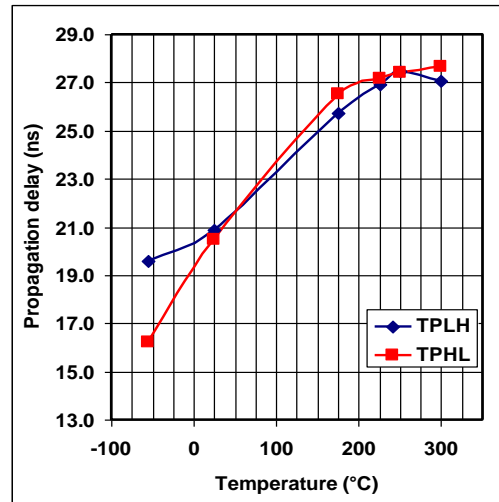
Transition times versus temperature,  
 $V_{DD} = 5V$



Transition times versus temperature,  
 $V_{DD} = 3.3V$



Propagation delays versus temperature,  
 $V_{DD} = 5V$

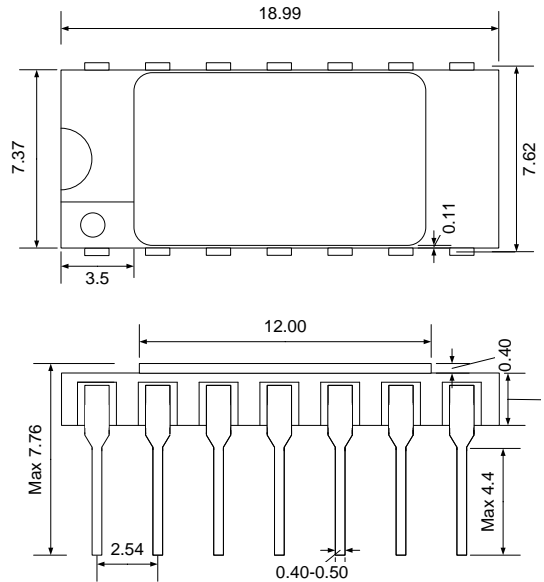


Propagation delays versus temperature,  
 $V_{DD} = 3.3V$

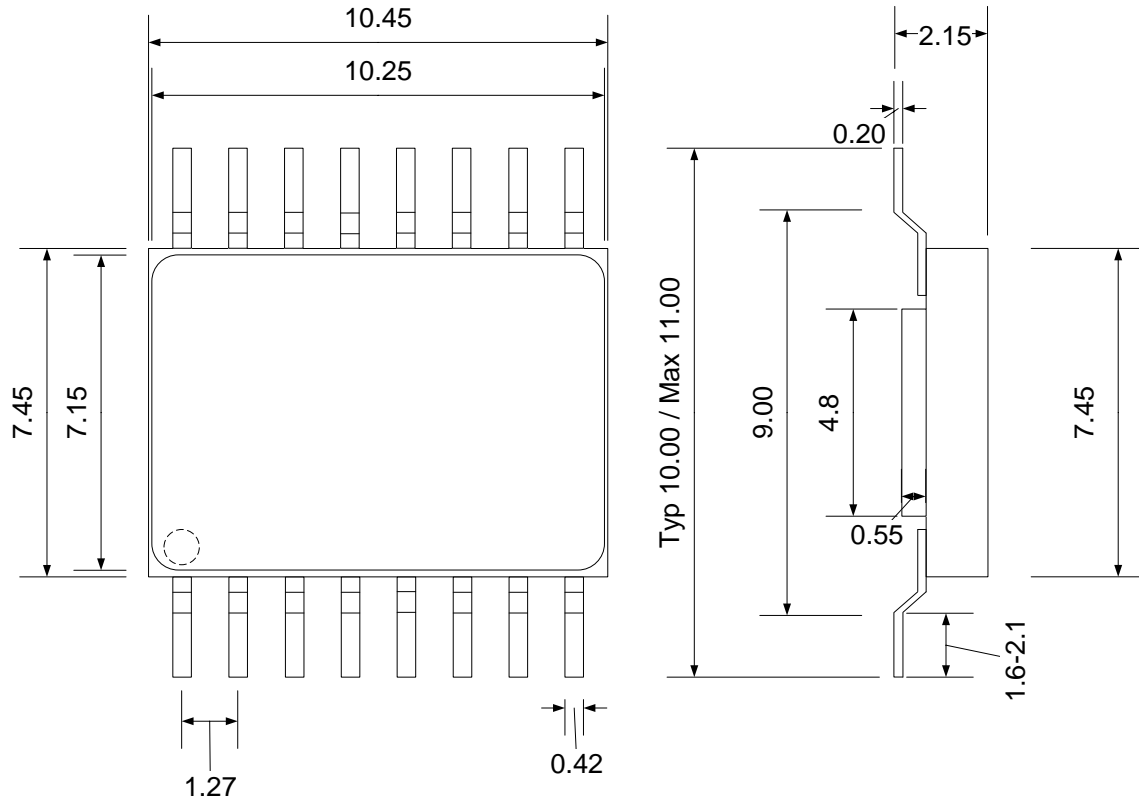
**Ordering Information**

Ordering Reference	Package	Temperature Range	Marking
CHT-7408-CDIL14-T	Ceramic DIL14	-55°C to +225°C	CHT-7408
CHT-7408-CSOIC16-T	Ceramic SOIC16	-55°C to +225°C	CHT-7408

**Package Dimensions**



Drawing CDIL14 (mm +/- 10%)



Drawing CSOIC16 (mm +/- 10%)



## Contact & Ordering

CISSOID S.A.

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