

CHT-NMOS8001-PRELIMINARY DATASHEET

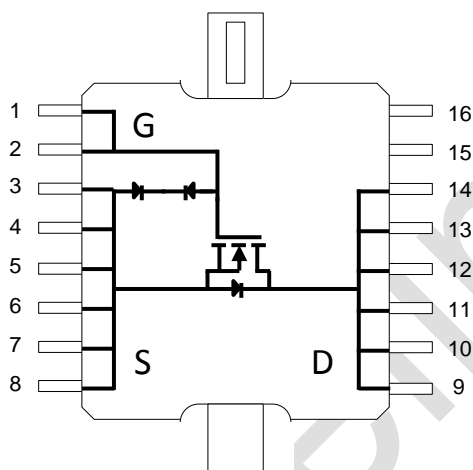
Version: 1.0

High-Temperature, 80V / 1A N-Channel MOSFET

General description

The CHT-NMOS8001 is a Medium Power 80V/1A N-channel power MOSFET's designed to achieve high performance in an extremely wide temperature range: typical operation temperature goes from -55°C to 225°C.

The CHT-NMOS8001 is available in a tiny TDFP16 hermetically-sealed Ceramic SMD package.

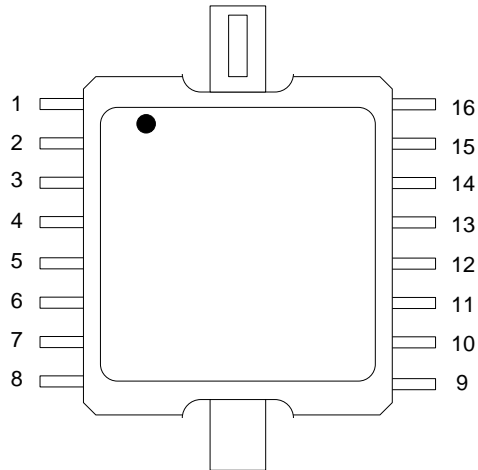


Features

- Specified from -55 to +225°C (Tj)
- Drain voltage up to 80V
- Max DC drain current: 1A
- Maximum pulsed drain current:
 - 3A @ 225°C
 - 5.2A @ 25°C
- R_{DSon} (typical):
 - 1.56Ω @ 225°C
 - 0.76 Ω @ 25°C
- $V_{GS} = -5.5V$ to +5.5V
- Anti-series ESD diodes between gate and source allow negative V_{GS} voltage
- Available in tiny TDFP16 (5x5.5mm) hermetically-sealed ceramic SMD package

Applications

- Well logging
- Oil & Gas
- Aeronautics & aerospace
- Automotive

Package type (TDFP16) & Pinout


Pin #	Pin Name	Pin Description
1	G	MOSFET gate
2		
3	S	MOSFET source
4		
5		
6		
7		
8		
9	D	MOSFET drain
10		
11		
12		
13		
14		
15	NC	NC
16	NC	NC

The 2 vertical large leads are internally connected to S and are also connected to the package heat sink. Those 2 vertical pins **MUST** be connected at PCB level to S

Preliminary

Absolute Maximum Ratings

Gate-to-Source voltage V_{GS}	-5.5V to 5.5V
Drain-to-Source voltage V_{DS}	0V to 80V
Power dissipation $T_a=25^\circ\text{C}$	2.5W
Derating Factor	0.015W/ $^\circ\text{C}$

ESD Rating

Human Body Model	CLASS 2 (>2KV)
------------------	----------------

Operating Conditions

Gate-to-Source voltage V_{GS}	-5V to 5V
Drain-to-Source voltage V_{DS}	0V to 80V
Drain DC current I_{DS}	0A to 1A
Junction temperature	-55 $^\circ\text{C}$ to +225 $^\circ\text{C}$

Maximum DC current depends as well on thermal characteristics (Θ_{JA} , T_a)

Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Frequent or extended exposure to absolute maximum rating conditions or above may affect device reliability.

Preliminary

Electrical characteristics

DC Characteristics

Unless otherwise stated, $T_j = 25^\circ\text{C}$. **Bold** figures point out values valid over the whole temperature range ($T_j = -55^\circ\text{C}$ to $+225^\circ\text{C}$).

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Threshold voltage	V_{TH}	$V_{TH} = V_{DS} @ I_D = 1 \text{ mA}$	0.85	1.6	1.95	V
Drain cut-off current	I_{DSS}	$V_{GS} = 0\text{V}, V_{DS} = 80\text{V}, T_j = 25^\circ\text{C}$		5		nA
		$V_{GS} = 0\text{V}, V_{DS} = 80\text{V}, T_j = 225^\circ\text{C}$		11		uA
Gate leakage current ¹	I_{GSS}	$V_{GS} = 5\text{V}, V_{DS} = 50\text{mV}, T_j = 25^\circ\text{C}$		1		nA
		$V_{GS} = 5\text{V}, V_{DS} = 50\text{mV}, T_j = 225^\circ\text{C}$		120		nA
Static drain-to-source resistance	$R_{DS(on)}$	$V_{GS} = 5\text{V}, T_j = -55^\circ\text{C}$		0.57		Ω
		$V_{GS} = 5\text{V}, T_j = 25^\circ\text{C}$		0.76		Ω
		$V_{GS} = 5\text{V}, T_j = 225^\circ\text{C}$		1.56		Ω
Breakdown drain-to-source voltage ²	V_{BRDS}	$V_{GS} = 0\text{V}$	80			V

Dynamic Characteristics

Unless otherwise stated, $T_j = 25^\circ\text{C}$. **Bold** figures point out values valid over the whole temperature range ($T_j = -55^\circ\text{C}$ to $+225^\circ\text{C}$).

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Input capacitance	C_{ISS}	$V_{GS} = 0\text{V}_{DC}, V_{DS} = 80\text{V}_{DC}$ $f = 1\text{MHz}$		232		pF
Output capacitance	C_{OSS}	$V_{GS} = 0\text{V}_{DC}, V_{DS} = 80\text{V}_{DC}$ $f = 1\text{MHz}$		38		pF
Feedback capacitance	C_{RSS}	$V_{GS} = 0\text{V}_{DC}, V_{DS} = 80\text{V}_{DC}$ $f = 1\text{MHz}$		9.8		pF

Switching Characteristics

Unless otherwise stated, $T_j = 25^\circ\text{C}$. **Bold** figures point out values valid over the whole temperature range ($T_j = -55^\circ\text{C}$ to $+225^\circ\text{C}$) (cfr Figure 13: Switching energy losses/timings measurement setup)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Turn-off delay time	$T_{d(OFF)}$	$V_{DS} = 40\text{V}, I_D = 1\text{A}$ $V_{GS} = 5\text{V}, R_G = 10\Omega$ 25°C		9.1		ns
Rise time	T_r			7.1		ns
Turn-on delay time	$T_{d(ON)}$			4.5		ns
Fall time	T_f			9.5		ns
Maximum drain current	I_D	$V_{DS} = 80\text{V}, V_{GS} = 5\text{V}$ 2 μs pulse, -55°C		7		A
		$V_{DS} = 80\text{V}, V_{GS} = 5\text{V}$ 2 μs pulse, 25°C		5.2		A
		$V_{DS} = 80\text{V}, V_{GS} = 5\text{V}$ 2 μs pulse, 225°C		3		A
Turn-On energy	E_{on}	$V_{DS} = 40\text{V}, I_D = 1\text{A}$		350		nJ
Turn-Off energy	E_{off}	$V_{GS} = 5\text{V}, R_G = 10\Omega$		63		nJ
Total switching energy	E_{tot}	25°C		413		nJ

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Forward voltage	V_F	$I_F = 1\text{mA}, T_j = 25^\circ\text{C}$		0.6		V
Forward current	I_F				1.2	A

Thermal Characteristics

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Thermal resistance (junction-to-case, TDFP16)	Θ_{JC}			11		$^\circ\text{C/W}$
Thermal resistance (junction-to-air, TDFP16)	Θ_{JA}	PCB pad area: 0.42 cm^2		82		$^\circ\text{C/W}$
		PCB pad area: 2.94 cm^2		71		
		PCB pad area: 5.46 cm^2		68		

¹ Includes ESD diode leakage current.

² Voltage for which the cut-off current evolution versus V_{DS} becomes exponential.

Typical Performance Characteristics

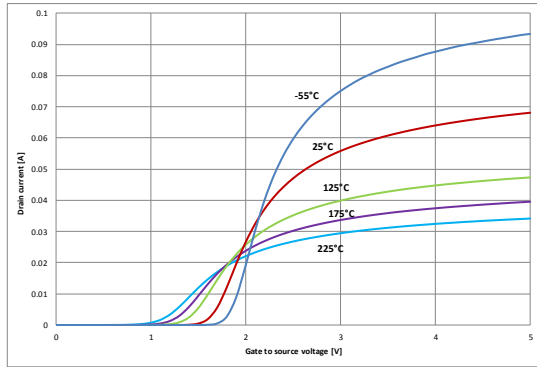


Figure 1: Drain current vs. gate voltage (VDS = 50mV).

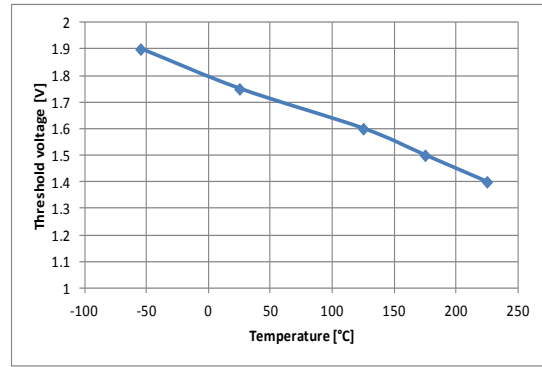


Figure 2: Threshold voltage vs. junction temperature.

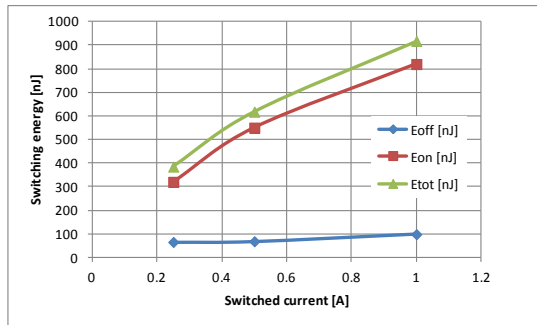


Figure 3: Switching energy losses (VDS= 60V, Tj=25°C)

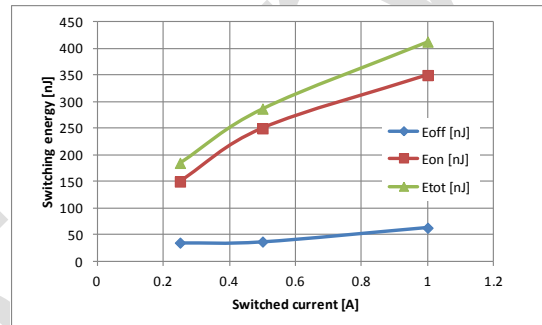


Figure 4: Switching energy losses (VDS= 40V, Tj=25°C)

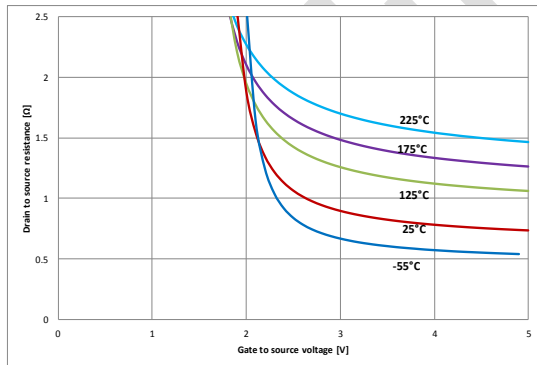


Figure 5: Drain-source resistance vs. gate voltage (VDS=50mV)

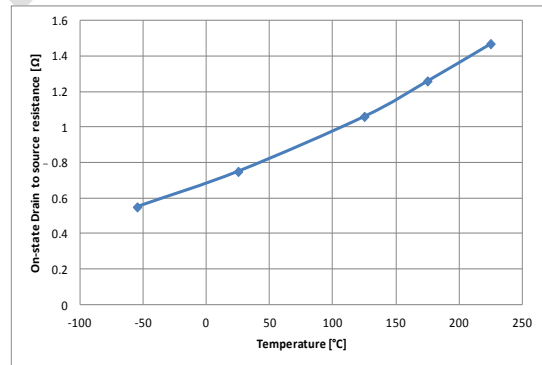
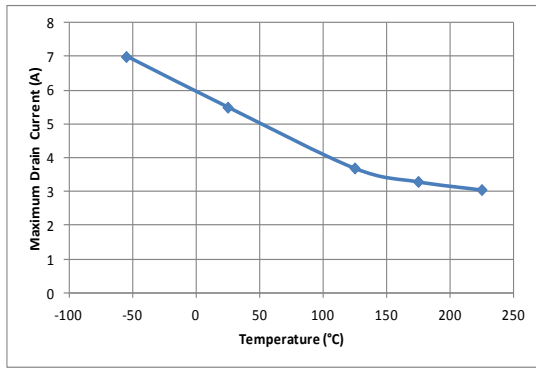
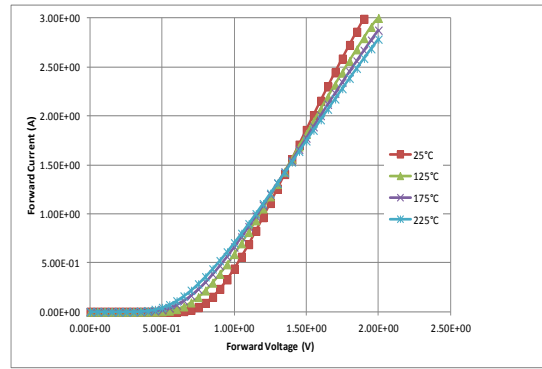
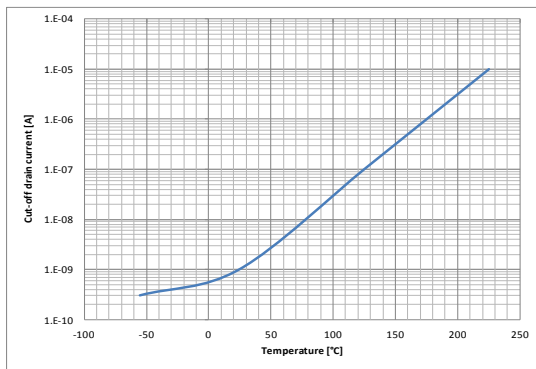
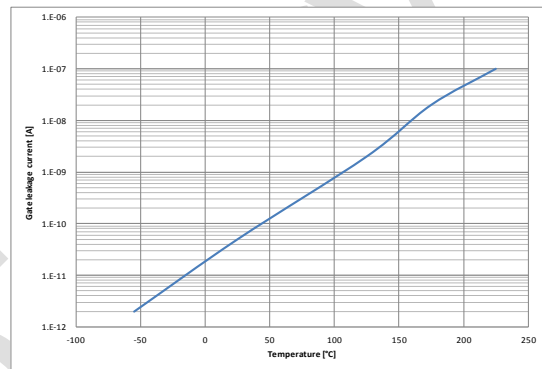
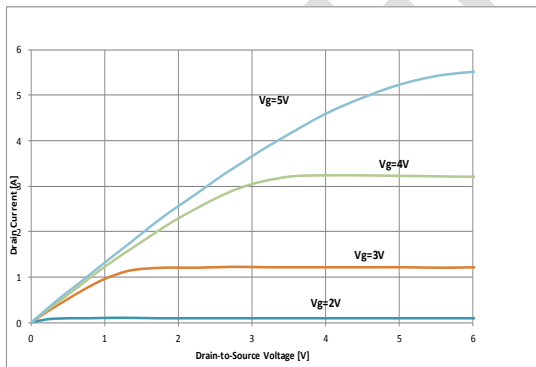
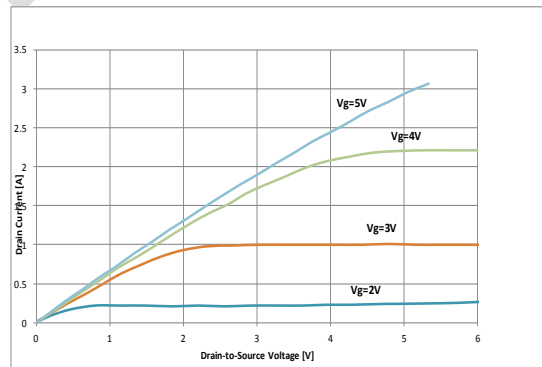


Figure 6: On-state drain source resistance vs. junction temperature (VGS=5V, VDS=50mV).


Figure 7: Maximum pulsed drain current vs. temperature (VGS=5V).

Figure 8: Body diode forward current vs. forward voltage and temperature

Figure 9: Cut-off current vs. junction temperature (VGS=0V, VDS=80V).

Figure 10: Gate and ESD diode leakage current vs. junction temperature (VGS=5V, VDS=50mV).

Figure 11: Pulsed drain current vs drain voltage (Tj=25°C)

Figure 12: Pulsed drain current vs drain voltage (Tj=225°C)

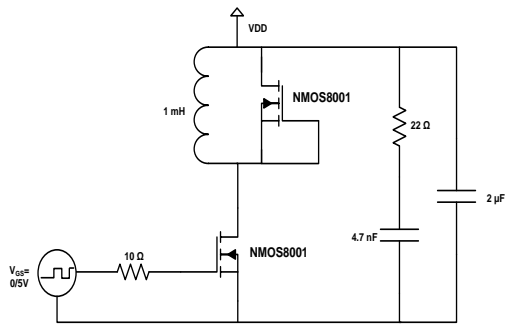


Figure 13: Switching energy losses/timings measurement setup

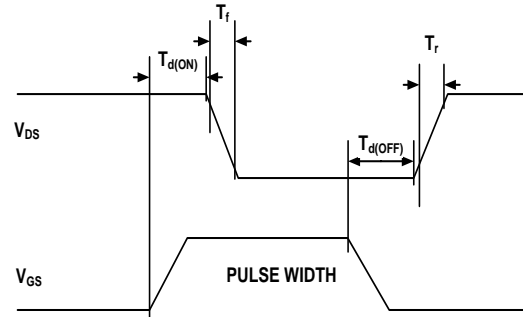


Figure 14: Timing definition diagram

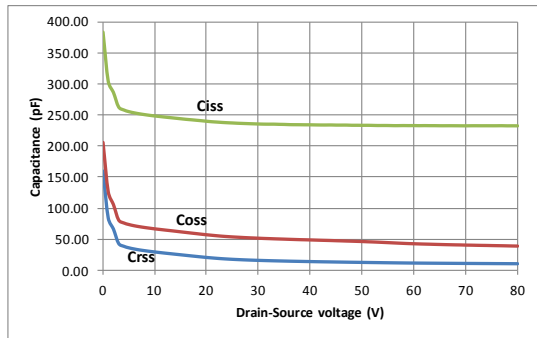
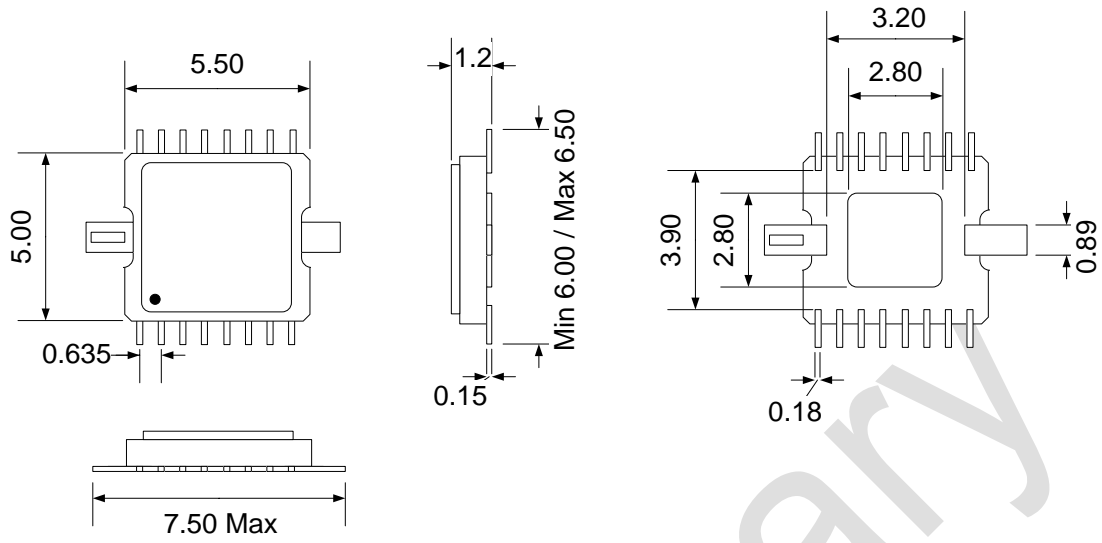


Figure 15: Typical capacitances

Preliminary

Package Dimensions (TDFP16)



Ordering Information

Product Name	Ordering Reference	Package	Marking
CHT-NMOS8001	CHT-PLA4091A-TDFP16-T	TDFP16	CHT-PLA4091A

Contact & Ordering

CISSOID S.A.

Headquarters and contact EMEA:	CISSOID S.A. – Rue Francqui, 3 – 1435 Mont Saint Guibert - Belgium T : +32 10 48 92 10 - F: +32 10 88 98 75 Email: sales@cissoid.com
Sales Representatives:	Visit our website: http://www.cissoid.com

Disclaimer

Neither CISSOID, nor any of its directors, employees or affiliates make any representations or extend any warranties of any kind, either express or implied, including but not limited to warranties of merchantability, fitness for a particular purpose, and the absence of latent or other defects, whether or not discoverable. In no event shall CISSOID, its directors, employees and affiliates be liable for direct, indirect, special, incidental or consequential damages of any kind arising out of the use of its circuits and their documentation, even if they have been advised of the possibility of such a damage. The circuits are provided "as is". CISSOID has no obligation to provide maintenance, support, updates, or modifications.

Preliminary