

## CHT-7474 DATASHEET

*Revision: 03.3  
1-Oct-12  
(Last Modified Date)*

## High-Temperature, Dual D-Flip-Flop

### General Description

The CHT-7474 is a dual positive-edge-triggered D type Flip-flop. Data on the D input is transferred to the output on a rising edge of the clock impulse.

Rn and Sn are asynchronous reset and set. On a low state, they operate on the outputs regardless of the other inputs.

This circuit is designed assuring latchup-free operation for all supply and temperature conditions.

The CHT-7474 can operate with supply voltages from 3.3 to 5V ( $\pm 10\%$ ).

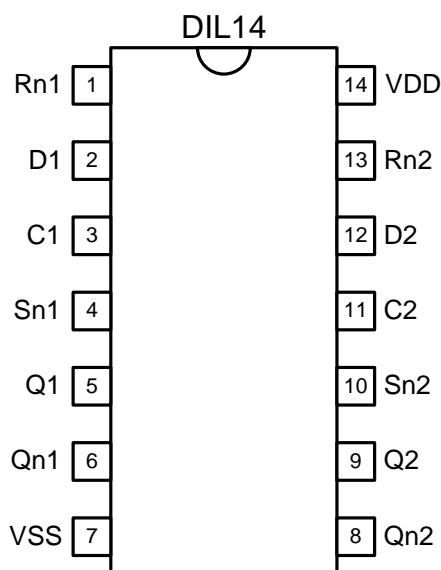
### Features

- Qualified from -55 to +225°C (Tj)
- 3.3 to 5V ( $\pm 10\%$ ) supply voltages
- Latchup-free at any supply and temperature condition
- Validated at 225°C for 30000 hours (CDIL14) and 20000 hours (CSOIC16) (and still on-going)
- Available in DIL14 and CSOIC16 hermetic standard package

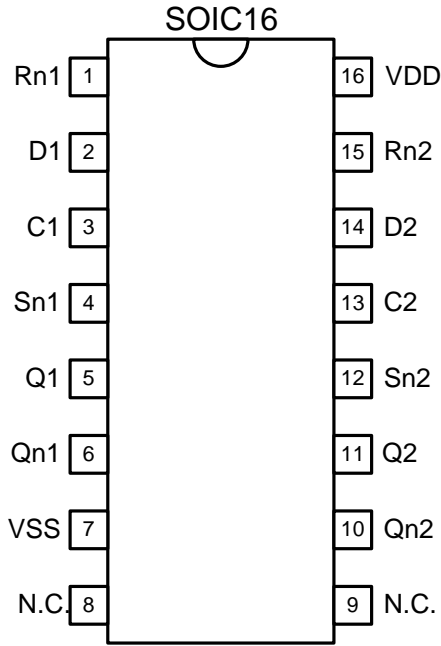
### Applications

- Well logging,
- Automotive, Aeronautics & Aerospace
- Harsh Environments

### Package and Pin Configuration



Pin	Symbol	Description
1	<b>RN1</b>	Reset of D-flip-flop 1
2	<b>D1</b>	Input of D-flip-flop 1
3	<b>C1</b>	Clock pulse of D-flip-flop 1
4	<b>SN1</b>	Set of D-flip-flop 1
5	<b>Q1</b>	Output of D-flip-flop 1
6	<b>QN1</b>	Inverted output of D-flip-flop 1
7	<b>GND</b>	Circuit core ground terminal.
8	<b>QN2</b>	Inverted output of D-flip-flop 2
9	<b>Q2</b>	Output of D-flip-flop 2
10	<b>SN2</b>	Set of D-flip-flop 2
11	<b>C2</b>	Clock pulse of D-flip-flop 2
12	<b>D2</b>	Input of D-flip-flop 2
13	<b>RN2</b>	Reset of D-flip-flop 2
14	<b>VDD</b>	Circuit core power supply terminal.



Pin	Symbol	Description
1	<b>RN1</b>	Reset of D-flip-flop 1
2	<b>D1</b>	Input of D-flip-flop 1
3	<b>C1</b>	Clock pulse of D-flip-flop 1
4	<b>SN1</b>	Set of D-flip-flop 1
5	<b>Q1</b>	Output of D-flip-flop 1
6	<b>QN1</b>	Inverted output of D-flip-flop 1
7	<b>VSS</b>	Circuit core ground terminal.
8	<b>NC</b>	Not connected
9	<b>NC</b>	Not connected
10	<b>QN2</b>	Inverted output of D-flip-flop 2
11	<b>Q2</b>	Output of D-flip-flop 2
12	<b>SN2</b>	Set of D-flip-flop 2
13	<b>C2</b>	Clock pulse of D-flip-flop 2
14	<b>D2</b>	Input of D-flip-flop 2
15	<b>RN2</b>	Reset of D-flip-flop 2
16	<b>VDD</b>	Circuit core power supply terminal.

**Function Table**

INPUT				OUTPUT	
<b>Sn</b>	<b>Rn</b>	<b>C</b>	<b>D</b>	<b>Q</b>	<b>Qn</b>
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	L	X <sup>1</sup>
<b>Sn</b>	<b>Rn</b>	<b>C</b>	<b>D</b>	<b>Q(n+1)</b>	<b>Qn(n+1)</b>
H	H	↑	L	L	H
H	H	↑	H	H	L

<sup>1</sup> Having Sn=Rn=LOW at the same time should be avoided. The only known output is Q.



## Logical Diagram

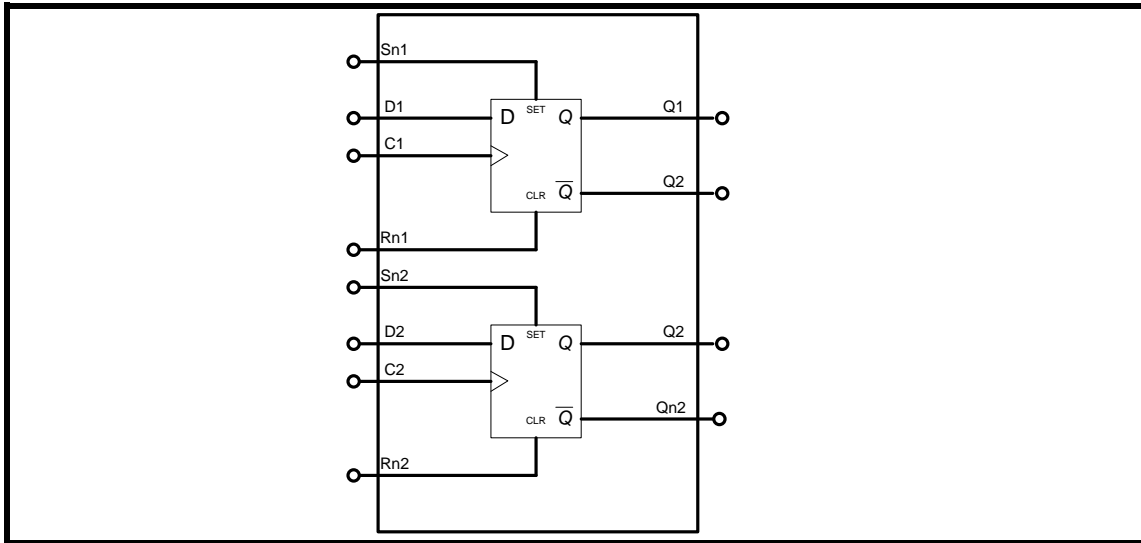


Figure 1. CHT-7474: simplified logical diagram.

**Absolute Maximum Ratings**

 Supply Voltage  $V_{DD}$  to GND -0.5 to 6.0V  
 Voltage on any Pin to GND -0.5 to  $V_{DD}+0.5V$ 
**Operating Conditions**

 Supply Voltage  $V_{DD}$  to GND 3.3V to 5V ( $\pm 10\%$ )  
 Junction temperature -55°C to +225°C

**ESD Rating (expected)**

Human Body Model 1kV

**DC Electrical Characteristics**

 Unless otherwise stated:  $V_{DD}=5V$ ,  $T_j=25^\circ C$ . **Bold underlined** figures indicate values valid over the whole temperature range ( $-55^\circ C < T_j < +225^\circ C$ ).

Parameter	Condition	Min	Typ	Max	Units
Supply voltage $V_{DD}$		2.97		5.5V	V
Quiescent current $I_{DD}$	$V_{DD} = 3.3V$ , $T_j = -55^\circ C$			20	nA
	$V_{DD} = 5V$ , $T_j = -55^\circ C$			20	
	$V_{DD} = 3.3V$ , $T_j = 225^\circ C$			<b><u>2650</u></b>	
	$V_{DD} = 5V$ , $T_j = 225^\circ C$			<b><u>3030</u></b>	
Minimum HIGH level output voltage $V_{OH}$	$V_{DD} = 3.3V$ , $I_{OH} < 4mA$ (source)	<b><u>2.7</u></b>	3.04		V
	$V_{DD} = 5V$ , $I_{OH} < 4mA$ (source)	<b><u>4.6</u></b>	4.82		
Maximum LOW level output voltage $V_{OL}$	$V_{DD} = 3.3V$ , $I_{OL} < 4mA$ (sink)		0.28	<b><u>0.5</u></b>	V
	$V_{DD} = 5V$ , $I_{OL} < 4mA$ (sink)		0.20	<b><u>0.4</u></b>	
Minimum HIGH level input voltage $V_{IH}$	$V_{DD} = 3.3V$	<b><u>2.4</u></b>	2.10		V
	$V_{DD} = 5V$	<b><u>3.7</u></b>	3.49		
Maximum LOW level input voltage $V_{IL}$	$V_{DD} = 3.3V$		1.72	<b><u>1.5</u></b>	V
	$V_{DD} = 5V$		2.16	<b><u>2.0</u></b>	
Input leakage current (source / sink) $\pm I_I$	$V_I = V_{CC}$ or GND, $V_{DD} = 3.3V$		$\pm 1$	<b><u><math>\pm 35</math></u></b>	nA
	$V_I = V_{CC}$ or GND, $V_{DD} = 5V$		$\pm 2$	<b><u><math>\pm 37</math></u></b>	

**AC Electrical Characteristics**

Unless otherwise stated: VDD=5V, T<sub>i</sub>=25°C. **Bold underlined** figures indicate values valid over the whole temperature range (-55°C < T<sub>i</sub> < +225°C).

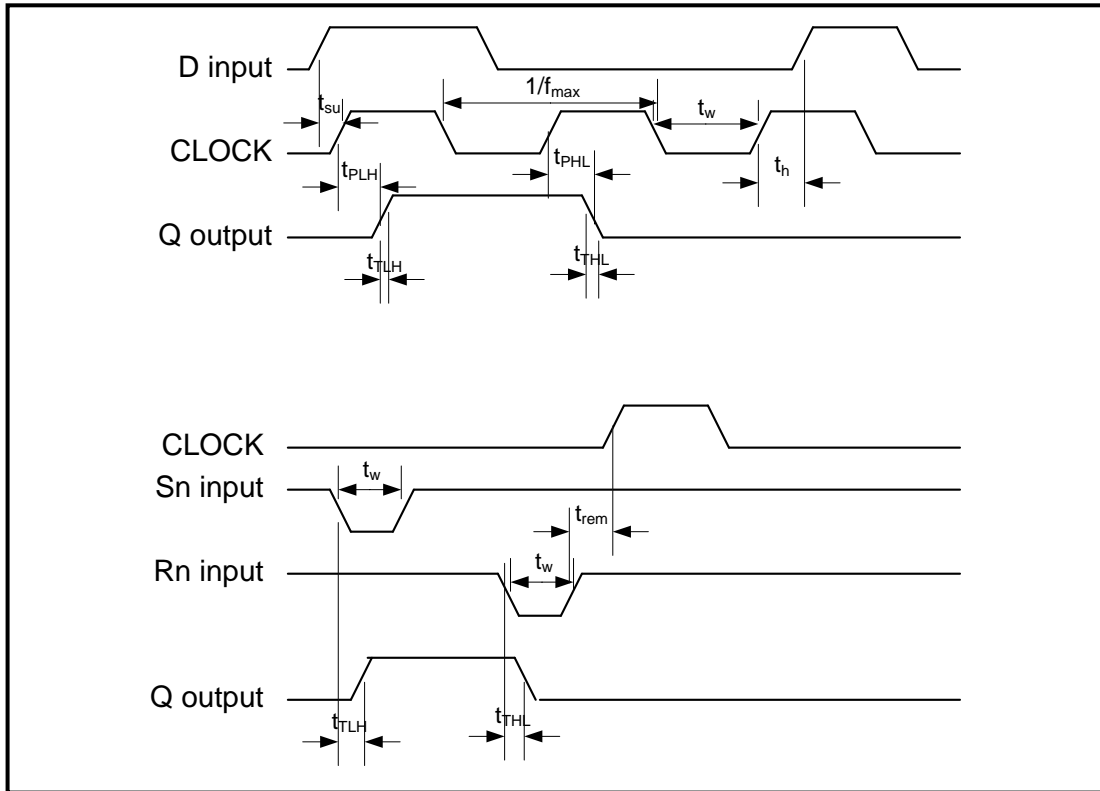
Parameter	Condition	Temperature	Min	Typ	Max	Units
Propagation delay from C to Q, Qn t <sub>PHL</sub>	C <sub>L</sub> =50pF	T <sub>j</sub> =-55°C		12	21	ns
		T <sub>j</sub> =25°C		14	25	
		T <sub>j</sub> =225°C		19	33	
Propagation delay from Rn to Q, Qn t <sub>PHL</sub>	C <sub>L</sub> =50pF	T <sub>j</sub> =-55°C		11	20	ns
		T <sub>j</sub> =25°C		12	21	
		T <sub>j</sub> =225°C		17	30	
Propagation delay from C to Q, Qn t <sub>PLH</sub>	C <sub>L</sub> =50pF	T <sub>j</sub> =-55°C		9	16	ns
		T <sub>j</sub> =25°C		10	18	
		T <sub>j</sub> =225°C		15	27	
Propagation delay from Sn to Q, Qn t <sub>PLH</sub>	C <sub>L</sub> =50pF	T <sub>j</sub> =-55°C		11	20	ns
		T <sub>j</sub> =25°C		12	21	
		T <sub>j</sub> =225°C		18	32	
Output transition time High to Low t <sub>THL</sub>	C <sub>L</sub> =50pF	T <sub>j</sub> =-55°C		13	17	ns
		T <sub>j</sub> =25°C		14	18	
		T <sub>j</sub> =225°C		17	<b><u>22</u></b>	
Output transition time High to Low t <sub>TLH</sub>	C <sub>L</sub> =50pF	T <sub>j</sub> =-55°C		19	25	ns
		T <sub>j</sub> =25°C		20	26	
		T <sub>j</sub> =225°C		23	<b><u>30</u></b>	
Clock pulse width t <sub>w</sub>	C <sub>L</sub> =50pF	T <sub>j</sub> =-55°C	4	2		ns
		T <sub>j</sub> =25°C	4	2		
		T <sub>j</sub> =225°C	<b><u>6</u></b>	3		
Set or reset pulse width t <sub>w</sub>	C <sub>L</sub> =50pF	T <sub>j</sub> =-55°C	4	2		ns
		T <sub>j</sub> =25°C	4	2		
		T <sub>j</sub> =225°C	<b><u>6</u></b>	3		
Removal time set or reset t <sub>rem</sub>	C <sub>L</sub> =50pF	T <sub>j</sub> =-55°C	4	2		ns
		T <sub>j</sub> =25°C	4	2		
		T <sub>j</sub> =225°C	<b><u>6</u></b>	3		
Set-up time D to C t <sub>su</sub>	C <sub>L</sub> =50pF	T <sub>j</sub> =-55°C	2	1		ns
		T <sub>j</sub> =25°C	2	1		
		T <sub>j</sub> =225°C	<b><u>2</u></b>	1		
Hold time C to D t <sub>h</sub>	C <sub>L</sub> =50pF	T <sub>j</sub> =-55°C	<b><u>2</u></b>	1		ns
		T <sub>j</sub> =25°C	2	1		
		T <sub>j</sub> =225°C	2	1		
Maximum clock pulse frequency f <sub>max</sub>	C <sub>L</sub> =50pF	T <sub>j</sub> =-55°C	31	63		MHz
		T <sub>j</sub> =25°C	27	55		
		T <sub>j</sub> =225°C	21	40		

**AC Electrical Characteristics (cntd)**

Unless otherwise stated: VDD=3.3V,  $T_j=25^\circ\text{C}$ . **Bold underlined** figures indicate values valid over the whole temperature range ( $-55^\circ\text{C} < T_j < +225^\circ\text{C}$ ).

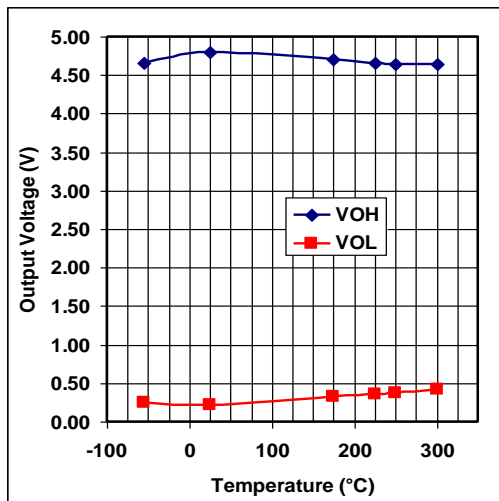
Parameter	Condition	Temperature	Min	Typ	Max	Units
Propagation delay from C to Q, Qn $t_{PHL}$	$C_L=50\text{pF}$	$T_j=-55^\circ\text{C}$		23	40	ns
		$T_j=25^\circ\text{C}$		26	45	
		$T_j=225^\circ\text{C}$		35	61	
Propagation delay from Rn to Q, Qn $t_{PHL}$	$C_L=50\text{pF}$	$T_j=-55^\circ\text{C}$		21	37	ns
		$T_j=25^\circ\text{C}$		23	40	
		$T_j=225^\circ\text{C}$		31	54	
Propagation delay from C to Q, Qn $t_{PLH}$	$C_L=50\text{pF}$	$T_j=-55^\circ\text{C}$		17	30	ns
		$T_j=25^\circ\text{C}$		20	35	
		$T_j=225^\circ\text{C}$		26	45	
Propagation delay from Sn to Q, Qn $t_{PLH}$	$C_L=50\text{pF}$	$T_j=-55^\circ\text{C}$		21	37	ns
		$T_j=25^\circ\text{C}$		24	42	
		$T_j=225^\circ\text{C}$		32	55	
Output transition time High to Low $t_{THL}$	$C_L=50\text{pF}$	$T_j=-55^\circ\text{C}$		20	26	ns
		$T_j=25^\circ\text{C}$		21	28	
		$T_j=225^\circ\text{C}$		27	<b><u>36</u></b>	
Output transition time Low to High $t_{TLH}$	$C_L=50\text{pF}$	$T_j=-55^\circ\text{C}$		23	30	ns
		$T_j=25^\circ\text{C}$		24	32	
		$T_j=225^\circ\text{C}$		26	<b><u>34</u></b>	
Clock pulse width $t_w$	$C_L=50\text{pF}$	$T_j=-55^\circ\text{C}$	6	3		ns
		$T_j=25^\circ\text{C}$	8	4		
		$T_j=225^\circ\text{C}$	<b><u>10</u></b>	5		
Set or reset pulse width $t_w$	$C_L=50\text{pF}$	$T_j=-55^\circ\text{C}$	6	3		ns
		$T_j=25^\circ\text{C}$	8	4		
		$T_j=225^\circ\text{C}$	<b><u>10</u></b>	5		
Removal time set or reset $t_{rem}$	$C_L=50\text{pF}$	$T_j=-55^\circ\text{C}$	6	3		ns
		$T_j=25^\circ\text{C}$	6	3		
		$T_j=225^\circ\text{C}$	<b><u>8</u></b>	4		
Set-up time D to C $t_{su}$	$C_L=50\text{pF}$	$T_j=-55^\circ\text{C}$	4	2		ns
		$T_j=25^\circ\text{C}$	4	2		
		$T_j=225^\circ\text{C}$	<b><u>4</u></b>	2		
Hold time C to D $t_h$	$C_L=50\text{pF}$	$T_j=-55^\circ\text{C}$	<b><u>2</u></b>	-1		ns
		$T_j=25^\circ\text{C}$	2	-1		
		$T_j=225^\circ\text{C}$	2	-2		
Maximum clock pulse frequency $f_{max}$	$C_L=50\text{pF}$	$T_j=-55^\circ\text{C}$	18	35		MHz
		$T_j=25^\circ\text{C}$	16	31		
		$T_j=225^\circ\text{C}$	<b><u>12</u></b>	24		

**AC Waveforms**

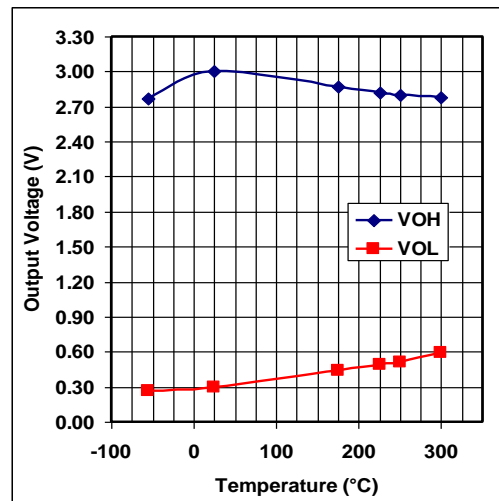


**Figure 2. AC Waveforms**

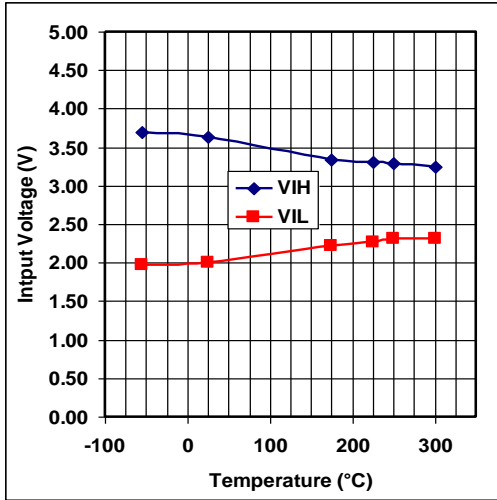
**Typical Performance Characteristics**



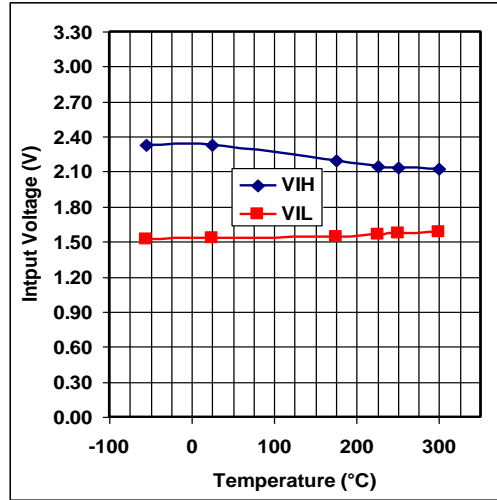
Output voltage levels versus temperature, V<sub>DD</sub> = 5V



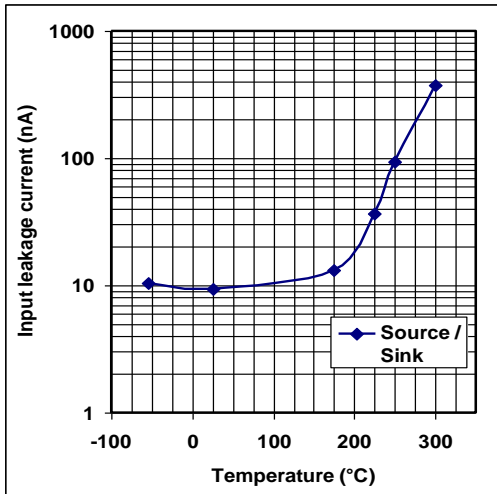
Output voltage levels versus temperature, V<sub>DD</sub> = 3.3V



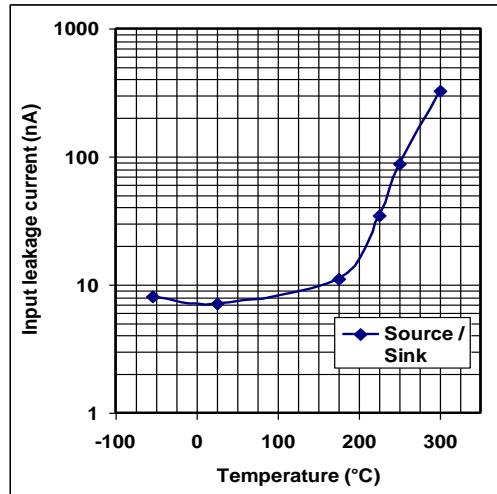
Input voltage levels versus temperature,  $V_{DD} = 5V$



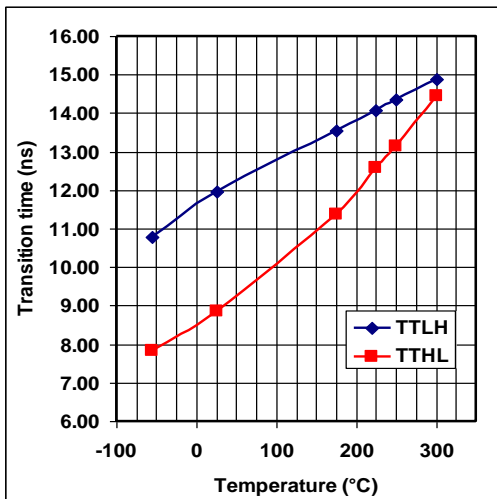
Input voltage levels versus temperature,  $V_{DD} = 3.3V$



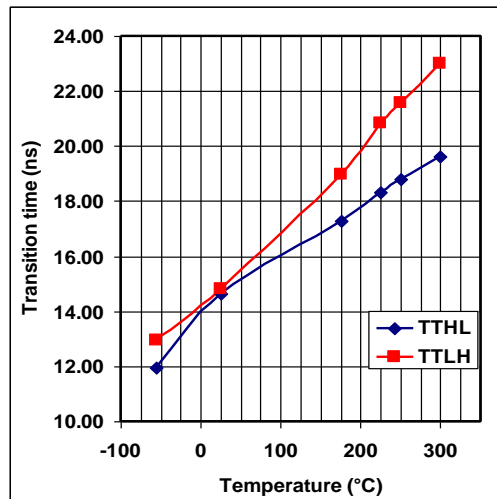
Input leakage current versus temperature,  $V_{DD} = 5V$



Input leakage current versus temperature,  $V_{DD} = 3.3V$

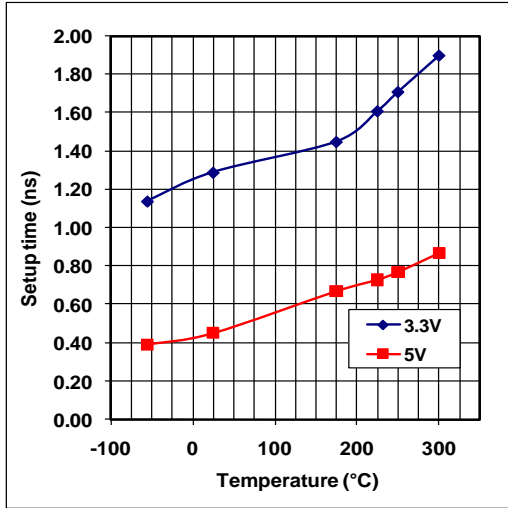


Transition times versus temperature,  $V_{DD} = 5V$

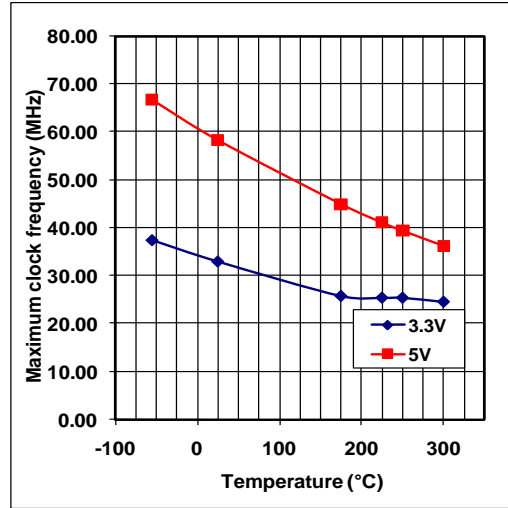


Transition times versus temperature,  $V_{DD} = 3.3V$





Setup time versus temperature,  
 $V_{DD} = 3.3V / 5V$



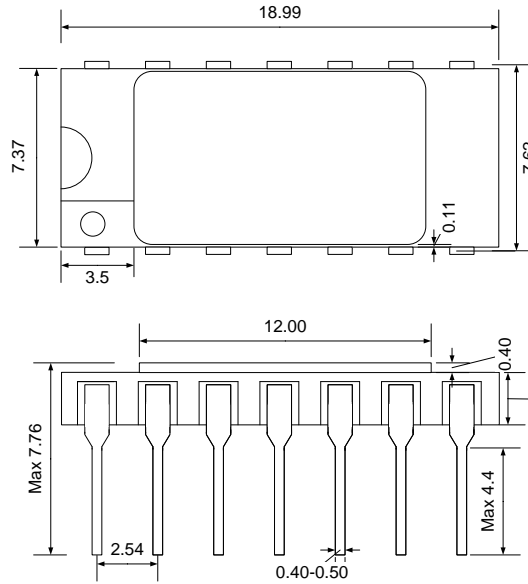
Maximum clock frequency versus  
temperature,  $V_{DD} = 3.3V / 5V$



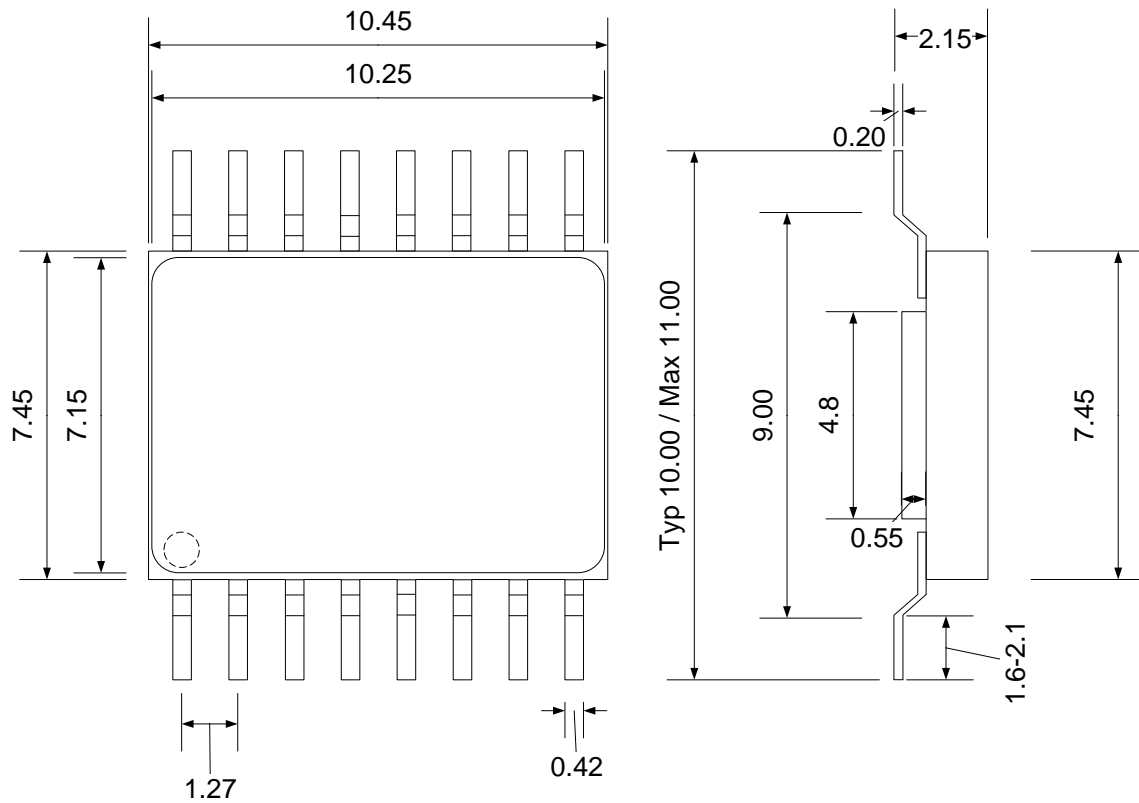
### Ordering Information

Ordering Reference	Package	Temperature Range	Marking
CHT-7474-CDIL14-T	Ceramic DIL14	-55°C to +225°C	CHT-7474
CHT-7474-CSOIC16-T	Ceramic SOIC16	-55°C to +225°C	CHT-7474

### Package Dimensions



Drawing CDIL14 (mm +/- 10%)



Drawing CSOIC16 (mm +/- 10%)



## Contact & Ordering

CISSOID S.A.

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