Features

- **256 x 4 static RAM for control store in high-speed computers**
- **CMOS for optimum speed/power**
- **High speed**
  - **— 15 ns (commercial)**
  - **— 25 ns (military)**
- **Low power**
  - **— 330 mW (commercial)**
  - **— 495 mW (military)**
- **Separate inputs and outputs**
- **5-volt power supply ±10% tolerance, both commercial and military**
- **Capable of withstanding greater than 2001V static discharge**
- **TTL-compatible inputs and outputs**

Functional Description

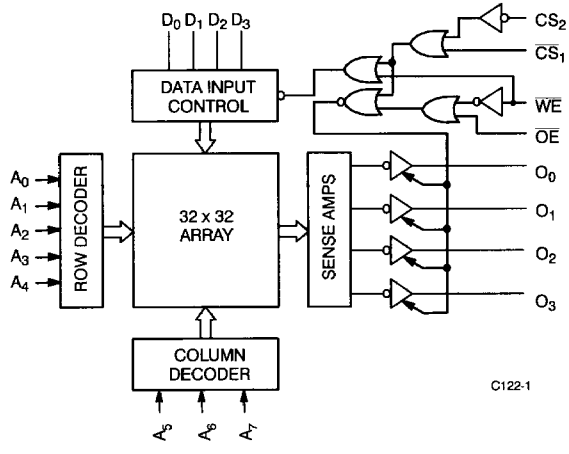
The CY7C122 is a high-performance CMOS static RAM organized as 256 words by 4 bits. Easy memory expansion is provided by an active LOW chip select one ($\overline{CS_1}$) input, an active HIGH chip select two (CS_2) input, and three-state outputs.

An active LOW write enable input ($\overline{WE}$) controls the writing/reading operation of the memory. When the chip select one ($\overline{CS_1}$) and write enable ($\overline{WE}$) inputs are LOW and the chip select two (CS_2) input is HIGH, the information on the four data inputs (D_0 to D_3) is written into the addressed memory word and the output circuitry is preconditioned so that the correct data is present at the outputs when the write cycle is complete. This preconditioning operation insures minimum write recovery times by eliminating the "write recovery glitch".

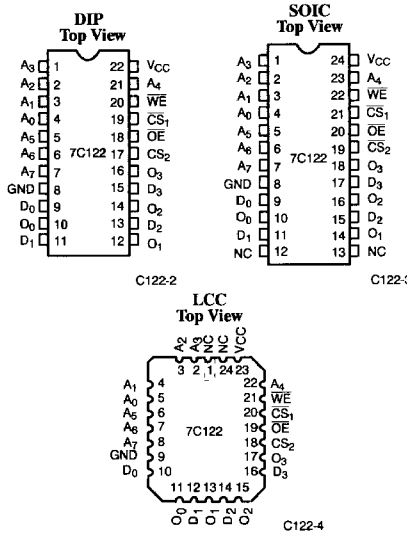
Reading is performed with the chip select one ($\overline{CS_1}$) input is LOW, the chip select two input (CS_2) and write enable ($\overline{WE}$) inputs are HIGH, and the output enable ($\overline{OE}$) input is LOW. The information stored in the addressed word is read out on the four non-inverting outputs (O_0 to O_3).

The outputs of the memory go to an active high-impedance state whenever chip select one ($\overline{CS_1}$) is HIGH, chip select two (CS_2) is LOW, output enable ($\overline{OE}$) is HIGH, or during the writing operation when write enable ($\overline{WE}$) is LOW.

Logic Block Diagram



Pin Configurations



Selection Guide

		7C122–15	7C122–25	7C122–35
Maximum Access Time (ns)	Commercial	15	25	35
	Military		25	35
Maximum Operating Current (mA)	Commercial	90	60	60
	Military		90	90

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... − 65°C to +150°C

Ambient Temperature with Power Applied ..... − 55°C to +125°C

Supply Voltage to Ground Potential (Pin 22 to Pin 8) ..... − 0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... − 0.5V to +7.0V

DC Input Voltage ..... − 3.0V to +7.0V

Output Current into Outputs (Low) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Military[1]	− 55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range[2]

Parameters	Description	Test Conditions		7C122−15 Min.	7C122−15 Max.	7C122−25 7C122−35 Min.	7C122−25 7C122−35 Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = − 5.2 mA		2.4		2.4		V
V_{OL}	Output LOW Current	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4	V
V_{IH}	Input HIGH Level			2.1	V_{CC}	2.1	V_{CC}	V
V_{IL}	Input LOW Level			− 3.0	0.8	− 3.0	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}			10		10	μA
V_{CD}	Input Diode Clamp Voltage				Note 3		Note 3	
I_{OZ}	Output Current (High Z)	V_{OL} ≤ V_{OUT} ≤ V_{OH}, Output Disabled		− 10	+10	− 10	+10	μA
I_{OS}	Output Short Circuit Current[4]	V_{CC} = Max., V_{OUT} = GND	Commercial		− 70		− 70	mA
			Military		− 80		− 80	mA
I_{CC}	Power Supply Current	V_{CC} = Max., I_{OUT} = 0 mA	Commercial		90		60	mA
			Military				90	mA

Capacitance[5]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	8	pF
C_{OUT}	Output Capacitance		8	pF

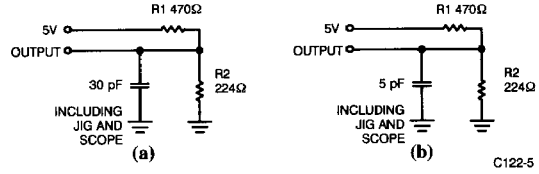
Logic Table[6]

Inputs					Outputs	Mode
$\overline{OE}$	$\overline{CS_1}$	CS_2	$\overline{WE}$	$D_0 - D_3$		
X	H	X	X	X	High Z	Not Selected
X	X	L	X	X	High Z	Not Selected
L	L	H	H	X	$O_0 - O_3$	Read Stored Data
X	L	H	L	L	High Z	Write "0"
X	L	H	L	H	High Z	Write "1"
H	L	H	H	X	High Z	Output Disabled

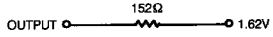
Notes:

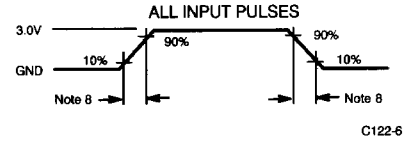
1. T_A is the "instant on" case temperature.
2. See the last page of this specification for Group A subgroup testing information.
3. The CMOS process does not provide a clamp diode. However, the CY7C122 is insensitive to −3V DC input levels and −5V undershoot pulses of less than 10 ns (measured at 50% point).
4. For test purposes, not more than 1 output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.
5. Tested initially and after any design or process changes that may affect these parameters.
6. H = HIGH Voltage, L = LOW Voltage, X = Don't Care, and High Z = High-Impedance

AC Test Loads and Waveforms



Equivalent to: THÉVENIN EQUIVALENT





Switching Characteristics Over the Operating Range[7, 8]

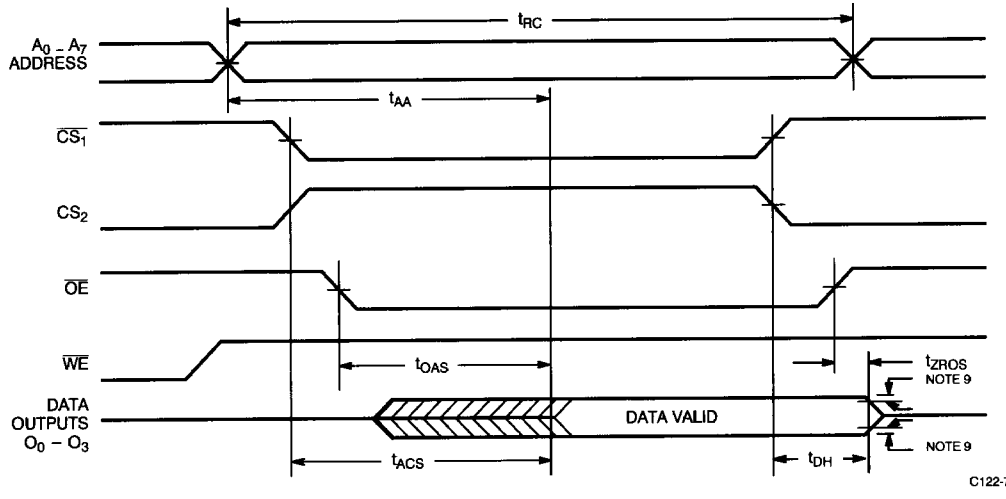
Parameters	Description	7C122–15		7C122–25		7C122–35		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t_{RC}	Read Cycle Time	15		25		35		ns
t_{ACS}	Chip Select Time		8		15		25	ns
t_{ZRCS}	Chip Select to High Z[9]		12		20		30	ns
t_{AOS}	Output Enable Time		8		15		25	ns
t_{ZROS}	Output Enable to High Z[8]		12		20		30	ns
t_{AA}	Address Access Time		15		25		35	ns
WRITE CYCLE								
t_{WC}	Write Cycle Time	15		25		35		ns
t_{ZWS}	Write Disable to High Z[8]		12		20		30	ns
t_{WR}	Write Recovery Time		12		20		25	ns
t_{PWE}	$\overline{WE}$ Pulse Width[6]	11		15		25		ns
t_{WSD}	Data Set-Up Time Prior to Write	0		5		5		ns
t_{WHD}	Data Hold Time After Write	2		5		5		ns
t_{WSA}	Address Set-Up Time[6]	0		5		10		ns
t_{WHA}	Address Hold Time	4		5		5		ns
t_{WSCS}	Chip Select Set-Up Time	0		5		5		ns
t_{WHCS}	Chip Select Hold Time	2		5		5		ns

Notes:

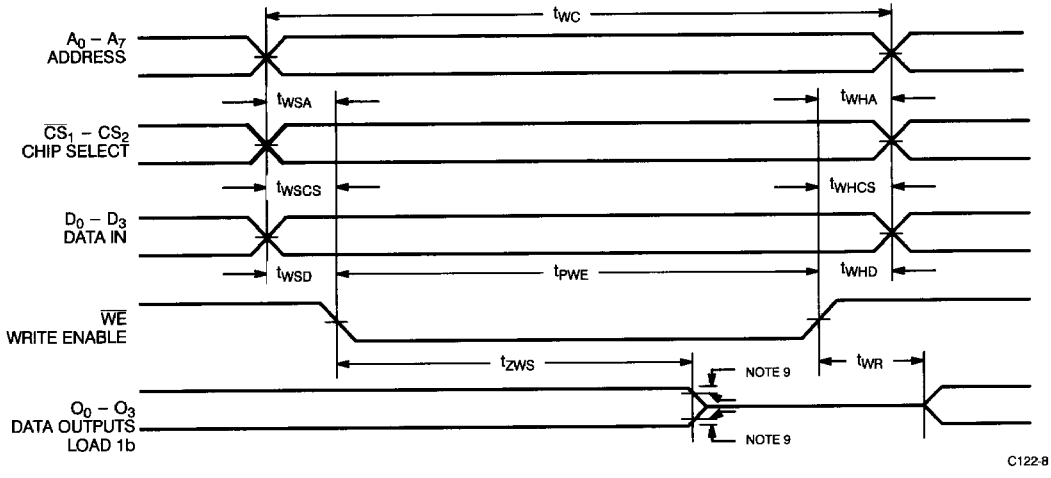
7. t_W measured at t_{WSA} = min.; t_{WSA} measured at t_W = min.
8. Test conditions assume signal transition times of 5 ns or less for the −15 product and 10 ns or less for the −25 and −35 product. Timing reference levels of 1.5V.
9. Transition is measured at steady state HIGH level −500 mV or steady state LOW level +500 mV on the output from 1.5V level on the input with load as shown in part (b) of AC Test Loads.

Switching Waveforms

Read Cycle[10]



Write Cycle[9, 11]

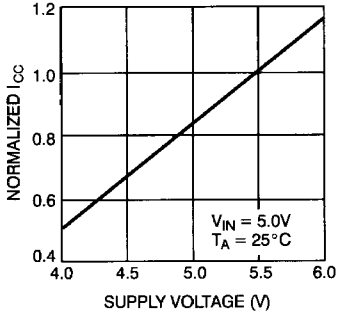


Notes:

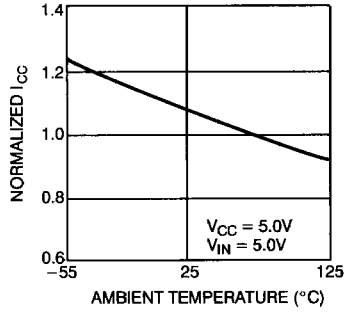
10. Measurements are referenced to 1.5V unless otherwise stated.
11. The timing diagram represents one solution that results in an optimum cycle time. Timing may be changed in varous applications as long as the worst-case limits are not violated.

Typical DC and AC Characteristics

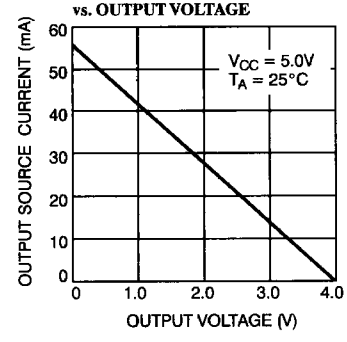
NORMALIZED I_{CC} vs. SUPPLY VOLTAGE



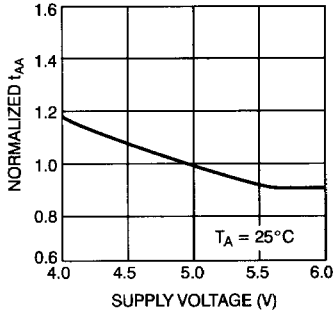
NORMALIZED I_{CC} vs. AMBIENT TEMPERATURE



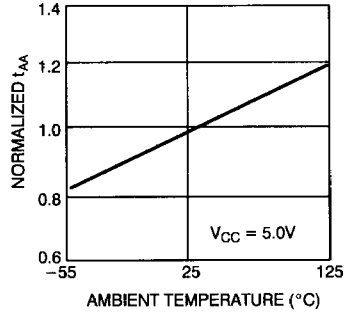
OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



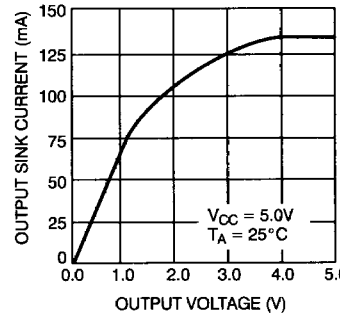
NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE



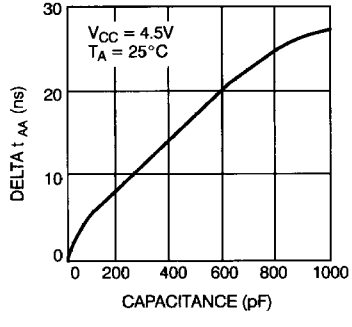
NORMALIZED ACCESS TIME vs. AMBIENT TEMPERATURE



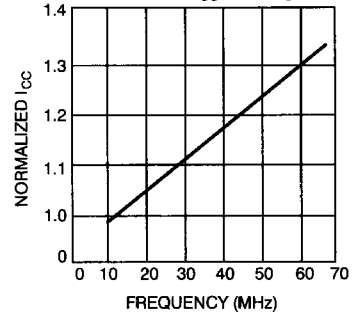
OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



ACCESS TIME CHANGE vs. OUTPUT LOADING



NORMALIZED I_{CC} vs. FREQUENCY



Ordering Information

Speed (ns)	Ordering Code	Package Type	Operating Range
15	CY7C122-15PC	P7	Commercial
	CY7C122-15DC	D8	
	CY7C122-15SC	S13	
25	CY7C122-25PC	P7	Commercial
	CY7C122-25DC	D8	
	CY7C122-25SC	S13	
	CY7C122-25LC	L53	
	CY7C122-25DMB	D8	Military
35	CY7C122-35PC	P7	Commercial
	CY7C122-35SC	S13	
	CY7C122-35DC	D8	
	CY7C122-35LC	L53	
	CY7C122-35DMB	D8	Military
	CY7C122-35LMB	L53	

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameters	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3

Switching Characteristics

Parameters	Subgroups
READ CYCLE	
t_{RC}	7, 8, 9, 10, 11
t_{ACS}	7, 8, 9, 10, 11
t_{OCS}	7, 8, 9, 10, 11
t_{AA}	7, 8, 9, 10, 11
WRITE CYCLE	
t_{WC}	7, 8, 9, 10, 11
t_{WR}	7, 8, 9, 10, 11
t_{PWE}	7, 8, 9, 10, 11
t_{WSD}	7, 8, 9, 10, 11
t_{WHD}	7, 8, 9, 10, 11
t_{WSA}	7, 8, 9, 10, 11
t_{WHA}	7, 8, 9, 10, 11
t_{WSCS}	7, 8, 9, 10, 11
t_{WHCS}	7, 8, 9, 10, 11

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