CISSOID

**The Leader in High Temperature Semiconductor Solutions**

# CHT-MOON DATASHEET

***Version:*** 1.4
***2-Jan-18***
***(Last Modification Date)***

## High-Temperature Medium Power Dual N-channel MOSFET

### General description

The CHT-MOON is a dual, high-voltage N-channel MOSFET in a very dense CSOIC16 SMD package. It is designed to achieve high performance in an extremely wide temperature range: typical operation temperature goes from -55°C to 225°C while keeping leakage currents low.
It has been optimized for use in low and medium power DC-DC converters such as synchronous buck operation, in combination with CISSOID' PWM controller CHT-MAGMA. This product is ideal for compact, high-efficiency DC-DC converters that supply voltages to applications where the operating temperature is high or (and) where reliability is critical.

### Features

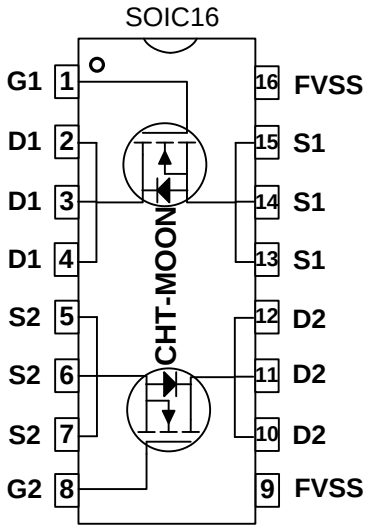
- Specified from -55 to +225°C (Tj)
- Drain voltage up to 40V
- $R_{DSon\ (per\ transistor)}$: 0.65Ω @ 225°C
- VGS =0V to +5V
- Reverse ESD diode between gate and source.
- Available in CSOIC16 package
- Validated at 225°C for 20000 hours (and still on-going)

### Applications

- SMPS, PoL and DC/DC converters
- Low and medium-power push-pull stages in motor drives and inverters

Refer to http://www.cissoid.com/files/files/products/planet/CHT-MOON.pdf for latest datasheet version.

### Package configurations




| Pin # | Pin Name | Pin Description |
|---|---|---|
| 1 | G1 | MOSFET1 gate |
| 2 | D1 | MOSFET1 drain |
| 3 | D1 | MOSFET1 drain |
| 4 | D1 | MOSFET1 drain |
| 5 | S2 | MOSFET2 source |
| 6 | S2 | MOSFET2 source |
| 7 | S2 | MOSFET2 source |
| 8 | G2 | MOSFET2 gate |
| 9 | FVSS | Input pin; to be connected to lowest voltage |
| 10 | D2 | MOSFET2 drain |
| 11 | D2 | MOSFET2 drain |
| 12 | D2 | MOSFET2 drain |
| 13 | S1 | MOSFET1 source |
| 14 | S1 | MOSFET1 source |
| 15 | S1 | MOSFET1 source |
| 16 | FVSS | Input pin; to be connected to lowest voltage |

## Absolute Maximum Ratings

| | |
|---|---|
| Gate-to-Source voltage $V_{GS}$ | -0.5V to 5.5V |
| Drain-to-Source voltage $V_{DS}$ | 0V to 40V |
| $V_{BACK}$-$V_{S1}$ | between -80V and 10V |
| $V_{BACK}$-$V_{S2}$ | between -80V and 10V |
| Pulsed drain current $I_{DS}$ (Tpulse ≤ 2µs): | |
| | 7A @ -55°C |
| | 6A @ 25°C |
| | 4A @ 225°C |
| DC drain current ($V_{GS}$=5V) (1 NMOS) | 3A |
| Power dissipation $T_c$=25°C | 3.33W |

**ESD Rating (expected)**

| | |
|---|---|
| Human Body Model | 2kV |

*Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Frequent or extended exposure to absolute maximum rating conditions or above may affect device reliability.*
*Gate terminals are ESD sensitive; please use appropriate handling methods.*

## Operating Conditions

| | |
|---|---|
| Gate-to-Source voltage $V_{GS}$ | 0V to 5V |
| Drain-to-Source voltage $V_{DS}$ | 0V to 40V |
| Junction temperature | -55°C to +225°C |

See Thermal characteristics for power derating with temperature

# Electrical characteristics (per MOSFET)

## DC Characteristics

Unless otherwise stated, $T_j$ =25°C. **Bold** figures point out values valid over the whole temperature range ($T_j$ =-55°C to +225°C).

| Parameter | Symbol | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Threshold voltage | $V_{TH}$ | $V_{DS}$ =50mV | **0.85** | 1.6 | **1.95** | V |
| Drain cut-off current | $I_{DSS}$ | $V_{GS}$ =0V, $V_{DS}$=40V, $T_j$=25°C | | 15 | | nA |
| | | $V_{GS}$ =0V, $V_{DS}$ =40V, $T_j$=225°C | | 8 | | uA |
| Gate leakage current[1] | $I_{GSS}$ | $V_{GS}$ =5V, $V_{DS}$ =50mV, $T_j$=25°C | | 189 | | pA |
| | | $V_{GS}$ =5V, $V_{DS}$ =50mV, $T_j$=225°C | | 72.1 | | nA |
| Static drain-to-source resistance | $R_{DSon}$ | $V_{GS}$ =5V, $V_{DS}$ =50mV, $T_j$=-55°C | | 0.3 | | Ω |
| | | $V_{GS}$ =5V, $V_{DS}$ =50mV, $T_j$=25°C | | 0.38 | | Ω |
| | | $V_{GS}$ =5V, $V_{DS}$ =50mV, $T_j$=225°C | | 0.65 | | Ω |
| Breakdown drain-to-source voltage[2] | $V_{BRDS}$ | $V_{GS}$ =0V | **40** | | | V |

## Dynamic Characteristics

Unless otherwise stated, $T_j$ =25°C. **Bold** figures point out values valid over the whole temperature range ($T_j$ =-55°C to +225°C).

| Parameter | Symbol | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Input capacitance | $C_{ISS}$ | $V_{GS}$ =0$V_{DC}$, DS shorted | | 370 | | pF |
| Output capacitance | $C_{OSS}$ | $V_{GS}$ =0$V_{DC}$, $V_{DS}$ =40$V_{DC}$ | | 50 | | pF |
| Feedback capacitance | $C_{RSS}$ | $V_{GS}$ =0$V_{DC}$, $V_{DS}$ =40$V_{DC}$ | | 21 | | pF |
| Gate to Source Charge | $Q_{GS}$ | $V_{GS}$ = [0->5]V; VD = 40V | | 3.8 | | nC |

## Switching Characteristics

Unless otherwise stated, $T_j$ =25°C. **Bold** figures point out values valid over the whole temperature range ($T_j$ =-55°C to +225°C).

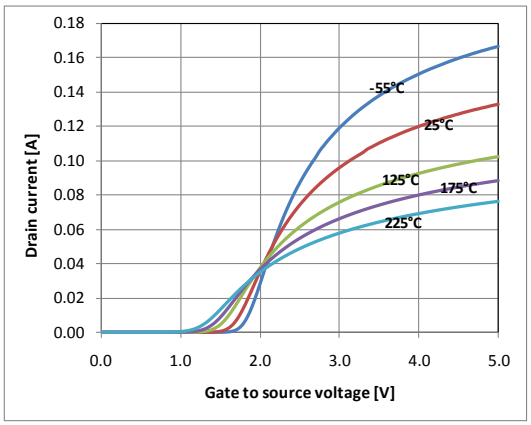
| Parameter | Symbol | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Turn-on delay time | $T_{d(ON)}$ | $V_{DS}$ =20V, $V_{GS}$ =5V 2µs pulse, $R_G$=2.7Ω, $R_D$=8.2Ω | | **30** | | ns |
| Rise time | $T_r$ | $V_{DS}$ =20V, $V_{GS}$ =5V 2µs pulse, $R_G$=2.7Ω, $R_D$=8.2Ω | | **50** | | ns |
| Turn-off delay time | $T_{d(OFF)}$ | $V_{DS}$ =20V, $V_{GS}$ =5V 2µs pulse, $R_G$=2.7Ω, $R_D$=8.2Ω | | **35** | | ns |
| Fall time | $T_f$ | $V_{DS}$ =20V, $V_{GS}$ =5V 2µs pulse, $R_G$=2.7Ω, $R_D$=8.2Ω | | **15** | | ns |
| Drain current | $I_D$ | $V_{DS}$ =40V, $V_{GS}$ =5V 2µs pulse, -55°C | | 6.6 | | A |
| | | $V_{DS}$ =40V, $V_{GS}$ =5V 2µs pulse, 25°C | | 5.7 | | A |
| | | $V_{DS}$ =40V, $V_{GS}$ =5V 2µs pulse, 225°C | | 3.9 | | A |

# Thermal Characteristics

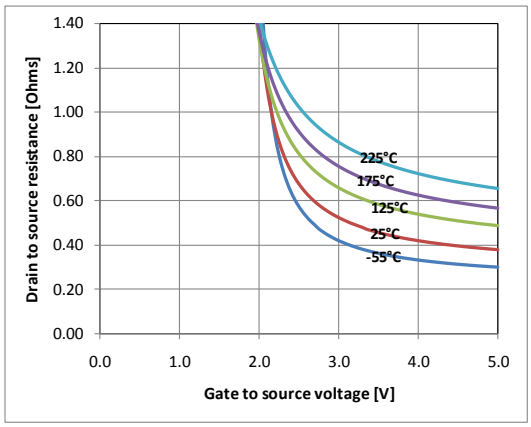
| Parameter | Symbol | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Thermal resistance (junction to air, CSOIC16) | $\Theta_{JA}$ | | | 60 | | °C/W |

[1] Includes ESD diode leakage current.
[2] Voltage for which the cut-off current evolution versus $V_{DS}$ becomes exponential.

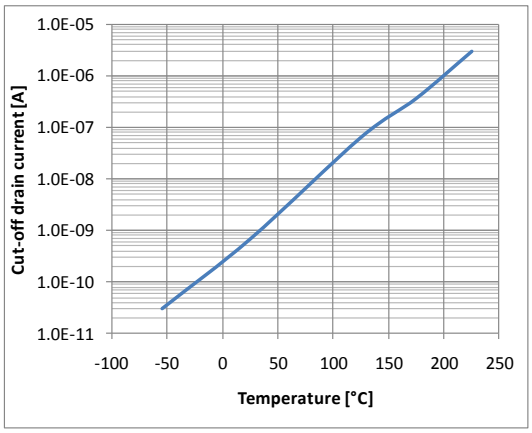
## Typical Performance Characteristics (per MOSFET)



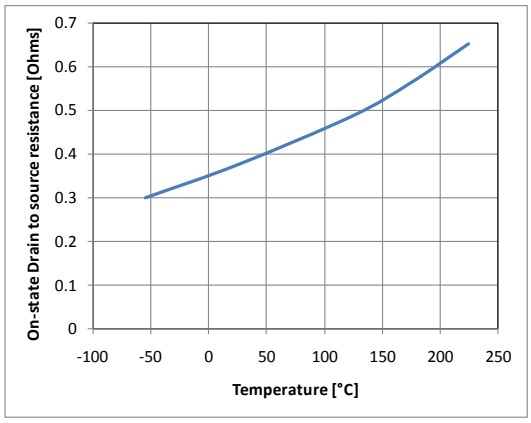

Drain current vs. gate voltage ($V_D$ = 50mV)



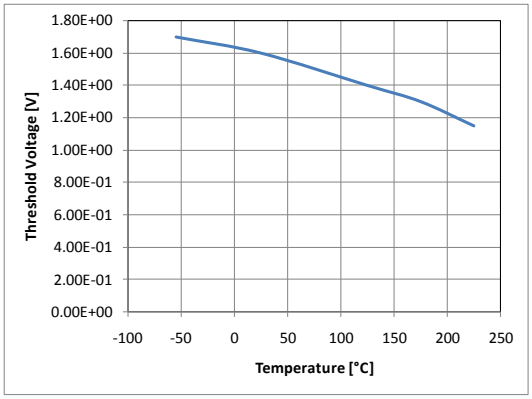

Drain source resistance vs. Drain source voltage ($V_D$ = 50mV)



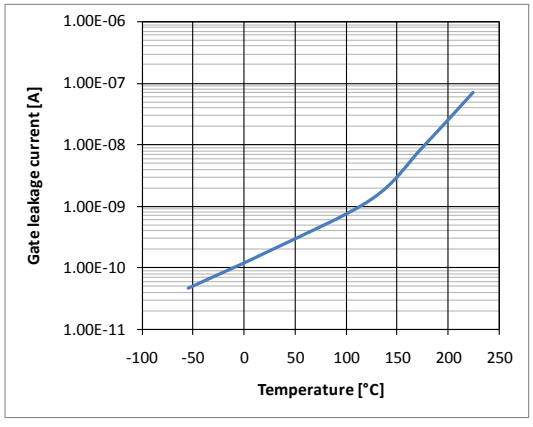

Cut-off current vs. temperature ($V_G$ =0V, $V_D$ = 40V)



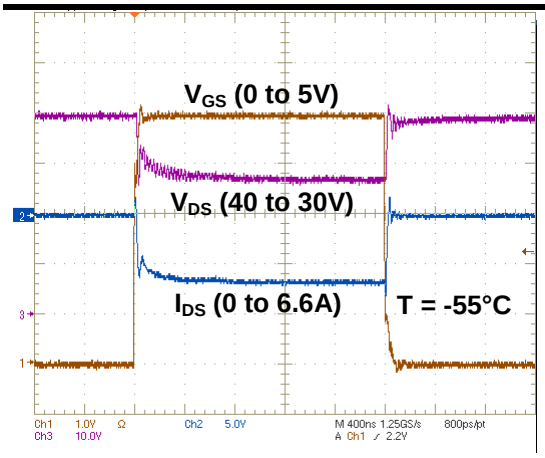

On-state drain source resistance vs. temperature ($V_G$ =5V, $V_D$ =50mV)



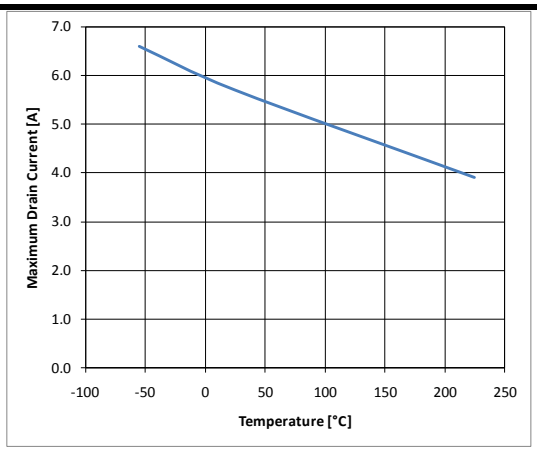

Threshold voltage vs. temperature



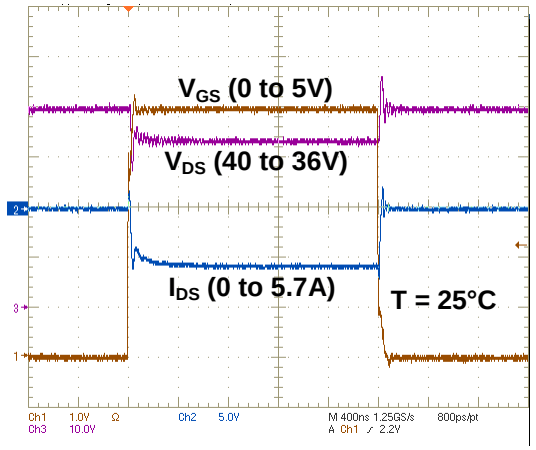

Gate and ESD diode leakage current vs. temperature ($V_G$ =5V, $V_D$ =50mV)



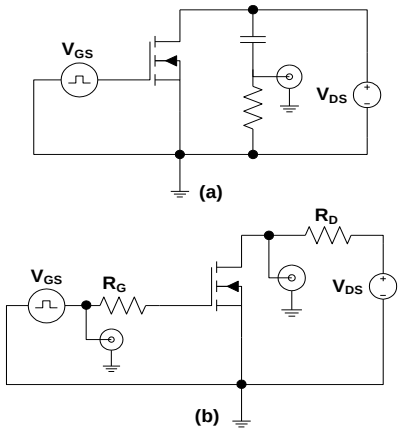

Maximum drain current pulse test (T =-55°C)



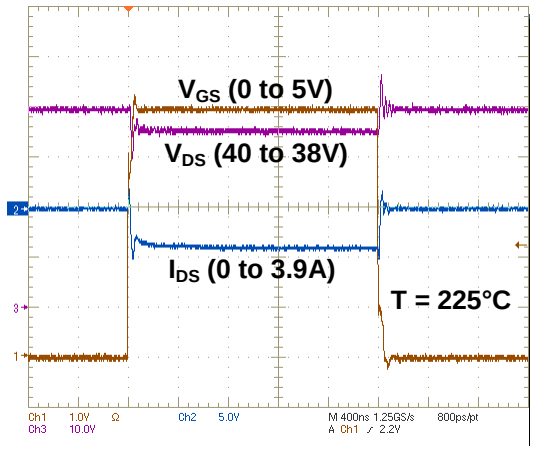

Peak drain current vs. temperature ($V_G$ = 5V, $V_D$ = 40V)



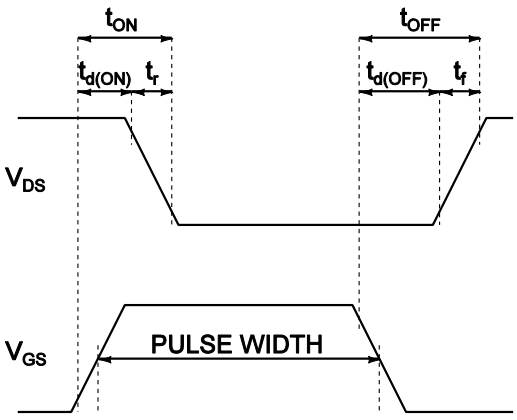

Maximum drain current pulse test (T =25°C)



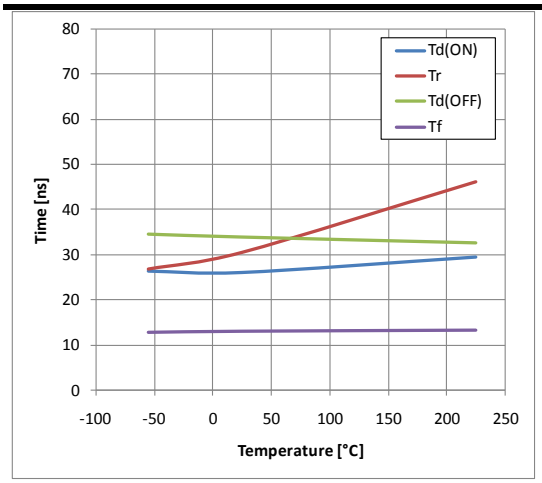

(a) $I_D^{MAX}$ measurement scheme R=1Ω, C=100µF, Compliance ($V_{DS}$=40V)=20mA (b) Timing measurement scheme $R_G$=2.7Ω, $R_D$=8.2Ω, $V_{DS}$=20V



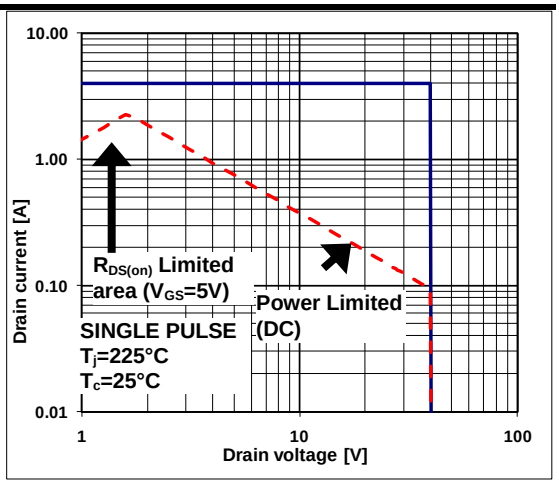

Maximum drain current pulse test (T =225°C)




Timing definition diagram



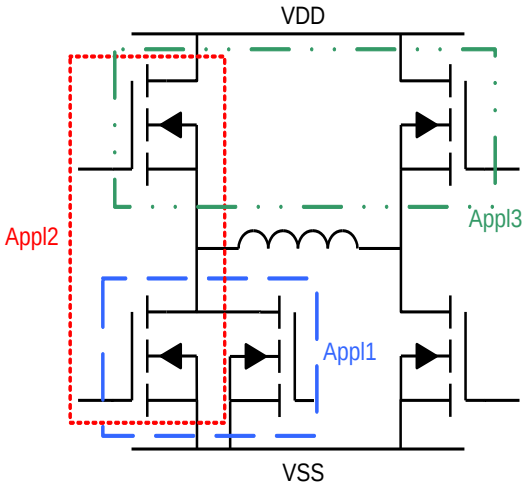

**Timing parameters versus temperature**




**Forward bias safe operating area**
(drain current = sum of drain current in both MOSFET devices)

## General description
## Applications

The 2 NMOS devices of CHT-MOON can be used in a variety of combinations. The figure below illustrates a few of them.




In Application1, the 2 NMOS are connected in parallel; this is useful for systems where Ron (and associated power dissipation) should be minimized

In Application2, the 2 NMOS form the push-pull stage of a half-bridge driver. This is the typical use case of a DC/DC synchronous buck converter.

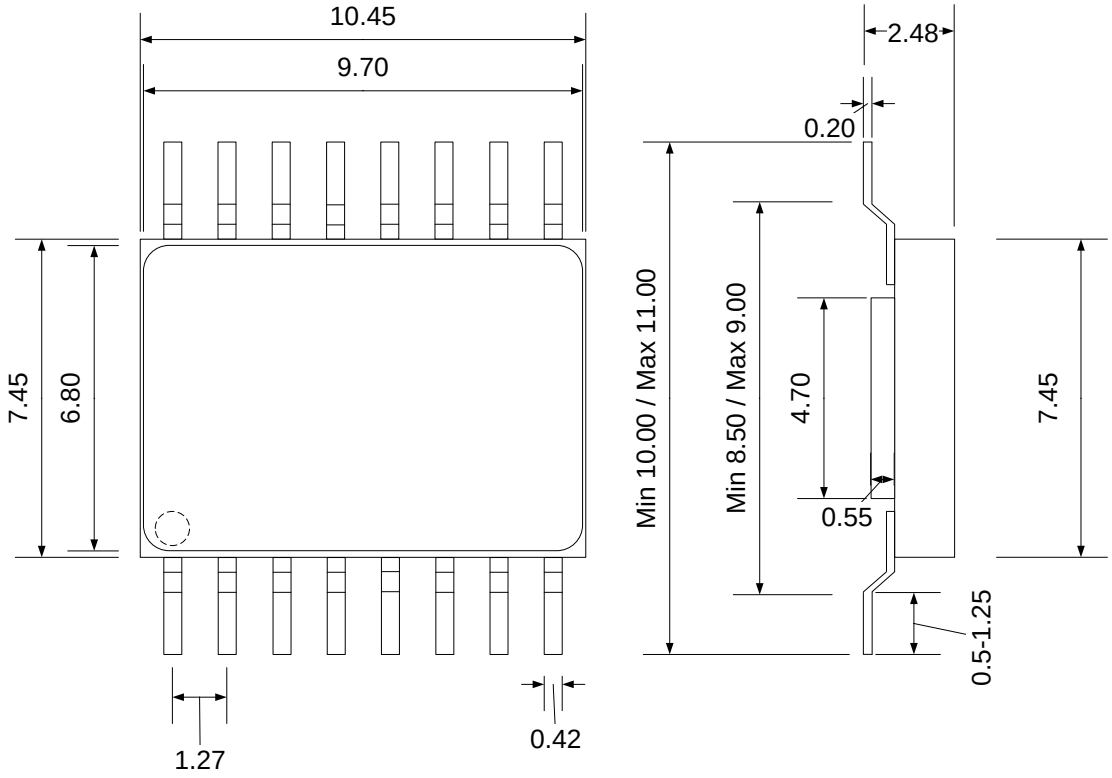
In Application3, the 2 NMOS implement the high side of a bridge driver.

In all cases, FVSS signal should be connected to the lowest potential e.g. VSS.

## Ordering Information

| Ordering Reference | Package | Temperature Range | Marking |
|---|---|---|---|
| CHT-PLA2016A-CSOIC16-T | CSOIC16 | -55°C to +225°C | CHT-PLA2016A |

## Package Drawing




CSOIC 16 Drawing (mm +/- 10%)

# Contact & Ordering

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| | |
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