CHT-RHEA DATASHEET

Version: 2.5
29-Aug-18
(Last Modification Date)

High-temperature Dual-Channel Isolated Transceiver

General Description

The CHT-RHEA is a high-temperature, high reliability integrated circuit that implements a dual-channel full duplex isolated data transceiver. It can be used in any application where there is a need to galvanically isolate a digital data line. The galvanic isolation is achieved by means of an external pulse transformer for each digital signal. The CHT-RHEA integrates in a single package 2 transceivers (2 transmit and 2 receive channels). A complete 4 lines data transmission (2 full duplex channels) requires 2 instances of CHT-RHEA, one being connected to the primary side of the transformers and one to the secondary side.

Each transmit channel (Tx) implements a modulation block using a circuit's built-in clock generator, which frequency can be programmed with one among 7 different values inside the range [5.9-15.3 Mhz]. Each receive channel (Rx) demodulates the signal coming from the transformer. The data transmission rate is up to 2 Mbit/s. During power-up of the circuit, the output signals can be forced to the 0 state through the control input pin ENABLE.

CHT-RHEA offers state-of-the-art digital signal isolation with substantial advantages over opto-couplers such as lower transmission delay, high reliability, lower power consumption, high immunity to dV/dt and operation in extreme temperature conditions.

The solution can be used anywhere there is a need to isolate control lines or status/ fault reporting lines in high voltage systems or to communicate data in sensing systems.

The complete solution is optimized to minimize the size of the transformer, the number of external components, the transmission delay (<100ns) and to maximize the noise margin, even in harsh dV/dt conditions (50kV/µs).

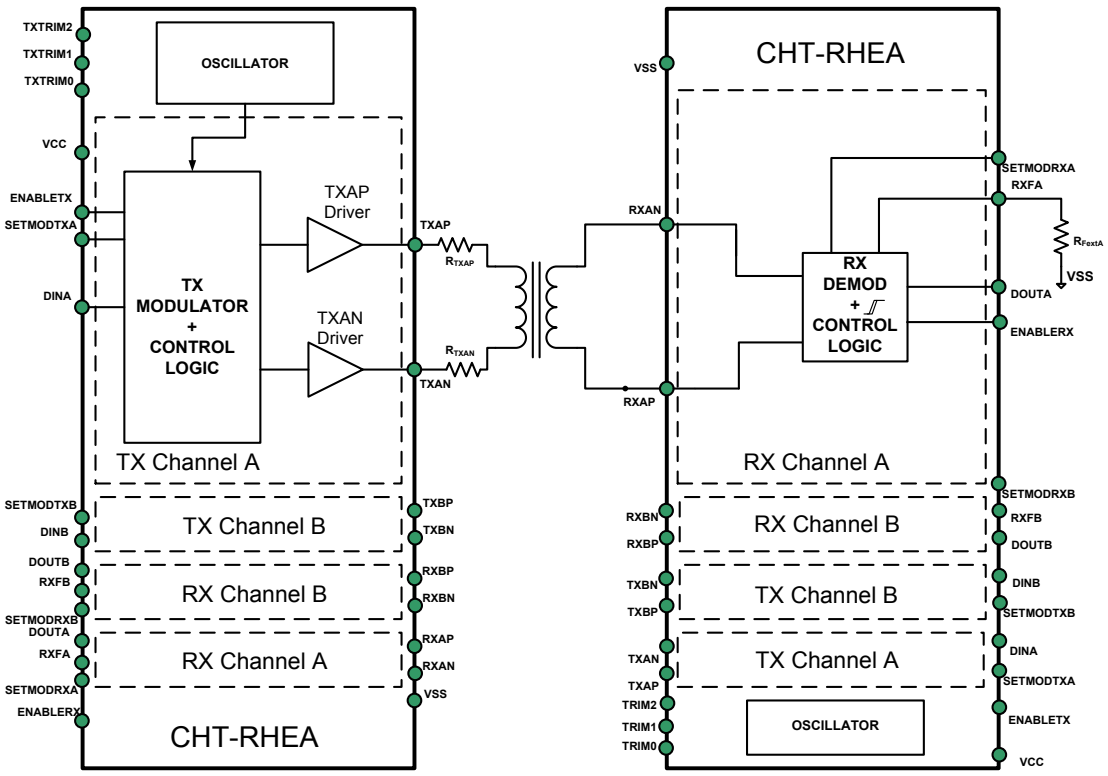
Features

- Operating junction temperature: from -55°C to +225°C
- 2 transmit (Tx) and 2 receive (Rx) channels
- Data rate up to 2 Mbits/sec per channel
- Transmission delay: max 100 ns
- Jitter (RMS cycle-2-cycle) : max 21 ns
- Power supply: 5V
- Low power consumption: 50 mW per channel (1 MHz NRZ input signal)
- Hysteresis on digital input for noise immunity
- Isolation: 10 MΩ @2500V
- High common mode transient immunity: 50KV/µS
- ENABLE control signal on both TX and RX functions
- On-Off Keying modulation
- Programmable modulation frequency (to manage EMC requirements of specific applications)
- Modulation polarity change by configuration
- Validated at 225°C for 10000 hours (and still on-going)
- Package: CSOIC28

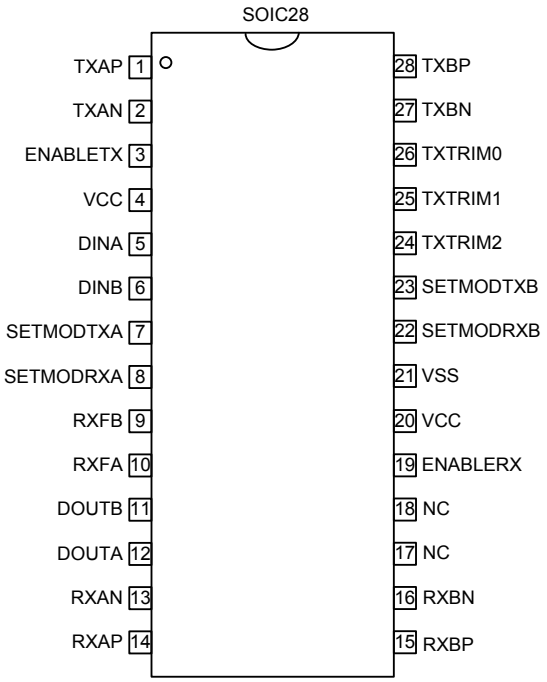
Applications

- Isolated gate drive for IGBT, MOSFET, JFET and SiC Transistors
- Isolated sensor interfaces
- Galvanic isolation of A-D converters
- Galvanic isolation of standard RS-232 / RS-422 / RS-485 / I2C transmission links
- Industrial field bus isolation
- Industrial power inverters
- Motor drives and battery management in EV / HEV

Functional Block Diagram



Package configuration and Pin Description



Pin #	Pin Name	Pin type	Pin Description
1	TXAP	Output	Positive differential output of TX channel A; to be connected to the primary of the transformer.
2	TXAN	Output	Negative differential output of TX channel A; to be connected to the primary of the transformer.
3	ENABLETX	Input	Controls the activation of the 2 TX channels; while at logical zero, both TX channels are disabled and TXAP/TXAN, TXBP/TXBN are forced to VSS level
4	VCC	Power supply	Positive power supply
5	DINA	Input	Schmitt trigger input of TX channel A
6	DINB	Input	Schmitt trigger input of TX channel B
7	SETMODTXA	Input	Controls the “polarity” of the modulation of TX channel A; cfr TX channel true table for more information
8	SETMODRXA	Input	Controls the “polarity” of the RX channel A demodulation
9	RXFB	Input/ Output	Connected to the internal demodulation node of RX channel B; Resistance RFextB to be connected between this node and VSS
10	RXFA	Input/ Output	Connected to the internal demodulation node of RX channel A; Resistance RfextA to be connected between this node and VSS
11	DOUTB	Output	Output of RX channel B
12	DOUTA	Output	Output of RX channel A
13	RXAN	Input	Negative differential input of RX channel A; to be connected to the secondary of the transformer.
14	RXAP	Input	Positive differential input of RX channel A; to be connected to the secondary of the transformer.
15	RXBP	Input	Positive differential input of RX channel B; to be connected to the secondary of the transformer.
16	RXBN	Input	Negative differential input of RX channel B; to be connected to the secondary of the transformer.
17	NC	Input	Not connected internally; can be left floating or connected to any net to ease PCB routing
18	NC	Input	Not connected internally; can be left floating or connected to any net to ease PCB routing
19	ENABLERX	Input	Controls the output of the 2 RX channels; while at logical zero, both RX channel outputs (DOUTA and DOUTB) are forced to VSS level
20	VCC	Input	Positive power supply
21	VSS	Power supply	Negative power supply
22	SETMODRXB	Input	Controls the “polarity” of the RX channel B demodulation
23	SETMODTXB	Input	Controls the “polarity” of the modulation of TX channel B; cfr TX channel true table for more information
24	TXTRIM2	Input	Control bit of the internal oscillator clock divider
25	TXTRIM1	Input	Control bit of the internal oscillator clock divider
26	TXTRIM0	Input	Control bit of the internal oscillator clock divider
27	TXBN	Output	Negative differential output of TX channel B; to be connected to the primary of the transformer.
28	TXBP	Output	Positive differential output of TX channel B; to be connected to the primary of the transformer.

CHT-RHEA: Absolute Maximum Ratings

These ratings are considered individually (not in combination). If not specified, voltages are related to VSS.

Parameter	Min.	Max.	Units
(VCC-VSS)	-0.5	5.5	V
Junction Temperature		225	°C
ESD Rating (Human Body Model) (expected)	2		kV

Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Frequent or extended exposure to absolute maximum rating conditions or above may affect device reliability.

Electrical Characteristics

Unless otherwise stated: T_j=25°C. **Bold underlined** values indicate values over the whole temperature range (-55°C < T_j < +225°C).

Parameter	Condition	Min	Typ	Max	Units
Supply voltage (VCC)		**4.5**		**5.5**	V
Supply current (1 TX + RX path)	DINx = all '0' (duty cycle = 0%); C_{DOUT} = 50 pF; TXTRIM[2..0] = '000 SETMODxxx = '0''		1.28		mA
	DINx = all '1' (duty cycle = 100%) ; C_{DOUT} = 50 pF; TXTRIM[2..0] = '000' SETMODxxx = '0'		18		mA
	DINx = 1 MHz NRZ signal (duty cycle = 50%); C_{DOUT} = 50 pF; TXTRIM[2..0] = '000' SETMODxxx = '0'		10		mA
Supply quiescent current	ENABLETX=0; ENABLERX=0		135	**230**	µA
Maximum data rate				**2**	Mbps
Modulation frequency	Using TXTRIM[2-0] control signals Discrete steps (cfr next section)	5.9		15.3	MHz
Modulation frequency variation	Includes process/temperature/power supply variations	**-35**		**+40**	%
Modulation frequency duty cycle	Includes process/temperature/power supply variations	**48.5**		**51.5**	%
Propagation delay	TXTRIM[2..0]= '0xx'			**100**	ns
Jitter (RMS cycle-2-cycle)	TXTRIM[2..0]= '0xx'			**21**	ns
Start-up time	When ENABLE goes to 1		100		ns
Isolation	At 2500V	**10**			MΩ
Common mode transient immunity				**50**	KV/µS
TX Channel					
High state output resistance	On each TX output			**9**	Ω
Low state output resistance	On each TX output			**6.7**	Ω
Propagation delay	Input rising (DINA->TXAP/N) R_{TXAP}+R_{TXAN} =50Ohms			**20**	ns
	Input falling (DINA->TXAP/N) R_{TXAP}+R_{TXAN} =50Ohms			**20**	ns
Minimum HIGH voltage level for digital inputs	Applies to:DINA, DINB, ENABLEx, SETMODx, TXTRIMx	**3.84**			V
Maximum LOW voltage level for digital inputs	Applies to:DINA, DINB, ENABLEx, SETMODx, TXTRIMx			**1.1**	V
Hysteresis		**1.68**	2.07	**2.39**	V
RX Channel					
External resistor R_{FEXTx}			1100		Ohms
Minimum HIGH level output voltage V_{OH}	I_{OH} < 8mA (source); applies to DOUTA & DOUTB	**4.4**			V
Maximum LOW level output voltage V_{OL}	I_{ol} < 8mA (sink); applies to DOUTA & DOUTB			**0.63**	V
Output Rise/Fall Time (10% to 90%)	On 50 pF external capacitance		3		ns

Typical Performance Characteristics

Unless otherwise stated: VCC = 5V.

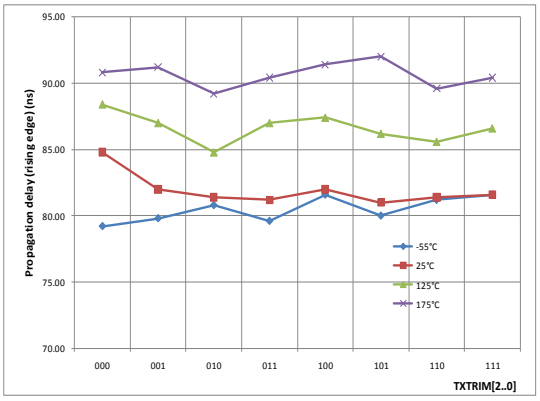


Figure 1: Propagation delay (rising edge) vs. TXTRIM[2..0] configuration bits and temperature

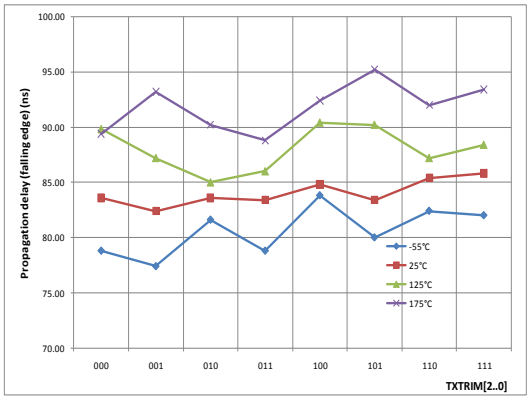


Figure 2: Propagation delay (falling edge) vs. TXTRIM[2..0] configuration bits and temperature

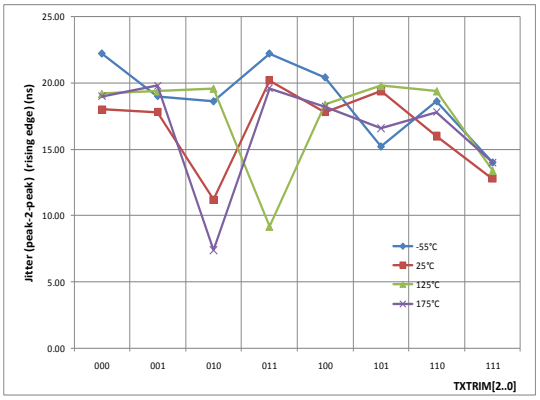


Figure 3: Jitter (peak-2-peak) (rising edge) vs. TXTRIM[2..0] configuration bits and temperature

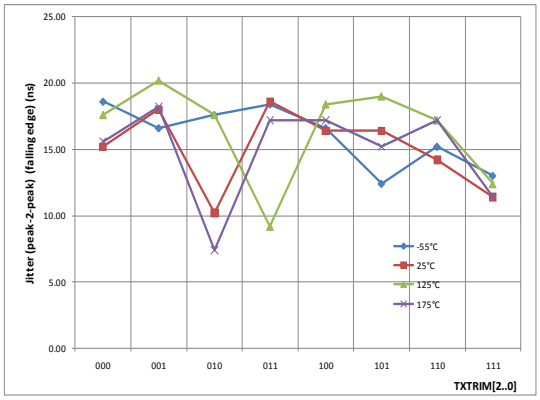


Figure 4: Jitter (peak-2-peak) (falling edge) vs. TXTRIM[2..0] configuration bits and temperature

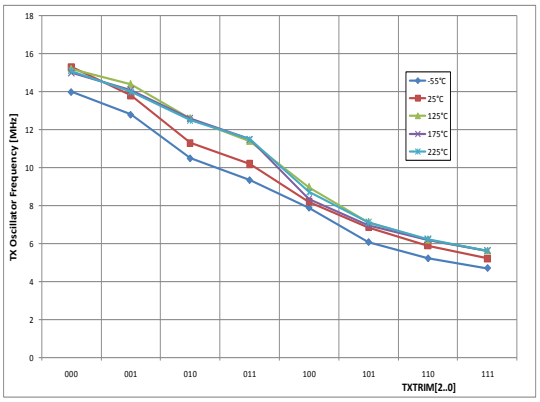


Figure 5 : TX Oscillator Frequency vs. TXTRIM[2..0] configuration bits and temperature

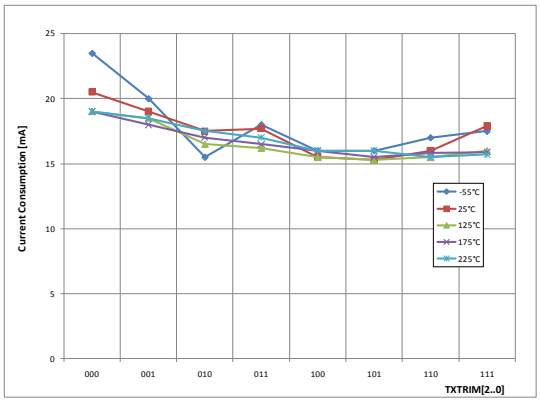


Figure 6 : Consumption vs. TXTRIM[2..0] configuration bits and temperature (all channels active, Input= 1MHz NRZ, DOUT load = 50 pF, SETMODTX/RX = '0')

General description

Transmit Block functionalities

The Transmit channel uses an internally generated clock to modulate the input signal and to generate 2 complementary outputs.

The 2 outputs drive the primary side of the pulse transformer in a differential manner.
Care has been taken in the component design to achieve 50% duty cycle on the TX outputs and so to avoid creating DC current inside the transformer.
For proper operation, R_{TXAN} and R_{TXAP} should be set to 5Ω.

The TX channel modulation clock frequency can be selected (7 discrete values) in the range [5.9Mhz-15.3Mhz]. Table below provides the modulation frequency in function of the 3 control signals (TXTRIM[2..0]) at 25°C.

TXTRIM [2..0]	Typ. Clock freq (MHz)
000	15.3
001	13.8
010	11.3
011	10.2
100	8.21
101	6.86
110	5.91
111	forbidden

This function can be used to manage potential electromagnetic compatibility issues at system level by moving the modulation clock frequency outside of system critical frequency bands.

ENABLETX signal offers the capability to tie down the 2 outputs of both channels. This signal is active high. In a typical application, this signal could be connected to the system power-on reset to ensure that no spurious transmission is taking place till system power-up is completed.

Finally, with SETMODTXA/B signal, one can invert the polarity of the Transmit Channel. Combined with the equivalent function on the Receive Block, the polarity of the modulation can be inverted while maintaining a non-inverting polarity end-to-end. This feature can be used to optimize the power dissipation of the isolated data transmission function.

The table below provides the complete logical truth table of the TX block.

CLK	DINx	ENABLE TX	SETMOD TXx	TXAP	TXAN
1	1	1	0	1	0
0	1	1	0	0	1
1	0	1	0	0	0
0	0	1	0	0	0
1	X	0	0	0	0
0	X	0	0	0	0
1	1	1	1	0	0
0	1	1	1	0	0
1	0	1	1	1	0
0	0	1	1	0	1
1	X	0	1	0	0
0	X	0	1	0	0

Receive Block functionalities

The Receive Block demodulates the differential signal sent through the pulse transformer by the Transmit Block.

The 2 differential inputs of each Receive Block are connected to the secondary of the transformer. $R_{FextA/B}$ resistance controls the demodulation function.

ENABLERX signal offers the capability to tie down the RX channel output. This signal is active high. In a typical application, this signal could be connected to the system power-on reset to ensure that no spurious transmission is taking place till system power-up is completed.

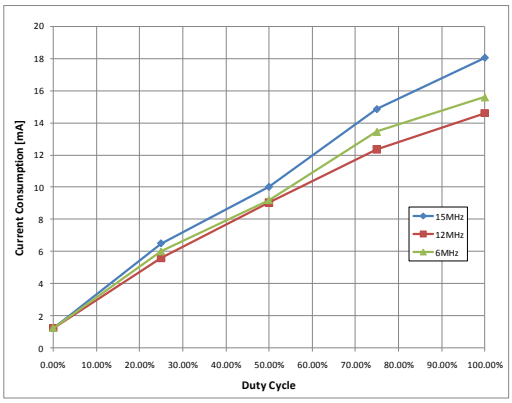
Finally, with SETMODRXA/B signal, one can invert the polarity of the Receive Channel. Combined with the equivalent function on the Transmit Block, the polarity of the modulation can be inverted while maintaining a non-inverting polarity end-to-end.
This feature can be used to optimize the power dissipation of the isolated data transmission function.

The table below provides the complete logical truth table of the RX block.

RX demodulated signal	ENABLE RX	SETMOD RXx	DOUTx
X	0	X	0
1	1	0	1
0	1	0	0
1	1	1	0
0	1	1	1

Power dissipation

The supply current of RHEA is a function of the supply voltage, the input data rate, the input data "duty cycle" (the average percentage of "1" in the input data stream), the settings SETMODTX/SETMODRX, the TX oscillator frequency and the load on DOUT.
The graph below provides supply current information for a complete TX+RX channel in function of TX oscillator frequency and input data "duty cycle" (0% = all "0" signal , 100% = all "1" signal, 50% = standard NRZ signal, Supply Voltage= 5V, DOUT load = 50 pF, SETMODTX/RX = '0').



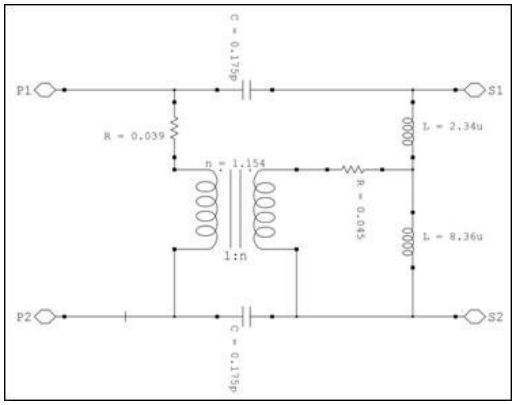
Influence of the input data rate can be considered as marginal compared to the other parameters.

Transformer

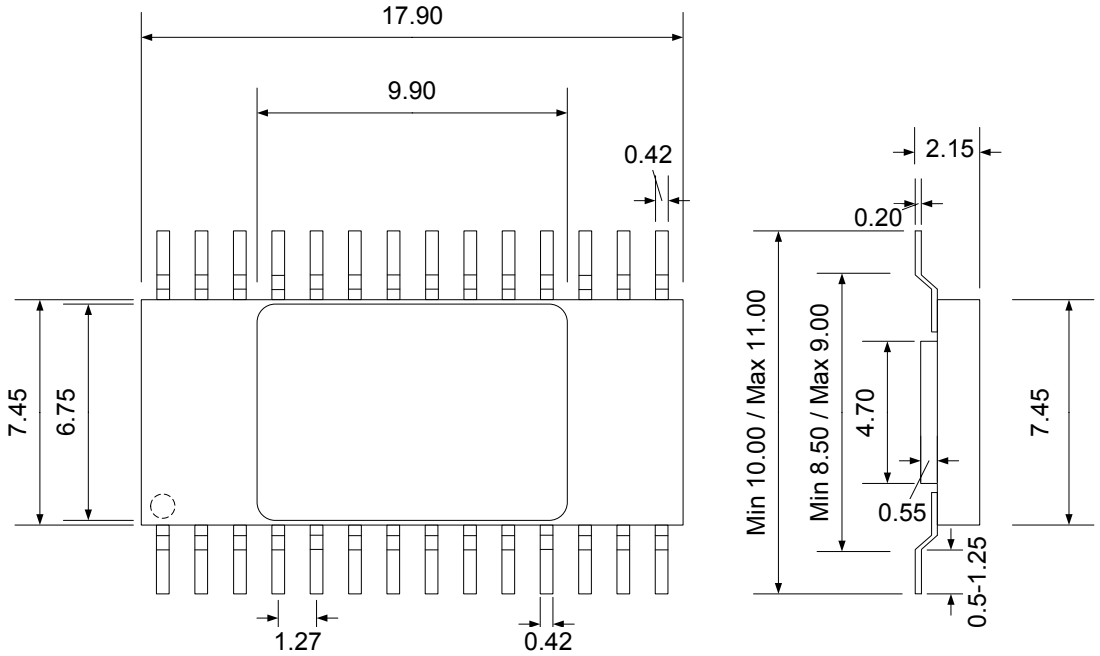
The transformer design has to cope with following constraints:

- Minimize parasitic capacitance (Cp) between Primary and Secondary; ideally Cp should be lower than 0.5 pF
- Respect isolation requirements
- Minimize core size
- Maximum current on primary side of 20 mA (CHT-RHEA drive capability)
- Primary driver power supply: 5V
- Maximum switching frequency: 20 MHz
- Secondary to primary ratio of about 1.1 (ideally 1 but needs to be slightly higher to compensate transformer losses)

The selected transformer has an equivalent electrical model as shown in figure below. The winding ratio (P/S) is 13/15.



Package Drawing



CSOIC 28 Drawing (mm +/- 10%)

Ordering Information

Ordering Reference	Package	Temperature Range	Marking
CHT-TIT4750G-CSOIC28-T	CSOIC28	-55°C to +225°C	CHT-TIT4750G

Contact & Ordering

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