CHT-THEMIS

Version: 2.2
12-Nov-13
(Last Modification Date)

Power Transistor Driver Controller

General description

CHT-THEMIS is the controller block of the Power Transistor Driver solution CHT-THEMIS and CHT-ATLAS. The chipset is specifically designed to drive wide-bandgap power transistors, in particular Gallium Nitride (GaN) and Silicon Carbide (SiC) devices including normally-On and normally-Off JFETs, MOSFETs and BJTs. It is also used with standard silicon MOSFETs and IGBTs in standard temperature applications (e.g. 125°C) where it brings an increase in reliability and lifetime by an order of magnitude compared to traditional solutions. CHT-THEMIS can drive up to 5 CHT-ATLAS chips for very high power applications that require up to ±20A to the gate of the power device. It implements a state machine that manages the control and the fault signals, it embeds a voltage reference as well as a 5V linear voltage regulator which is used to supply CHT-ATLAS. This 5V power supply can also be used to power up other external circuits, such as the isolated transceiver CHT-RHEA for complete isolated gate-drive implementations. The circuit features an adjustable under-voltage lockout (UVLO) function with hysteresis as well as a de-saturation detection circuit. It also includes a pulse generation pre-driver to accommodate for Normally Off SiC JFET. CHT-THEMIS also features an active Miller clamping (AMC) function and pre-driver for an external transistor.

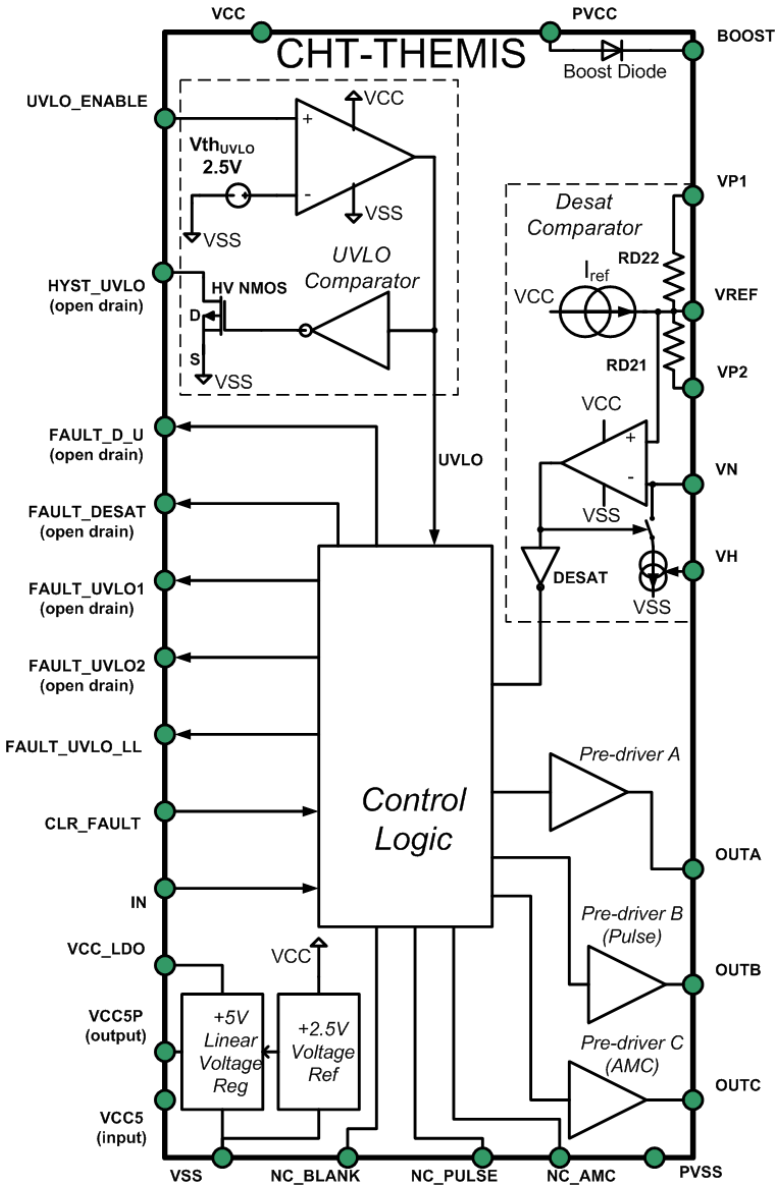
Features

- Operating junction temperature: from -55°C to +225°C
- Supply Voltage: 5 to 30V
- Adjustable Under-voltage lockout (UVLO)
- De-saturation detection circuit
- Active Miller clamping (AMC) support
- Validated at 225°C for 5000 hours (and still on-going)
- Package: CSOIC28

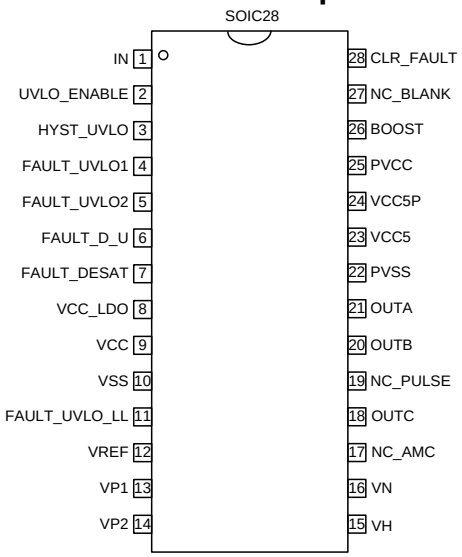
Applications

- Intelligent Power Modules (IPM)
- Power conversion, power generation and actuator controls in aeronautics
- Solar inverters
- Motor drives, battery chargers and DC-DC converters in EV / HEV
- Power conversion and motor drive in railway
- Switched mode power supplies (SMPS)
- Wind turbine power converters

Functional Block Diagram



Package Configurations and Pin Description:



Pin #	Pin Name	Pin Description
1	IN	Schmitt triggered input of the driver. 5V CMOS input with respect to VSS.
2	UVLO_ENABLE	Positive input of the under-voltage lockout (UVLO) comparator. The UVLO threshold is set comparing the supply voltage multiplied by (RUVLO2/(RUVLO2+RUVLO3)) with the comparator threshold Vth_{UVLO} (≅2.5V)
3	HYST_UVLO	Open-drain output providing a feedback of the UVLO signal in order to set the hysteresis of the UVLO threshold. The drain is open when UVLO=1 (supply voltage above the threshold).
4	FAULT_UVLO1	Open-drain output for the under-voltage lockout (UVLO) FAULT signal. This output is pulled up when the supply voltage is below UVLO threshold.
5	FAULT_UVLO2	Open-drain output for the under-voltage lockout (UVLO) FAULT signal. This output is pulled up when the supply voltage is below UVLO threshold.
6	FAULT_D_U	Open-drain output combining FAULT_UVLO and FAULT_DESAT signals. This output in pulled down when the supply voltage is below UVLO threshold or when a desaturation has been detected.
7	FAULT_DESAT	Open-drain output for the desaturation FAULT signal. This output is pulled down when a desaturation has been detected.
8	VCC_LDO	Positive power supply of the internal voltage regulator. Connect to an external supply voltage from 7V to 30V.
9	VCC	Positive power supply. Connect to an external supply voltage from 7V to 30V.
10	VSS	Negative power supply. Connect to ground or to a negative supply when a negative drive is necessary.
11	FAULT_UVLO_LL	Logic level output for the under-voltage lockout (UVLO) FAULT signal. This output is low when the supply voltage is below UVLO threshold.
12	VREF	Midpoint of RD22-RD21 resistor divider (available if external tuning is necessary)
13	VP1	First positive input of the DESAT comparator
14	VP2	First positive input of the DESAT comparator
15	VH	Connected to VCC5P through a resistor to set the hysteresis voltage of the DESAT comparator
16	VN	Negative input of the DESAT comparator
17	NC_AMC	To be bypassed to VSS by a capacitor in order to set the time constant t_{amc} (refer to OUTC output pin description)
18	OUTC	Output of Pre-driver C (5V/250mA output buffer) This output is used to drive an external N-channel MOSFET transistor used for Active Miller Clamping. It inverts OUTA on rising edge of OUTA. It inverts and delays (by t_{amc}) OUTA on falling edges of OUTA. The duration of t_{amc} is set by the capacitor on node NC_AMC
19	NC_PULSE	To be bypassed to VSS by a capacitor in order to set the pulse width on OUTB output. This pulse is triggered by the rising edge of the input signal on node IN.
20	OUTB	Output of Pre-driver B (5V/250mA output buffer) This output is used to drive Normally-Off SiC JFET. It generates a short pulse triggered by rising edge on IN input. The duration is set by the capacitor on node NC_PULSE
21	OUTA	Output of Pre-driver A (5V/250mA output buffer)
22	PVSS	Negative power supply of driver output stage. To be connected to VSS
23	VCC5 (input)	5V positive power supply of the control logic. To be connected VCC5P
24	VCC5P (output)	5V positive output with respect to VSS. To be bypassed to VSS by a decoupling capacitor (of appropriate value for the application).
25	PVCC	Positive power supply of the boost diode. Connect to an external supply voltage from 7V to 30V.
26	BOOST	Cathode of the on-chip boost diode
27	NC_BLANK	To be bypassed to VSS by a capacitor in order to set the blanking time of the desaturation comparator. After the blanking time, the result of the FAULT comparator is read.
28	CLR_FAULT	Schmitt triggered input of the FAULT state clearing signal. 5V CMOS input with respect to VSS.

Absolute Maximum Ratings

Parameter	Min.	Max.	Units
(VCC-VSS)	-0.5	35	V
(VCC5P-VSS)	-0.5	6	V
(BOOST-VCC)	-0.5	35	V
OUTA, OUTB, OUTC	PVSS-0.5	VCC5P+0.5	V
IN, CLR_FAULT	VSS-0.5	VCC5P+0.5	V
VP1, VP2	VSS-0.5	VCC+0.5	V
VN	VSS-0.5	VCC+0.5	V
UVLO_ENABLE	VSS-0.5	VCC+0.5	V
NC_BLANK, NC_PULSE, NC_AMC	VSS-0.5	VCC5P+0.5	V
(VSS-PVSS)	-0.5	0.5	V
(PVCC-PVSS)	-0.5	35	V
Junction Temperature		250	°C
ESD Rating (Human Body Model)	2 (expected)		kV
Max power dissipation		1	W

Operating conditions

Parameter	Min.	Max.	Units
(VCC-VSS)	0	30	V
(VCC5P-VSS)	0	5.5	V
(BOOST-VCC)	0	35	V
IN, CLR_FAULT	VSS	VCC5P	V
VP1, VP2	VSS	VCC	V
VN	VSS	VCC	V
UVLO_ENABLE	VSS	VCC	V
NC_BLANK, NC_PULSE, NC_AMC	VSS	VCC5P	V
(VSS-PVSS)	-0.1	0.1	V
(PVCC-PVSS)	0	30	V
Junction Temperature		225	°C
Max power dissipation		0.5	W

Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Frequent or extended exposure to absolute maximum rating conditions or above may affect device reliability.

Electrical Characteristics

Unless otherwise stated: (VCC-VSS)=15V, T_j=25°C. **Bold underlined** values indicate values over the whole operational temperature range (-55°C < T j < +225°C).

Parameter	Condition	Min	Typ	Max	Units
External Power Supply					
External Power Supplies[1] (PVCC & VCC) versus VSS	If internal linear voltage regulator is bypassed	4.75		5.25	V
	If internal linear voltage regulator is used	7		30	V
VCC quiescent current	Ta = 25°C		1.53	**2.5**	mA
VCC_LDO quiescent current				**0.5**	mA
PVCC quiescent current				**0.1**	mA
VCC average current	IN signal = 20kHz, 50% duty cycle, Ta = 25°C		1.73		mA
5V Internal Power Supply					
Internal 5V Power Supply[2] (VCC5P) versus VSS	(VCC-VSS) from 7V to 30V, Iout from 0.25mA to 25mA	**4.75**	5	**5.25**	V
Output Capacitor C5P	Capacitor value at Tamb=25°C		1		µF
Output Current		**0.25**		**25**	mA
Initial Accuracy	(VCC-VSS)= 15V; Iout=2.5mA		+/-1.2		%
Drift with temperature	(VCC-VSS)= 15V; Iout=2.5mA		0.5		mV/°C
Line Regulation	(VCC-VSS) from 7V to 30V; Iout=2.5mA		+/-0.1		%
Load Regulation	(VCC-VSS)= 15V; Iout from 2.5mA to 25mA		1.25		%
Under-voltage Lockout (UVLO)					
Internal UVLO comparator threshold voltage		**2.375**	2.5	**2.625**	V
Internal UVLO comparator threshold voltage: absolute accuracy	(PVCC-PVSS) from 7V to 30V	**-5**		**5**	%
Open-drain transistor ON-Resistance	Note: transistor drain is HYST_UVLO pin		1K		Ω
Delay from UVLO_ENABLE to FAULT_UVLO	500mV overdrive[3]		100		ns
Delay from UVLO_ENABLE to driver outputs (OUTA and OUTB) when VCC goes low	CLoad=0.5nF		100		ns
UVLO_ENABLE Max forced input current[4]				**3**	mA
UVLO_ENABLE Max input leakage current		**-3**		**+3**	µA
Input signal (IN, CLR_FAULT)					
Input start threshold		**3.03**	3.43	**3.83**	V
Input stop threshold		**1.1**	1.39	**1.68**	V
Hysteresis		**1.68**	2.04	**2.39**	V
Pre-Drivers					
Output sink current (OUTA/B)			0.25		A
Output source current (OUTA/B)			0.25		A
Propagation delay when output rising (IN→OUTA/B)	CLoad=0.5nF (50%→ 50%)		30		ns
Propagation delay when output falling (IN→OUTA/B)	CLoad=0.5nF (50%→ 50%)		30		ns
Rise Time (10%-90%)	CLoad=0.5nF		10		ns
Fall Time (10%-90%)	CLoad=0.5nF		10		ns
Pulse time t_{pulse} for a given	C_{PULSE}=30pF[5]	**75**	100	**125**	ns

[1] Voltage externally supplied to the chip
[2] 5V supply generated on-chip
[3] This delay is obtained for a step from 2V to 3V with a rise time of 10ns at node UVLO_ENABLE
[4] Comparator differential voltage (V+-V-) is clamped to about 5V by current limiting diodes able to absorb 3mA
[5] This supposes an external Ceramic COG capacitor with a 50ppm/°C temperature coefficient

Parameter	Condition	Min	Typ	Max	Units
external capacitor					
Pulse time t_{pulse} range	C_{PULSE} from 15pF to 150pF	50		500	ns
Active Miller Clamping (AMC) Pre-driver					
AMC delay t_{AMC} for a given external capacitor	C_{AMC}=30pF[6]	**150**	200	**250**	ns
AMC delay range t_{AMC} range	C_{AMC} from 15pF to 220pF	100		1500	ns
FAULT/DESAT comparator					
Iref*RD22		**2.25**	2.5	**2.75**	V
Effective threshold range w/ respect to ND node for Normally On SiC JFET	Vp1 to NS, Vp2 to VSS; Programmable with external resistors RD11, RD12 with the equation of note [7]	**2.5**		**7.5**	V
Effective threshold range w/ respect to ND node for Normally Off SiC JFET	Vp1 to VSS, Vp2 floating; Programmable with external resistors RD11, RD12 with the equation of note [8]	**2.5**		**7.5**	V
VN max forced input current[9]				**10**	mA
VN max input leakage current		**-1**		**+1**	µA
Delay from VN to FAULT_DESAT output	IN=1 for t> t_{BLANK}, 500mV overdrive[10]		100		ns
Blanking time t_{BLANK} accuracy for fixed external capacitor	C_{BLANK}=300pF[11]	**3**	4	**5**	µs
Blanking time range	C_{BLANK} from 15pF to 600pF	0.2		8	µs
Delay t_{AL_DESAT} between FAULT_DESAT pulled down and OUTA forced to ZERO	In case of DESAT Fault event	100	200	300	ns
Hysteresis open-drain transistor (Vh input) ON-Resistance			1K		Ω
FAULT Outputs (FAULT_UVLO1, FAULT_UVLO2, FAULT_DESAT & FAULT_D_U)					
Open-drain transistor ON-Resistance		**40**	60	**120**	Ω

[6] This assumes an external Ceramic COG capacitor with a 50ppm/°C temperature coefficient

[7] Case Normally-On JFET: Vth_{ND}=(RDD11+RDD12)*(Iref*RD22)/RDD12 with the constraint of RDD11//RDD12=R'

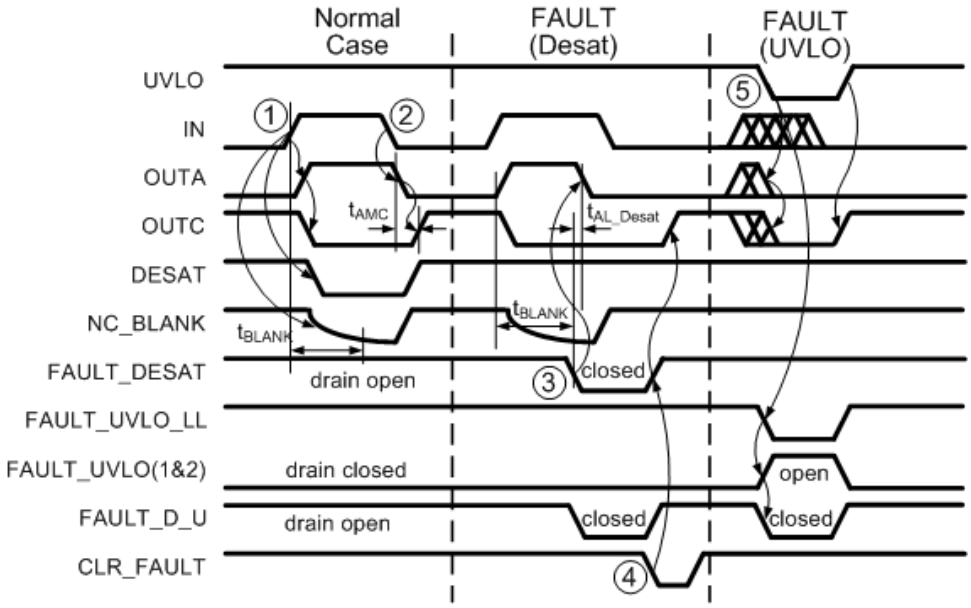
[8] Case Normally-Off JFET: Vth_{ND}=(RDD11+RDD12)*(Iref*RD22)/RDD12

[9] (Vref-Vn) is clamped to about 5V by current limiting diodes able to absorb 10mA

[10] This delay is obtained for a step from 2V to 3V with a rise time of 10ns at node VN, the effective threshold being set to 2.5V

[11] This assumes an external Ceramic COG capacitor with a 50ppm/°C temperature coefficient

Control Logic Timing Diagram



Main Events:

① Rising input 'IN' signal:

→ The output 'OUTA' rises up after a propagation delay

→ The output 'OUTC' falls down after a propagation delay

→ The output of the DESAT comparator falls down, as a consequence of the turn ON of the external power transistor

→ The node NC_BLANK discharges with a time constant $t_{BLANK}=R_{BLANK}*C_{BLANK}$. As the output of the DESAT comparator falls down before the end of the blanking time t_{BLANK}, no DESAT fault occurs and node FAULT_DESAT remains high (FAULT_DESAT is active LOW).

② Falling input 'IN' signal:

→ The output 'OUTA' fall down after a propagation delay

→ The output 'OUTC' rise up after a time constant $t_{AMC}=R_{AMC}*C_{AMC}$

→ The output of the DESAT comparator rises up, as a consequence of the turn OFF of the external power transistor

③ DESAT Fault Event: The output of the DESAT comparator doesn't fall down after a rising input 'IN' signal

→ After time constant t_{BLANK}, the output 'FAULT_DESAT' is forced to return to 0

→ After time constant ($t_{BLANK}+t_{AL\_DESAT}$), the output 'OUTA' is forced to return to 0

→ The output 'OUTC' is hold to 0 until the DESAT Fault clear (see ④)

④ CLEAR_FAULT signal is sent by the controller (negative pulse)

→ The internal DESAT fault state is cleared and FAULT_DESAT output rises up

→ The output 'OUTC' is released and goes to not(OUTA)

⑤ UVLO Fault Event: The output of the UVLO comparator falls down

→ The output 'OUTA' is forced to zero

→The output 'OUTC' is also forced to zero, aiming to put the external AMC transistor in high impedance (drain open)

→The output 'FAULT_UVLO_LL' fall down (FAULT_UVLO_LL is active LOW)

→Outputs 'FAULT_UVLO(1&2)' rise up (FAULT_UVLO(1&2) are active HIGH)

Typical Performance Characteristics (VCC-VSS = 15V)

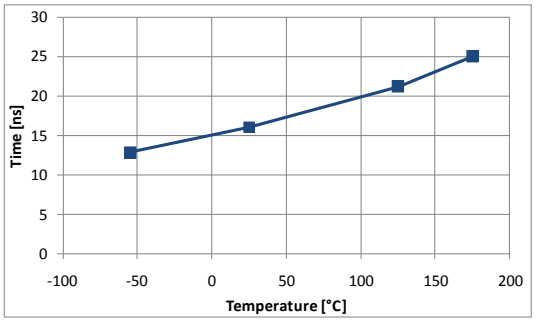


Figure 1. OUTA rise time vs. temperature.

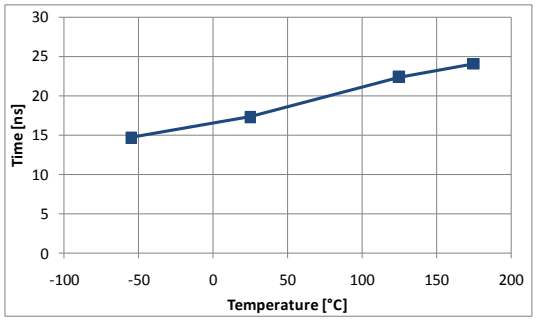


Figure 2. OUTA fall time vs. temperature.

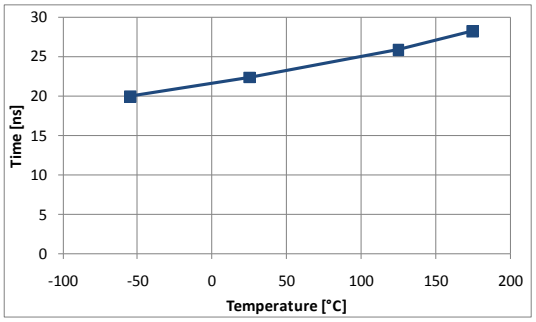


Figure 3. OUTA rising propagation delay vs. temperature.

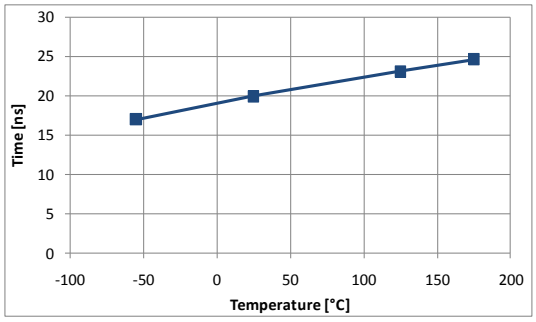


Figure 4 OUTA falling propagation delay vs. temperature.

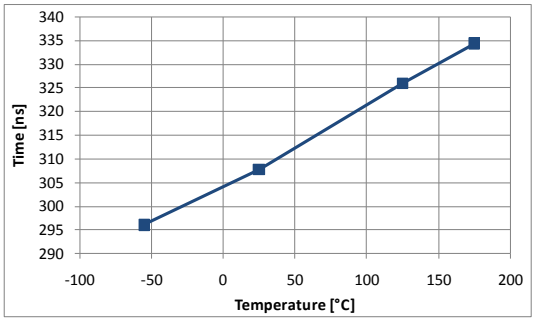


Figure 5. t_{PULSE} versus temperature (C_{PULSE}=100pF).

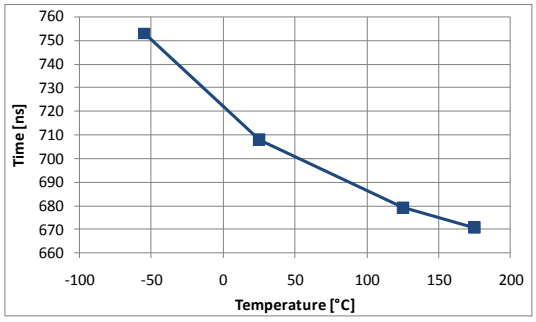


Figure 6. t_{AMC} versus temperature (C_{AMC}=100pF).

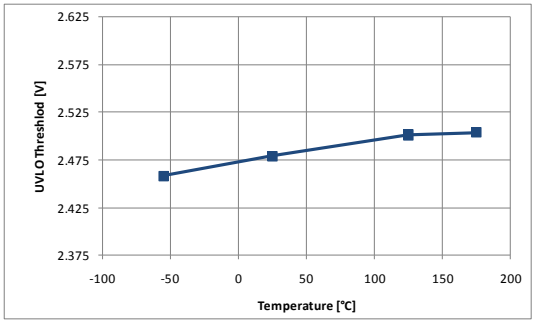


Figure 7. UVLO threshold versus temperature.

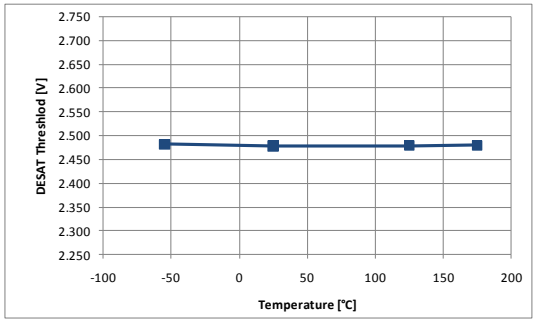


Figure 8. DESAT threshold versus temperature.

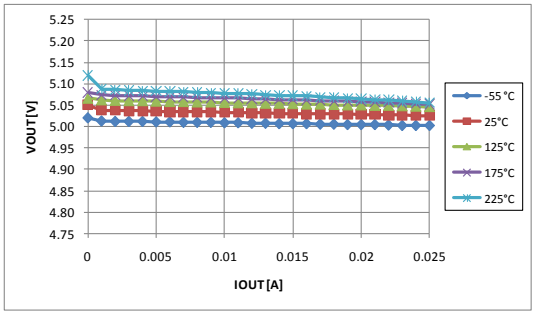


Figure 9. LDO load regulation (VCC_LDO= 15V)

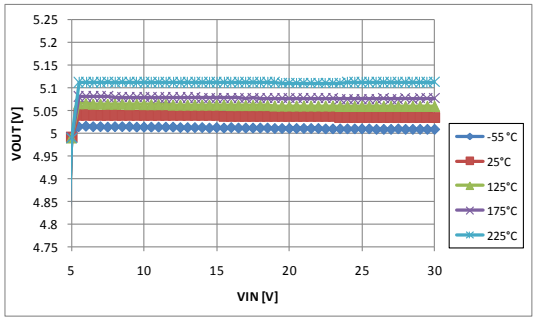


Figure 10. LDO line regulation (IOUT=0A)

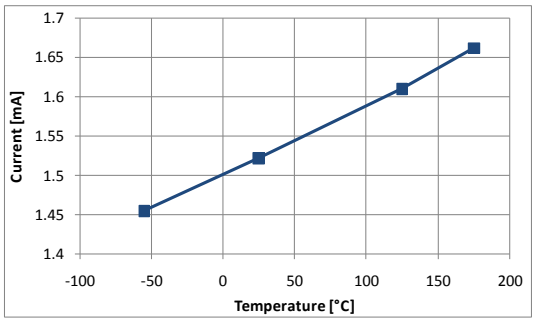
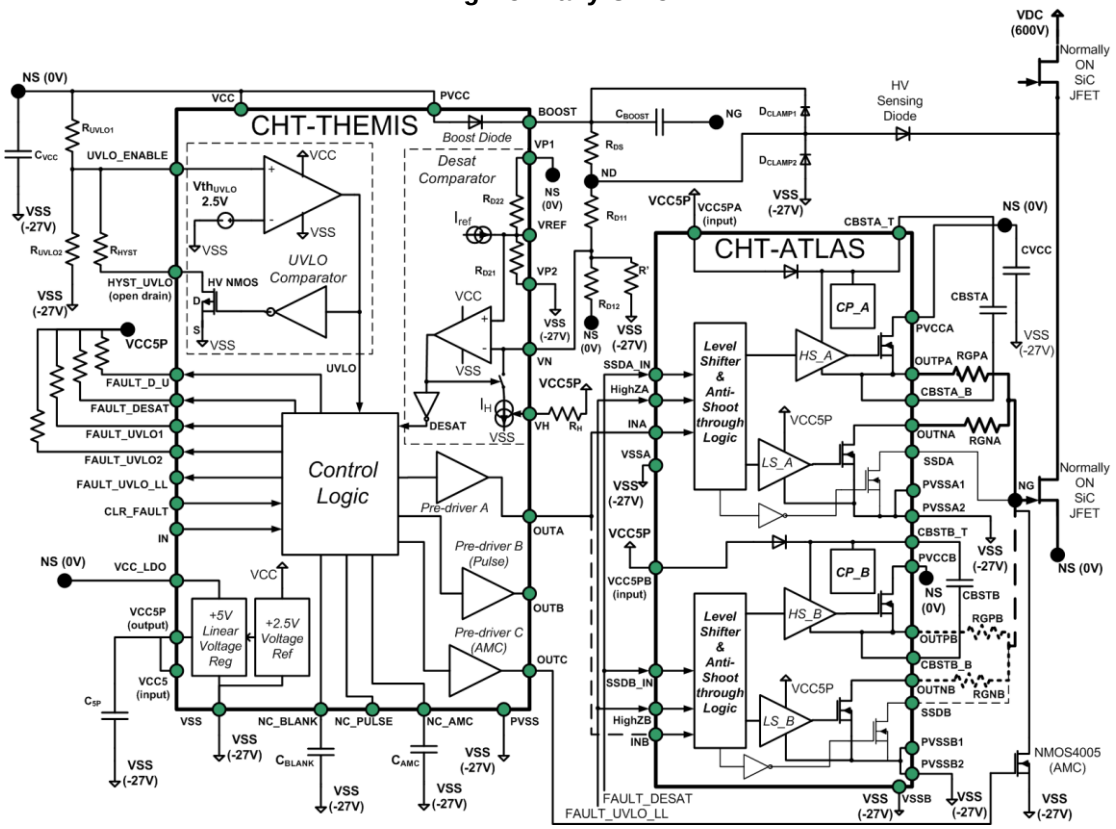


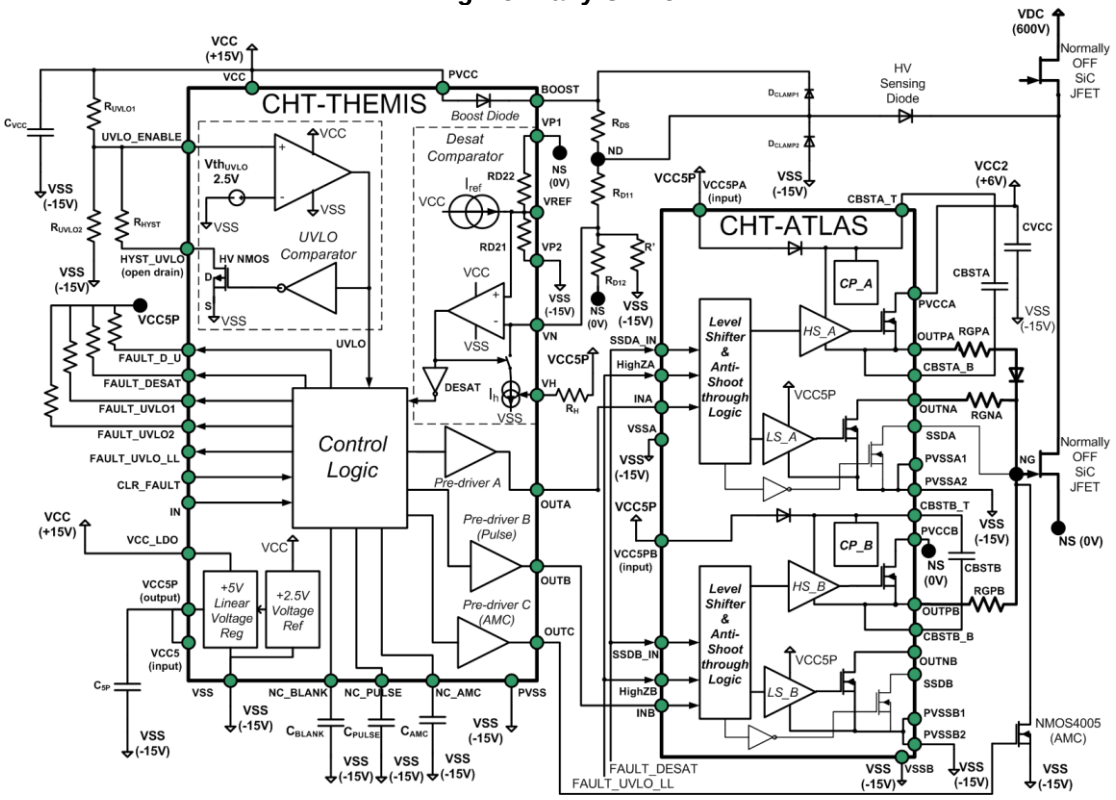
Figure 11. Quiescent current consumption vs. temperature (VCC, PVCC, VCC_LDO connected together)

Application diagrams

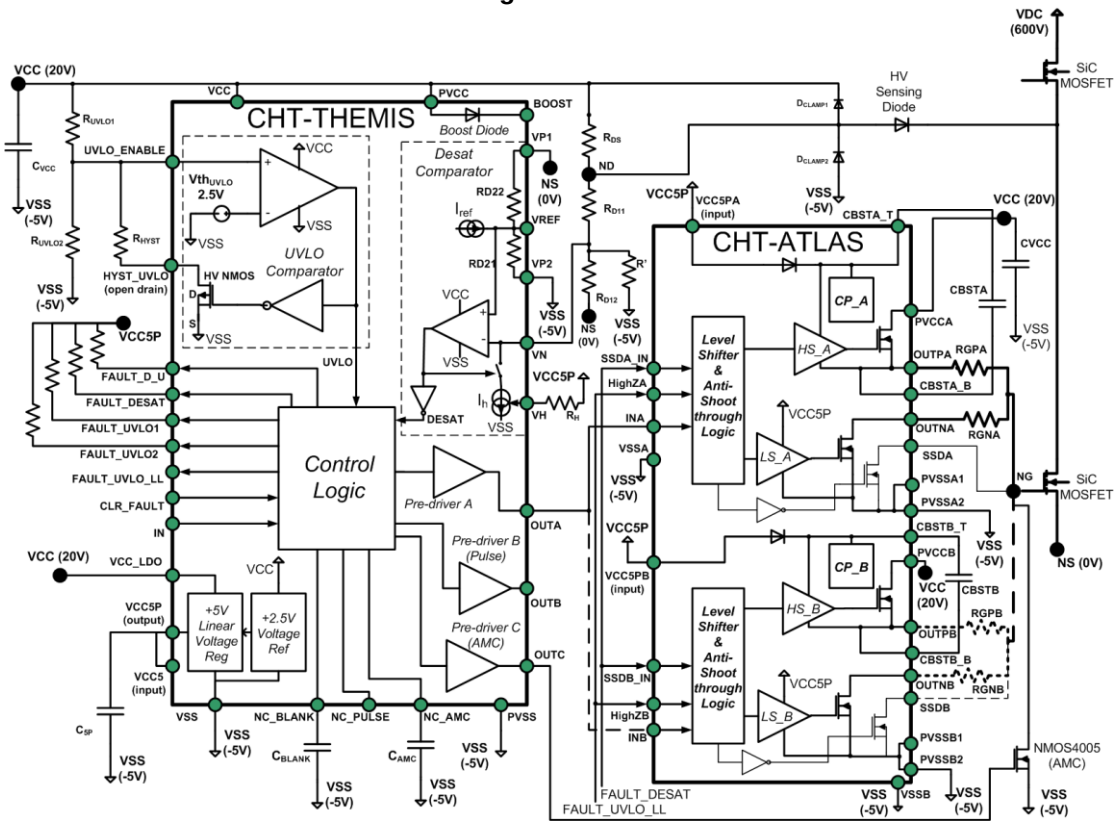
Driving Normally ON JFET



Driving Normally OFF JFET



Driving SiC MOSFET



General Description

CHT-THEMIS is the controller of the CHT-THEMIS / CHT-ATLAS chipset. The chipset is a high-temperature power switch driver specifically designed to drive Silicon Carbide (SiC) power transistors including normally-On and normally-Off JFETs, MOSFETs and BJTs. In this section, some of the different blocks shown in the Block Diagram section (page 2) are described and formulas are given for the selection of the external components for the typical applications presented in the last section.

Under Voltage Detection

The aim of this function is to allow the user to specify a threshold voltage for the power supply (VCC-VSS) under which the driver outputs (OUTA, OUTB, and OUTC) are pulled down to VSS and a fault is reported to the logic part of the system through the FAULT_UVLO_LL/FAULT_UVLO1/FAULT_UVLO2 outputs. For a given threshold voltage, noted V_{UVLO}, the R_{UVLO1} and R_{UVLO2} are obtained as follows:

- Choose R_{UVLO2} to satisfy (V_{UVLO}-VSS)/ R_{UVLO2} >> 3µA (leakage current on UVLO_ENABLE pin)
- Then, compute R_{UVLO1} with the desired V_{UVLO} using the following equation:

$$R_{UVLO1} = R_{UVLO2}\left(\frac{V_{UVLO}\text{-}VSS}{2.5}\text{-}1\right)$$

To avoid oscillation when (VCC-VSS) are close to the UVLO threshold, an adjustable hysteresis can be configured through the resistor R_{HYST} which value can be obtained as follows:

- The R_{HYST} must satisfy the condition R_{HYST} >> 1kΩ (R_{ON} of the hysteresis pool-down transistor)
- Then, compute R_{HYST} with the desired V_{HYST_UVLO} (see Figure 12 for the definition of V_{HYST_UVLO}):

$$R_{HYST} = \frac{2.5\text{-}VSS}{\frac{V_{HYST\_UVLO}}{R_{UVLO1}} - \left(\frac{1}{R_{UVLO1}} + \frac{1}{R_{UVLO2}}\right) * VSS}$$

Example: for VSS=0; V_{UVLO}=7.5V; V_{HYST_UVLO}=0.5V, and by choosing R_{UVLO2}=100kΩ we obtain: R_{UVLO1}=200kΩ and R_{HYST}=1MΩ

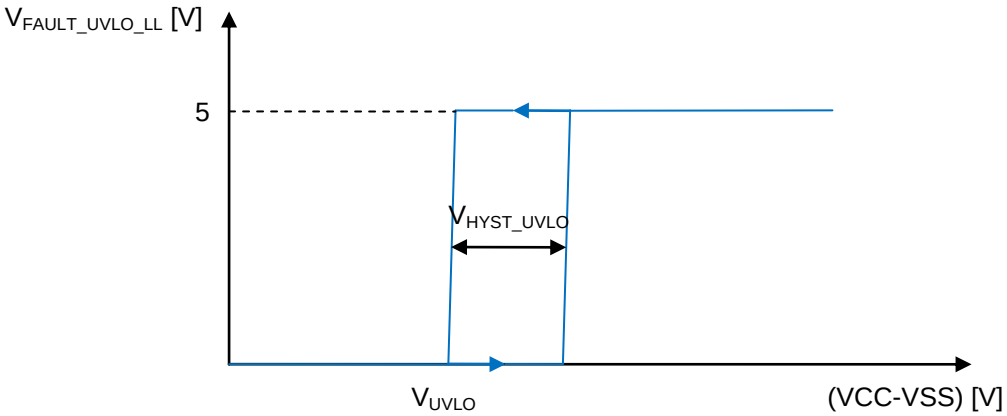


Figure 12. UVLO threshold and hysteresis definition.

De-saturation detection

The purpose of the DESAT function is to detect that the voltage at the drain of the power switch, in "ON" state, is lower than a given threshold (defined by external resistors R_{D11}, R_{D12}, and R'). This informs the logic part of the system about possible damage of the power switch through FAULT_DESAT output. The values of the external resistors R_{D11}, R_{D12} and R' can be obtained as follows:

- The value of R' must satisfy the following condition R'=RD11//RD12 to remove the VSS contribution from the de-saturation voltage sensing
- Then, compute R_{D11} and R_{D12} with the desired de-saturation threshold V_{DESAT} and a given value of R' (small enough to avoid VN leakage current < 10nA):

$$R_{D11}=\frac{R'*\left(V_{DESAT}+V_{SENSE\_DIODE}+V_{NS}\right)}{2.5+V_{NS}}$$

$$R_{D12}=\frac{R_{D11}*R'}{R_{D11}-R'}$$

To avoid oscillation when V_{DEASAT} is close to the de-saturation threshold, an adjustable hysteresis can be configured through the resistor R_H which value can be obtained as follows for a given de-saturation hysteresis V_{HYST_DESAT}:

$$R_H=R_{D11}*\frac{3.3}{V_{HYST\_DESAT}}$$

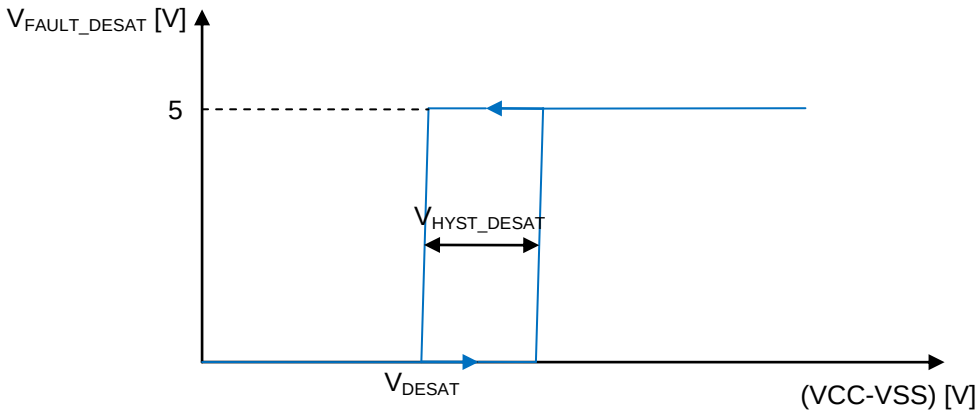


Figure 13. DESAT threshold and hysteresis definition.

At system level, the de-saturation detection should only be taken into account after a defined time following the low-to-high transition on "IN" input. This "blanking" time t_{BLANK} is adjusted by an external capacitor C_{BLANK} on the NC_BLANK pin and is used inside the Control Logic block to determine if a de-saturation took place or not. The t_{BLANK} delay must be higher than the de-saturation comparator delay and can be calculated using the following equation:

$$t_{BLANK}=13333 * C_{BLANK}$$

Example: for R'=100kΩ, V_{DESAT}=2V, V_{SENSE_DIODE}=1V, and V_{HYST_DESAT}=0.5V we obtain: R_{D11}=120kΩ, R_{D12}=600kΩ, and R_H=792kΩ.

Active Miller Clamping

The purpose of the Active Miller Clamping (AMC) feature is to avoid parasitic cross-conduction (positive kick on VGS) or punch-through (negative kick on VGS) during different switching phases in FET bridge arms (high/low side switches) in the context of power inverter application (see Figure 14).
Cross-conduction effect can happen with all types of FET devices while punch-through effect is more related to JFET devices.
These 2 effects are due to drain-to-gate coupling through the Miller capacitance of the FETs. They are further enhanced with the gate resistance which is necessary to kill the ringing effect due to parasitic inductances. The AMC provides a low impedance path, without series resistance, to maintain the gate voltage at its desired value to turn OFF the JFET properly with reduced risk of cross-conduction/punch-through. Figure 14 shows the cross-conduction and punch-through effects in a power inverter arm delivering positive current to an inductive load. In this case, the AMC feature in the low side driver provides a solution to significantly reduce the risk of cross-conduction/punch-through effects. Similarly, the same effects can be observed at the high side in the case of a power inverter arm delivering negative current.
For proper operation, the AMC delay (t_{AMC}) must be carefully adjusted and smaller than the non-overlapping delay between low and high side PWM inputs. This is made possible thanks to the external capacitor C_{AMC} which is related to t_{AMC} as:

$$t_{AMC}=6666 * C_{AMC}$$

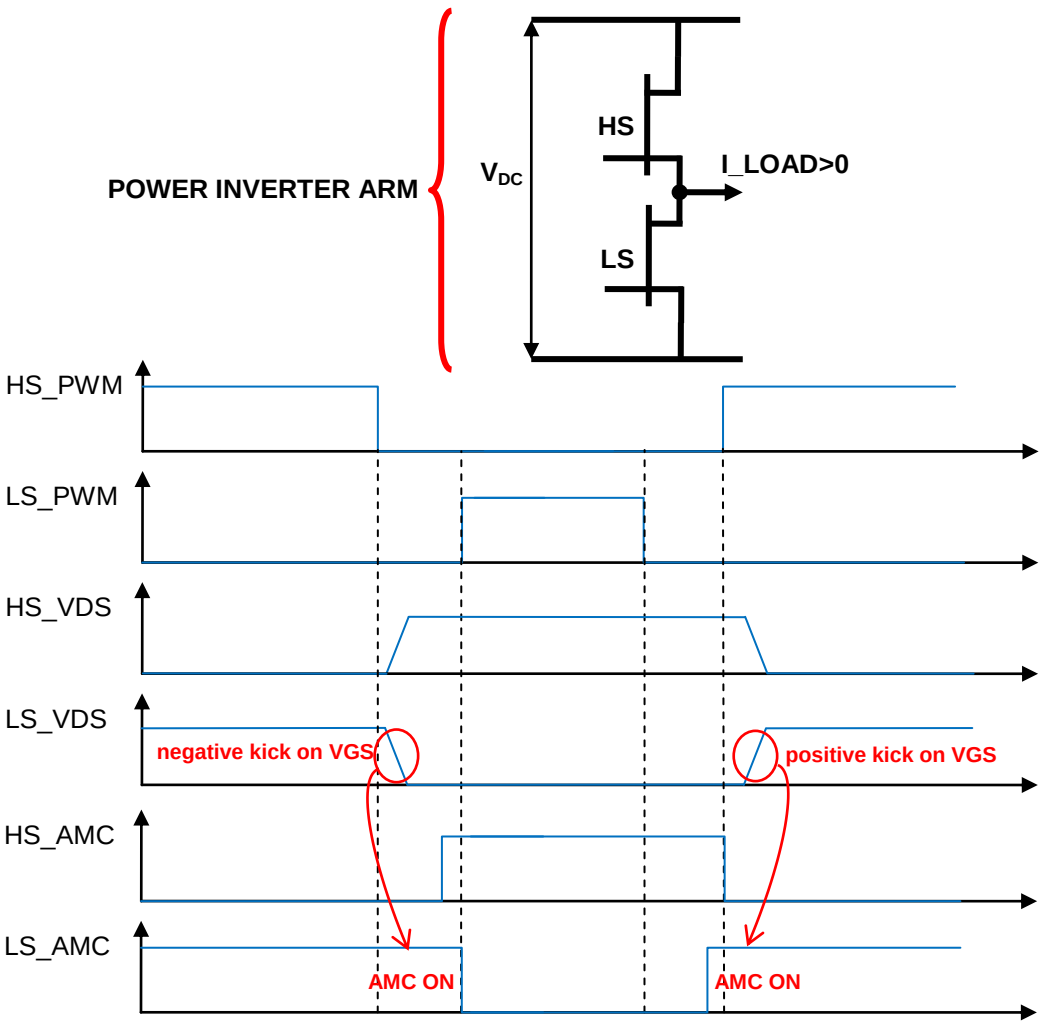


Figure 14. Cross-conduction and punch-through effects in a power inverter arm delivering positive current to an inductive load.

Support of Normally-Off devices

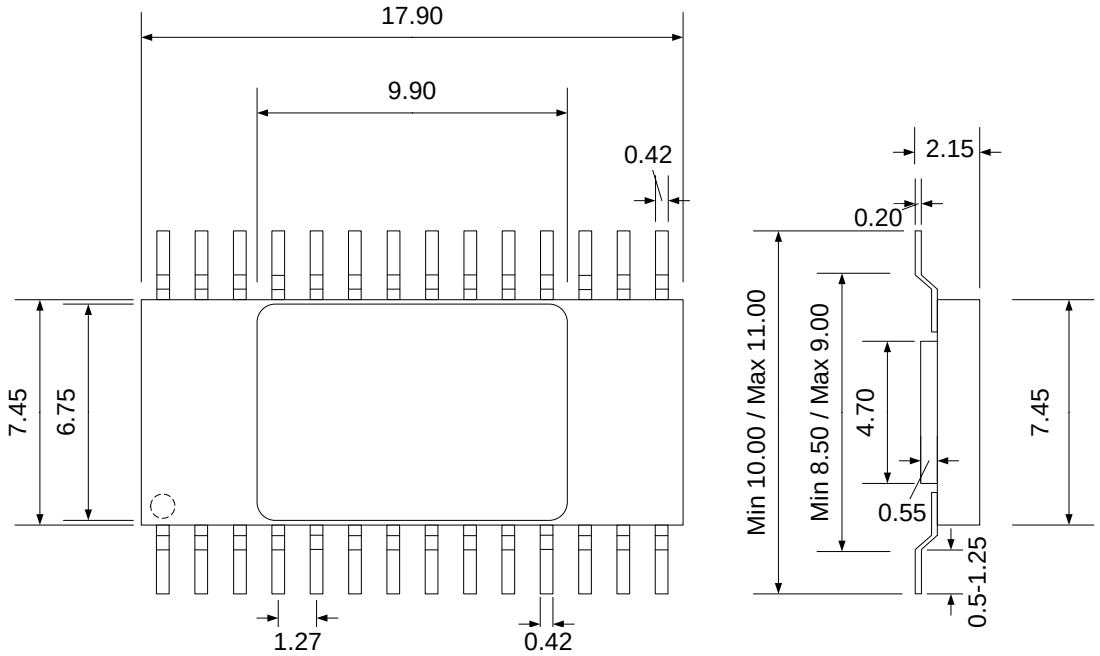
Unlike the normally-on JFET, the gate-source junction of the normally-off SiC JFET is forward biased in the device conduction state. In addition to the dynamic current for charging/discharging the total gate capacitance, some steady-state current has to be provided to maintain conduction after the device has been switched on.

The two channels of CHT-ATLAS can be combined to deliver both dynamic and steady-state currents (please refer to application diagrams).

Channel A must be driven with the regular PWM control signal (OUTA) while channel B must be driven by the second control signal (OUTB) giving a shorter impulse at the turn-on. The pulse width t_{PULSE} of this second control signal can be adjusted thanks to the external capacitor C_{PULSE} as:

$$t_{PULSE}=3333 * C_{PULSE}$$

Package Drawing



CSOIC 28 Drawing (mm +/- 10%)

Ordering Information

Ordering Reference	Package	Temperature Range	Marking
CHT-TIT9570C-CSOIC28-T	CSOIC28	-55°C to +225°C	CHT-TIT9570C

Contact & Ordering

CISSOID S.A.

Headquarters and contact EMEA:	CISSOID S.A. – Rue Francqui, 3 – 1435 Mont Saint Guibert - Belgium T : +32 10 48 92 10 - F: +32 10 88 98 75 Email: sales@cissoid.com
Sales Representatives:	**Visit our website: http://www.cissoid.com**

Disclaimer

Neither CISSOID, nor any of its directors, employees or affiliates make any representations or extend any warranties of any kind, either express or implied, including but not limited to warranties of merchantability, fitness for a particular purpose, and the absence of latent or other defects, whether or not discoverable. In no event shall CISSOID, its directors, employees and affiliates be liable for direct, indirect, special, incidental or consequential damages of any kind arising out of the use of its circuits and their documentation, even if they have been advised of the possibility of such a damage. The circuits are provided "as is". CISSOID has no obligation to provide maintenance, support, updates, or modifications.