High Temperature Industrial Adjustable, Linear Voltage Regulator +3.0V to +28V / 50mA CMT-STA4453- Preliminary Datasheet

Version: 1.0 (see note [1])

General description

CMT-STA4453 is a new linear voltage regulator designed and qualified for high-temperature industrial environments.

It is a high-temperature, high-reliability, 50mA adjustable linear voltage regulator suitable to generate from a +4.5V to +30V voltage source any regulated voltage in the range +3.0V to +28V. Its operating junction temperature ranges from -55°C to +175°C. The regulator is self-protected with a built-in current limiter and a thermal protection. CMT-STA4453 brings unique benefits in applications where the ambient or operating temperature is high and above the temperature supported by traditional semiconductors.

The IC features a chip-enable (CE active low) input signal allowing placing the circuit in low-power, disable mode.

The output voltage is adjustable by an external feedback resistor network.

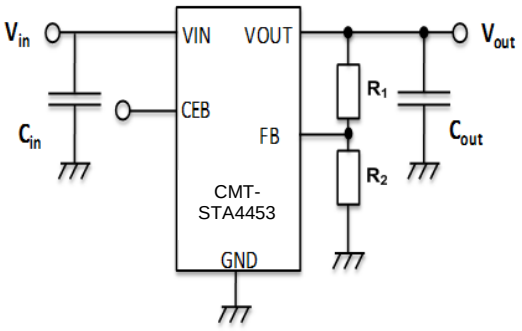
CMT-STA4453 is available in a tiny plastic package PSOIC8 with exposed pad for small PCB footprint and low thermal resistance.

Applications

Regulated power supplies for embedded electronics in industrial systems.

Features

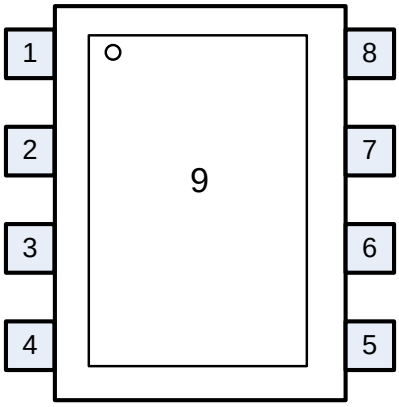
- Junction operating temperature from -55°C to 175°C
- Input voltage from 4.5V to 30V
- Output voltage: from 3.0V to 28V
- Output voltage total accuracy: ±5%[2]
- Output current: 50mA max
- Min voltage dropout @ 50mA: 0.7V
- Line regulation: -1% max
- Load regulation: -0.2% max
- C_{out}: min 1 µF
- Chip Enable
- Input ripple rejection: 65dB typ @ 100Hz
- Quiescent current: 1.1 mA typ.
- Stand-by current: 40 µA typ.
- Current limitation
- Latch-up free
- PSOIC8 Package with exposed pad



[1] Please always refer to the latest datasheet version available at http://www.cissoid.com/files/files/products/star/CMT-STA4453.pdf

[2] Excluding accuracy of external components
but including initial accuracy variation, temperature variation, line and load regulation variations

Pinout



Pin Number	Pin Name	Description
1	CEB	Chip Enable
2	GND	Negative power supply[3]
3	GND	Negative power supply3
4	OUT	Output voltage[4]
5	OUT	Output voltage4
6	VIN	Positive power supply[5]
7	VIN	Positive power supply5
8	FB	Feedback
9	VIN	Positive power supply[6]

[3] Pins 2 and 3 need to be connected at PCB level
[4] Pins 4 and 5 need to be connected at PCB level
[5] Pins 6 and 7 need to be connected at PCB level
[6] Exposed pad connection to PCB is only necessary if thermal design requires it

Absolute Maximum Ratings

Supply Voltage VIN to GND	-0.5 to 35V
Voltage on CEB and FB	max VIN
Peak output current	Internally limited
Junction Temperature (Tj)	185°C

ESD Rating

Human Body Model	>4kV

CAUTION: *Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Frequent or extended exposure to absolute maximum rating conditions or above may affect device reliability. Permanent uses of the device in short-circuit state or in over-temperature state may affect long term reliability of the device.*

Operating Conditions

Supply Voltage VIN to GND:	4.5V to 30V
Junction temperature	-55°C to +175°C
Continuous current	0 to 50 mA

Electrical Characteristics

Unless otherwise stated, T_j = 25°C, C_{in} = 4.7µF, C_{out}= 4.7µF . **Bold** figures point out values valid over the whole temperature range (T_j = -55°C to +175°C).

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Input Voltage	VIN		**4.5**		**30**	V
Output voltage range	VOUT	VIN = [4.5V-30V]	**3.0**		**28V**	V
Dropout[7]	D_r	Iout = 50mA	**0.7**		**25**	V
Output current	I_{out}		**0**		**50**	mA
Output voltage total accuracy		VIN =[4.5-30]V Iout = [0 .. 50]mA	**VOUT -5%**		**VOUT +5%**	V
Output voltage temperature drift		VIN= 5V; VOUT = 3.3V Iout = 0mA T_j = [25°C - 175°C]		+2.2		%
Output voltage line regulation		VIN =[4.5-30]V; VOUT = 3.3V Iout= 0mA			**-1**	%
Output voltage load regulation		VIN =5V; VOUT = 3.3V Iout = [0 .. 50]mA		**-0.06**[8]		%
		VIN =30V; VOUT = 27V Iout = [0 .. 50]mA		**-0.18**		
Quiescent current[9]	I_q	VIN= 5V; VOUT = 3.3V Iout = 0 mA		**1**		mA
		VIN= 30V; VOUT = 5V Iout = 0 mA		**1.15**		
Standby current[9]	I_{stdby}	VIN = 5V; T_j =175°C CEB = 5V		7		µA
		VIN = 30V; T_j = 175°C CEB = 5V		40		µA
Response to Line Transient		VIN from 5V to 10V (5V/µs) VOUT = 3.3V; Iout = 50mA		+5		%
		VIN from 10V to 5V (5V/µs) VOUT = 3.3V;Iout = 50mA		-5		%
		VIN from 5V to 6V (5V/µs) VOUT = 3.3V; Iout = 50mA		+1		%
		VIN from 6V to 5V (5V/µs) VOUT = 3.3V;Iout = 50mA		-1		%
Response to Load Transient		VIN = 10V; VOUT = 3.3V Iout from 10mA to 50 mA (10mA/µs), T_j = 175°C		-5		%
		VIN = 10V; VOUT = 3.3V Iout from 50 mA to 10 mA (10mA/µs), T_j = 175°C		+7		%
Power Supply Rejection Ratio (VIN=10V,VOUT=1.8V,Iout=10mA)	PSRR	100Hz		**65**		dB
		1 KHz		**45**		dB
Output noise voltage		BW = [1Hz .. 10KHz] VOUT=3.3V; T_j = 25°C		37		μV_{RMS}
Short-circuit current	Isc	VIN = [4.5-30]V	**110**	200	**260**	mA
FB input current	I_{FB}	VIN=10V; T_j = 175°C V_{FB} = 0.9V +/- 10%		50		nA
CEB input current	I_{CEB}	VIN = 5V; V_{CEB}=5V; T_j = 175°C		3		µA
CEB V_{IL}	$V_{IL\ CEB}$				**1.2**	V
CEB V_{IH}	$V_{IH\ CEB}$		**2**			V
Over temperature protection threshold	TH_{OTP}			TBD		°C
Over temperature protection hysteresis	$Hyst_{OTP}$			10		°C
Junction–to-case thermal resistance	$R_{\Theta JC}$			TBD		°C/W
Junction–to-ambient thermal resistance[10]	$R_{\Theta JA}$			55		°C/W

[7] Refer to Figure 11 for evolution of min dropout in function of required output current

[8] Load regulation measurements must be done in a way to avoid self-heating effect

[9] Current through feedback resistances excluded

[10] Based on FR4 2s2p board + thermal vias under the exposed pad

Typical Performance Characteristics at VOUT=5V

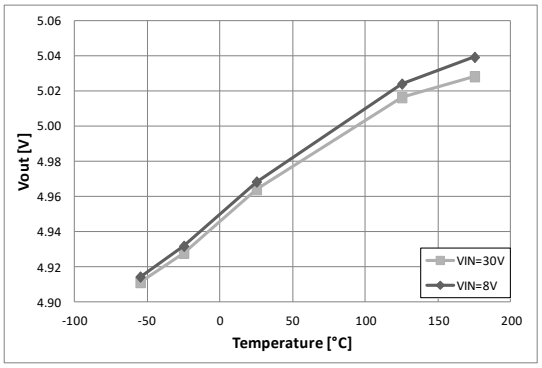


Figure 1: Output voltage temperature drift (Iout = 0 mA)

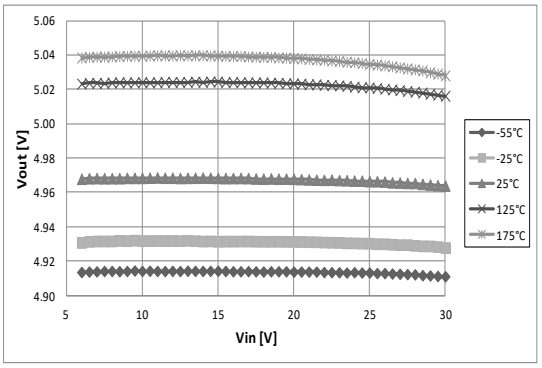


Figure 2: Output voltage line regulation (Iout = 0mA)

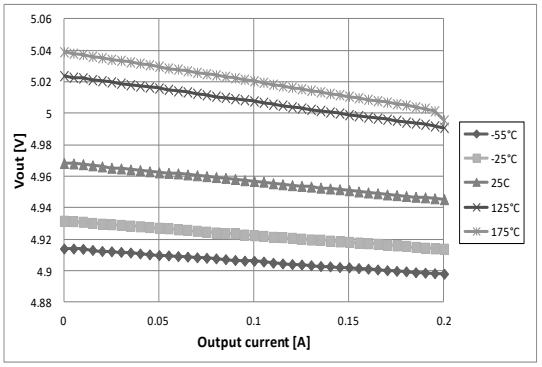


Figure 3: Output voltage load regulation (VIN = 7.5V)

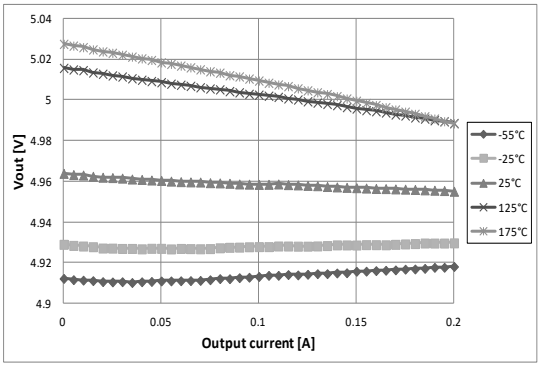


Figure 4: Output voltage load regulation (VIN = 30V)

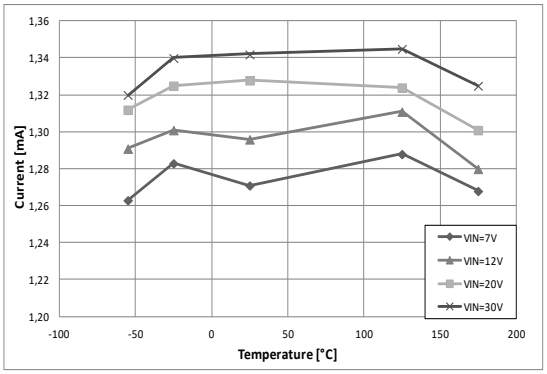


Figure 5: Quiescent current versus temp (Iout = 0 mA)

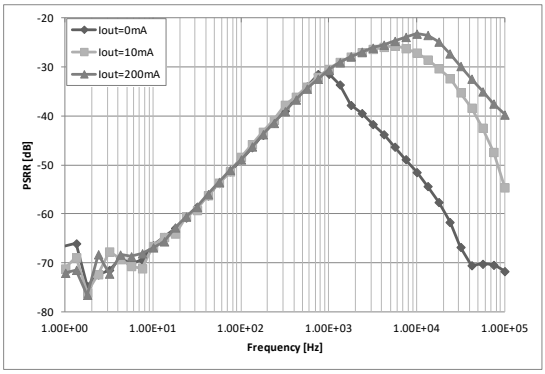


Figure 6: PSRR (VIN=10V, Cout= 4.7µF, Ta=25°C)

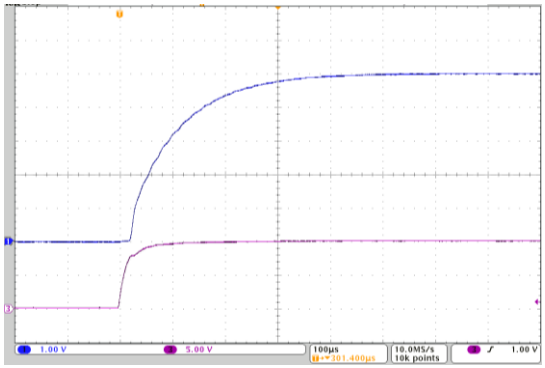


Figure 7: Start-up transient (VIN = 0 to 10V; Iout = 50mA,Ta = 175°C) (1:VOUT, 3:VIN)

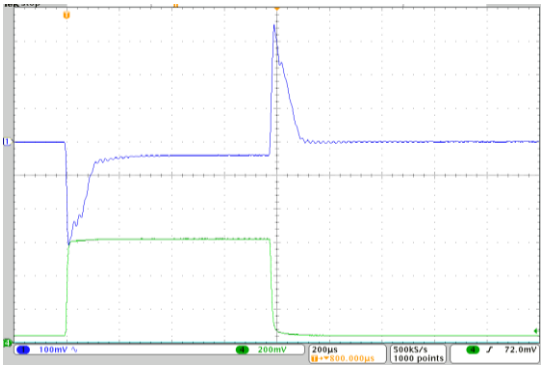


Figure 8: Response to load transient (10mA <-> 50 mA, 25mA/µs, VIN = 10V, Ta= 175°C, Cout = 4.7µF)

Typical Performance Characteristics (cnt'd)

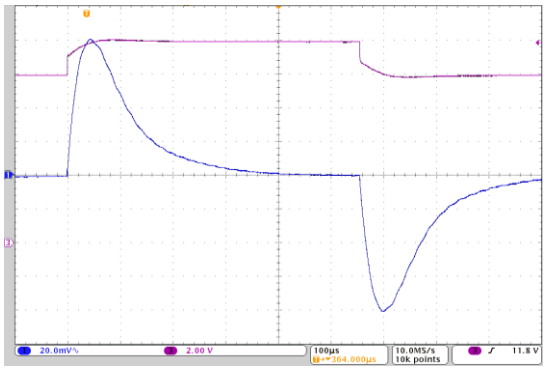


Figure 9: Response to line transient (Iout = 50 mA, VIN: 10 <-> 12V, 5V/µS, Ta= 175°C; Cout= 4.7µF) (1:VOUT AC, 3:VIN)

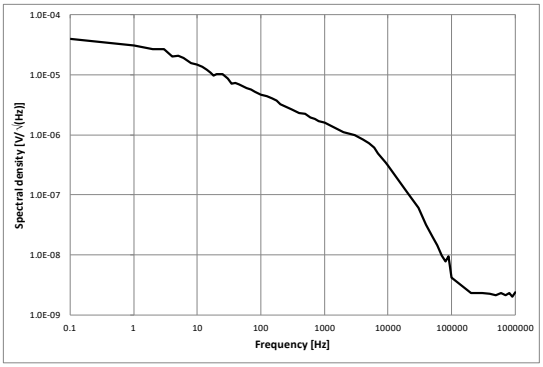


Figure 10: Output noise spectral density (VIN=8V, Iout= 0mA, Cout = 4.7 µF, Ta=25°C)

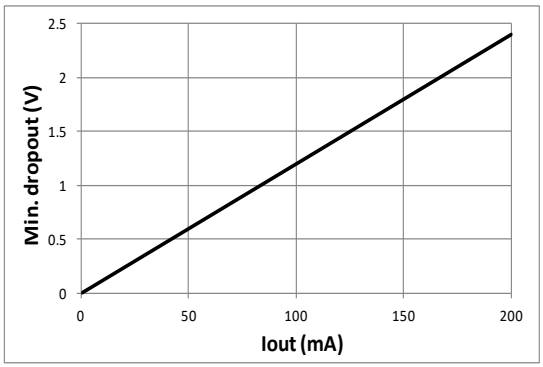


Figure 11: Dropout versus output current (Tj=175°C)

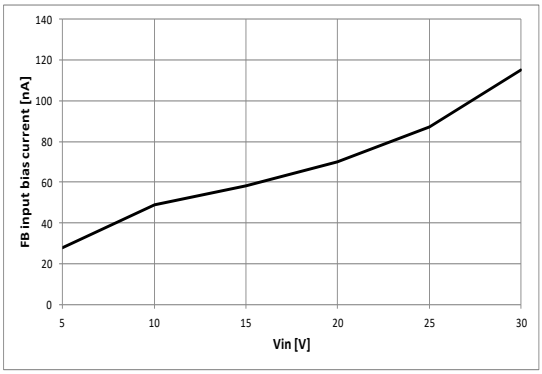


Figure 12: FB pin input leakage current (175°C)

Circuit Functionality

Safe operating area, power dissipation, and PCB layout considerations:

The tiny PSOIC8 package with exposed pad used for CMT-STA4453 requires adequate PCB layout in order to achieve efficient thermal dissipation, the minimization of the junction operating temperature, and maximizing the power dissipation taking advantage of the temperature behavior capability of CMT-STA4453.
The junction-to-air overall thermal resistance of CMT-STA4453 in PSOIC8 with exposed pad package relies, to a large extend, on the implementation of the copper mounting pads that act as a heatsink for the integrated circuit. The design must take into consideration the size of the copper pad and its placement on either of the board surfaces, or both.

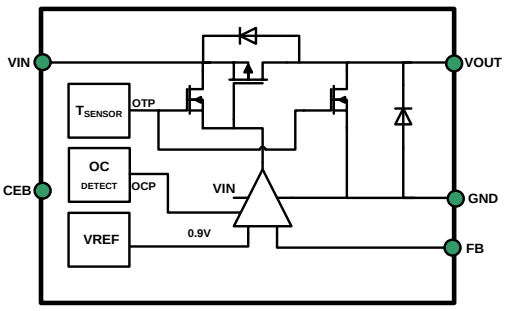
The maximum power dissipation is determined by the maximum junction temperature rating, the ambient temperature, and junction-to-ambient thermal resistance:

$$P_{DMAX} = (T_{JMAX} - T_A)/R_{\theta JA}$$

Where T_{JMAX}=175°C and $R_{\theta JA}=R_{\theta JC}+R_{\theta CA}$ with $R_{\theta JA}\cong$55°C/W (depends on the size of the copper mounting pad and thermal coupling to the PSOIC8 package with exposed pad[11]).

Contact Cissoid for getting access to reference PCB layout information.

Functional Block diagram



A PMOS transistor controls the level of current flowing from VIN to VOUT. An internal voltage reference of 0.9V (highly stable over the whole temperature range) provides the reference to which the voltage on the FB pin is compared. The internal amplifier drives the gate of the PMOS and regulates VOUT.
An on-chip temperature sensor with hysteresis monitors the die temperature; if this die temperature exceeds a predefined threshold, the PMOS transistor is disabled and VOUT is connected to GND.
In addition, an overcurrent protection circuit is implemented which limits gracefully the output current to a pre-defined value.

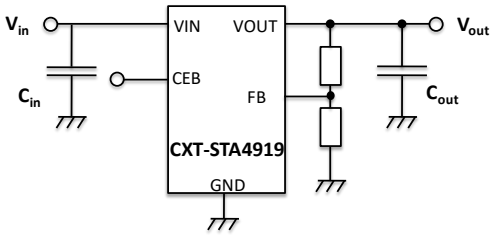
A Chip Enable function is provided thru the CEB pin: when tied low, the CMT-STA4453 is enabled and operates normally; when CEB is tied high, CMT-STA4453 is disabled. Note that the disable circuitry acts in the same way as the over-temperature disabling scheme as described above.

[11] More information available soon.

External resistances calculation rules

R1 and R2 values should be computed as follows:

$$\frac{R1+R2}{R2} = \frac{VOUT}{0.9V}$$



R1+R2 value should be lower than 200kΩ to limit the impact of the FB input leakage current. For VOUT = 0.9V, VOUT signal can be tied directly to FB pin.

Input and output capacitance

CMT-STA4453 requires an output capacitor connected between VOUT and GND to stabilize the internal control loop. The output capacitance value must be between 1 µF and 10 µF; ESR (equivalent series resistance) value should be between 0.01Ω and 1Ω.
Higher capacitor values offer improved behaviour in case of fast and high amplitude load transient.

There is no explicit requirement on the value of the input capacitance. Its size mainly depends on system aspects (impedance of the power source, distance between power source and CMT-STA4453, amount and speed of the load transients ...). CISSOID recommends the use of a 1 µF input capacitance.

CEB input

CEB input pin internal circuit is depicted in Figure 13.

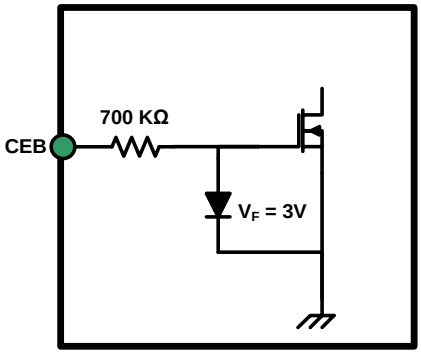


Figure 13

CEB threshold is set by the threshold of the transistor T1 (value between 1.2 and 2V).

It is expected that CEB pin will be driven by a controller and so that the CEB control signal voltage range will be typically between 0V and [3.3V-5V]; in this case, the leakage current through the CEB pin will 3 µA typ. over the whole temperature range.

Would the application use a larger voltage swing to control the CEB pin, system designers should take into account that CEB pin will present an additional equivalent resistance of about 700KΩ.

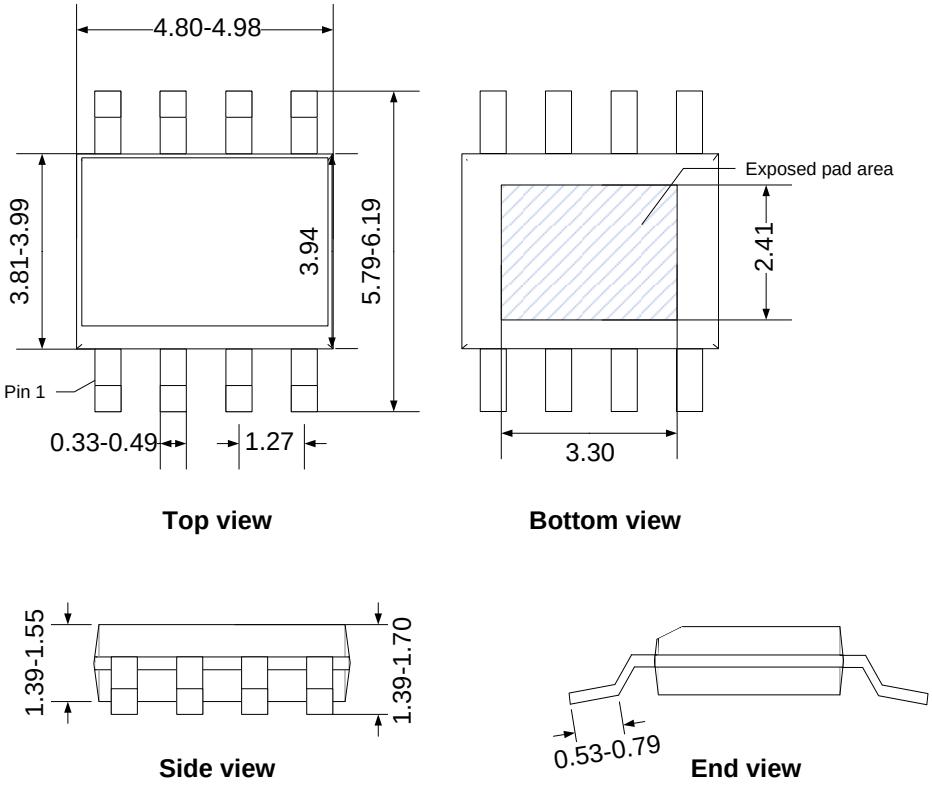
Current limit

In case the load connected to CMT-STA4453 would demand more than 50 mA current, the internal current limiter circuit will limit the maximum current delivered by CMT-STA4453 to 200mA (typical) whatever the output voltage.
If the output current exceeds the recommended 50mA and depending on the conditions (dropout, junction-2-air thermal resistance), the internal thermal protection could get activated and CMT-STA4453 would then switch between 2 modes:

- Thermal protection active; no output current
- Thermal protection not active; output current internally limited.

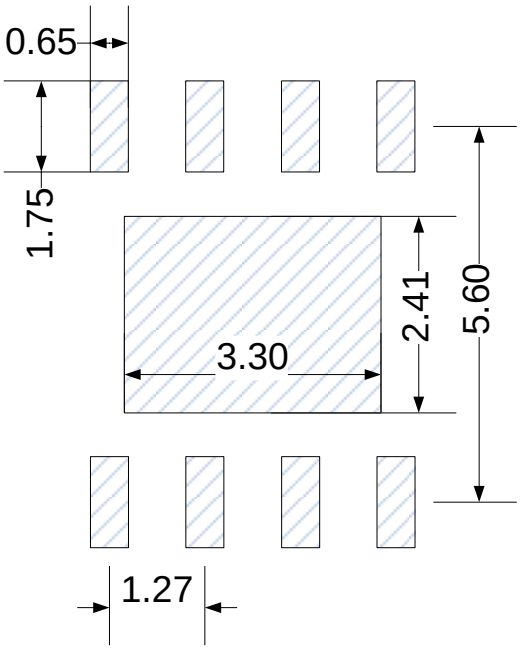
In case of short-circuit, both current limiter and thermal protection will be activated and will protect the device.

Package Dimension

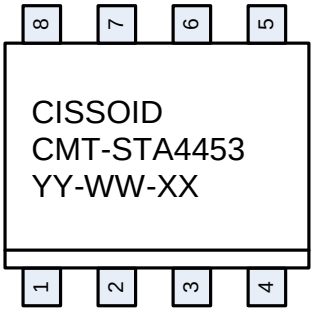


PSOIC8-EP physical dimensions (+/-0.2mm)

Suggested Pad Layout



Marking information



YY	Year (last 2 digits)
WW	Week (1 to 53)
XX	Assembly lot ID

Ordering Information

Product Name	Ordering Reference	Package	Marking
CMT-STA4453	**CMT-STA4453A-PSOIC8-EP**	**PSOIC8-EP**	**CMT-STA4453A**

Contact & Ordering

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