

CMT-VOLGA DATASHEET

Version: 1.1

High Temperature High-Speed, Rail-to-Rail Comparator

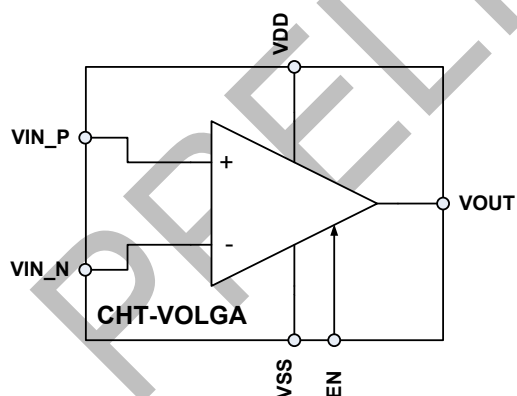
General description

The CMT-VOLGA is a single high-speed comparator with a normal operating temperature range -55°C to $+175^{\circ}\text{C}$.

The device operates from a single $+5\text{V}\pm 10\%$ power supply, with rail-to-rail input / output. CMT-VOLGA features a shutdown mode, controllable through an Enable digital input pin that places the device in a low power consumption mode when the comparator function is not needed. The comparator features an internal hysteresis (6mV Typ.) for improved noise immunity.

The output stage implements a push-pull CMOS stage, that can sink /or source up to 16mA.

The CMT-VOLGA is available in PSOIC8 surface mount package.

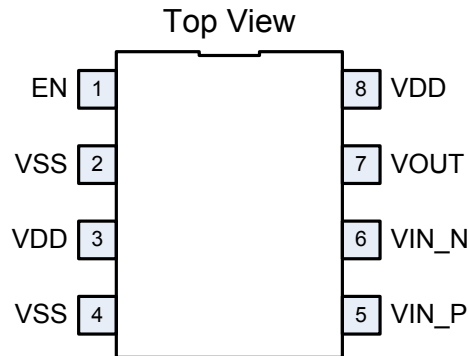


Features

- Rail to rail I/O
- Internal hysteresis: 6 mV Typ.
- Push-Pull CMOS output stage: $\pm 16\text{mA}$ Max
- Propagation delay: 29ns Typ. (with 20 mV overdrive)
- Shutdown current consumption:
 - 1 nA Typ. (25°C)
- Static current consumption:
 - 600 μA Typ. (@ 25°C)
 - 1.2 mA Typ. (@ 175°C)
- Maximum operating frequency:
 - 25 MHz Typ.
- Package:
 - PSOIC8
- Validated at 175°C for 1000 hours (and still on-going)

Applications

- Threshold detectors / discriminators
- Window comparators
- Zero-crossing detectors

Pinout: PSOIC8


Pin #	Pin Name	Pin Description
1	EN	Enable input signal (active high)
2	VSS	Negative power supply
3	VDD	Positive power supply
4	VSS	Negative power supply
5	VIN_P	Positive Input signal
6	VIN_N	Negative Input signal
7	VOUT	Comparator output signal
8	VDD	Positive power supply

Absolute Maximum Ratings

Supply Voltage V_{DD} to GND -0.5 to 6.0V
 Voltage on any Pin to GND -0.5 to $V_{DD}+0.3V$
 Junction temperature T_j 175°C

Operating Conditions

Supply Voltage V_{DD} to GND 4.5V to 5.5V
 Junction temperature -55°C to +175°C

ESD Rating

Human Body Model > 2000V

Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Frequent or extended exposure to absolute maximum rating conditions or above may affect device reliability.

Electrical Characteristics

Unless otherwise stated: $V_{DD}=5V$, $V_{SS}=0V$, $T_j=25^\circ C$. **Bold underlined** values indicate values over the whole temperature range ($-55^\circ C < T_j < +175^\circ C$).

Parameter	Condition	Min	Typ	Max	Units
Supply Voltage V_{DD}		4.5		5.5	V
Static Consumption Current I_{DD}	$T_j = 25^\circ C$ $T_j = -55$ to $175^\circ C$		600	812 <u>1712</u>	μA
Shutdown Quiescent Current I_{SHDN}	$T_j = 25^\circ C$ $T_j = 175^\circ C$		1 8		nA μA
Input Voltage Range V_{CM}^1		V_{SS}		V_{DD}	V
Input-Referred Trip Points V_{TRIP}		<u>± 1</u>	± 3	<u>± 12</u>	mV
Input-Referred Hysteresis V_{HYST}			6^2		mV
Input Offset Voltage V_{OS}	$V_{CM} = V_{SS}$ to V_{CC}			<u>5.2</u>	mV
Input Offset Drift TC_{VOS}			2.3		$\mu V/^\circ C$
Input Bias Current I_B	$T_j=175^\circ C$		30		nA
Input Offset Current I_{OS}	$T_j=175^\circ C$		20		nA
Common-Mode Rejection $CMRR^3$		<u>54</u>			dB
Power-Supply Rejection Ratio $PSRR^4$		<u>60</u>			dB
Input Capacitance C_{IN}			tbd		pF

¹ Only one of the inputs has to be within the common-mode limits to have a valid output.

² Trip Point is defined as the input voltage required to make the comparator output change state. The difference between upper (V_{TRIP+}) and lower (V_{TRIP-}) trip points is equal to the width of the input-referred hysteresis zone (V_{HYST})

³ $CMRR$ is defined as the change in offset voltage measured from $V_{CM}=0V$ to $V_{CM}=5V$ divided by 5V:
 $CMRR = (V_{OS,VCM=0} - V_{OS,VCM=5}) / 5$

⁴ $PSRR$ is defined as the change of the offset voltage measured from $V_{DD} = 4.5V$ to $V_{DD} = 5.5V$ divided by 1V: $PSRR = (V_{OS,VDD=4.5} - V_{OS,VDD=5.5}) / 1$

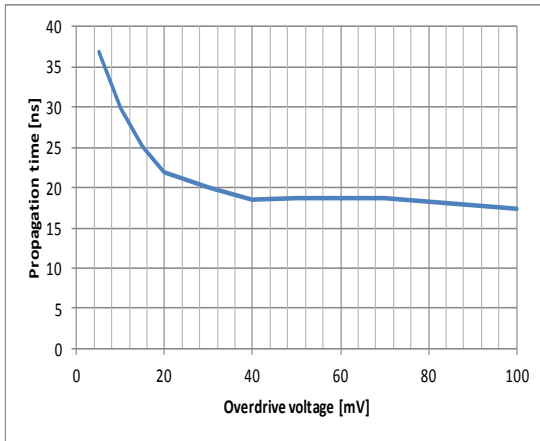
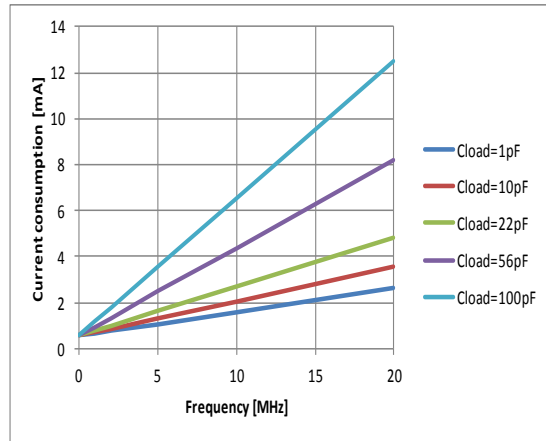
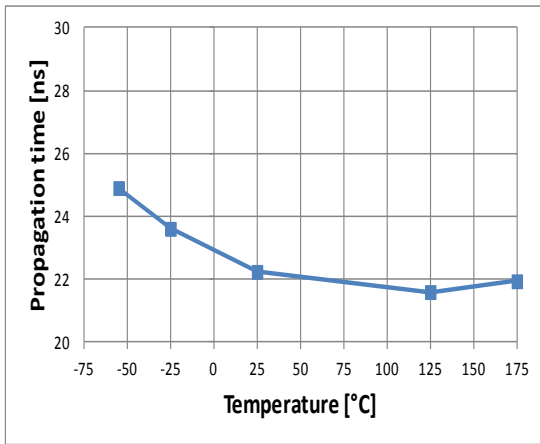
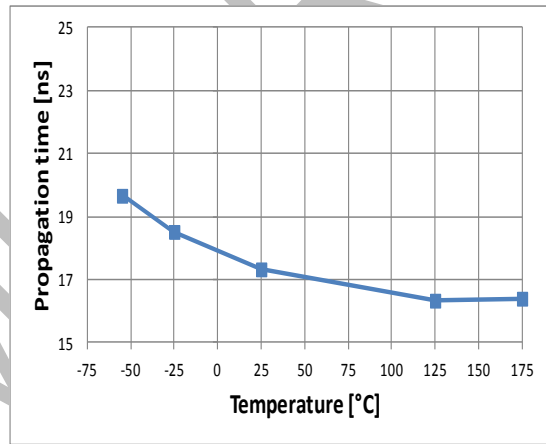
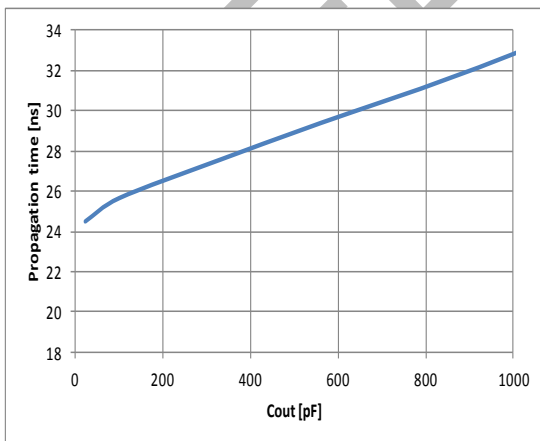
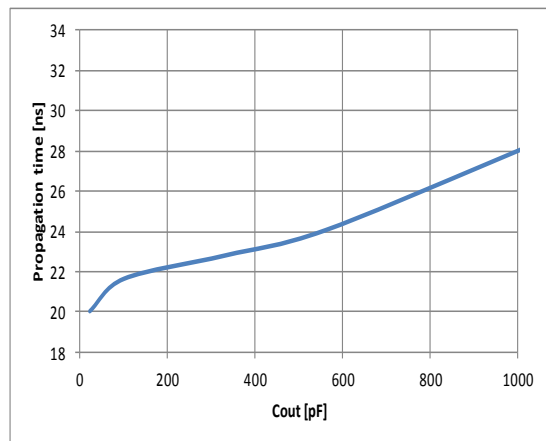
Electrical Characteristics (cnt'd)

Unless otherwise stated: $V_{DD}=5V$, $V_{SS}=0V$, $T_j=25^{\circ}C$. **Bold underlined** values indicate values over the whole temperature range ($-55^{\circ}C < T_j < +175^{\circ}C$).

Parameter	Condition	Min	Typ	Max	Units
Output High Voltage V_{OH}	$I_{SOURCE} = 16mA$	<u>4.6</u>	4.8		V
Output Low Voltage V_{OL}	$I_{SINK} = 16mA$		0.18	<u>0.37</u>	V
Propagation Delay Time t_{PD}	$V_{OV} = 20mV, C_{OUT} = 30pF$		29	<u>50</u>	ns
	$V_{OV} = 5mV, C_{OUT} = 30pF$		42		
Propagation Delay Skew ¹ t_{SKEW}	$V_{OV} = 20mV, C_{OUT} = 30pF$		1.5		ns
Rise Time ² t_R	$C_{OUT} = 30pF$		2		ns
Fall Time ² t_F	$C_{OUT} = 30pF$		2		ns
Disable Time t_{OFF}			50		ns
Enable Time t_{ON}			4		μs
EN Logic Input Low V_{IL}				<u>$V_{SS} + 1$</u>	V
EN Logic Input High V_{IH}		<u>$V_{DD} - 1$</u>			V
EN Input Bias Current $I_{B,EN}$				<u>35</u>	nA

¹ The difference between the propagation delay going high and the propagation delay going low

² Measured between 10% of VDD and 90% of VDD

Typical Performance Characteristics

Figure 1: Propagation delay vs overdrive voltage ($T_a = 25^\circ\text{C}$)

Figure 2: Current consumption vs frequency and load ($T_a = 25^\circ\text{C}$)

Figure 3: Propagation delay vs temperature (overdrive= 20mV)

Figure 4: Propagation delay vs temperature (overdrive= 100mV)

Figure 5: Propagation delay vs output capacitance (overdrive= 20mV, $T_a = 25^\circ\text{C}$)

Figure 6: Propagation delay vs output capacitance (overdrive= 100mV, $T_a = 25^\circ\text{C}$)

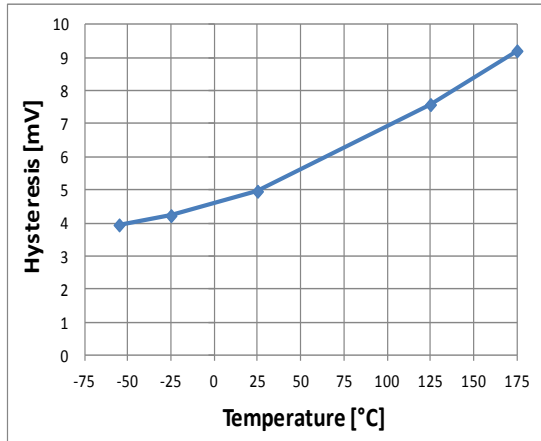


Figure 7: Hysteresis vs temperature

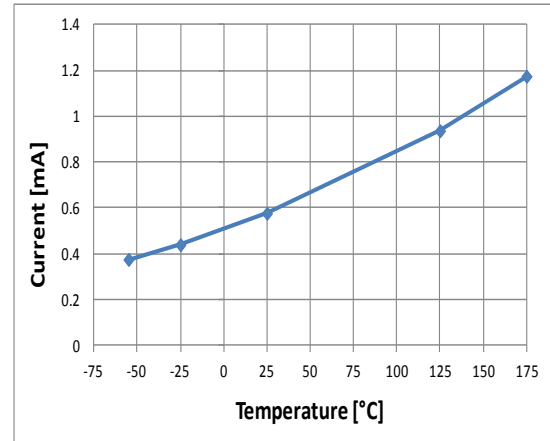


Figure 8: Static current vs temperature

Circuit Functionality

Shutdown

A device-enable pin (EN) allows the circuit to go in Idle state (very low current consumption). When the shutdown pin is low, the device draws 1 nA typ and the output is tied to ground.

If this feature is not required in the application, EN pin should be tied to the positive power supply VDD.

It takes a maximum of 4 μs time to come out of idle state.

Hysteresis

VOLGA features an internal hysteresis of 6 mV typical.

For applications with noisy or slow moving input signals, the comparator may display multiple switching when input difference is very small. In such applications, it might be desired to increase the noise immunity of the circuit. This can be achieved by implementing an external hysteresis through external resistors, as shown in Figure 9.

Total hysteresis is determined as follows:

$$V_{hyst} = \frac{V_{DD} * R1}{R1 + R2} + Int.Hyst.$$

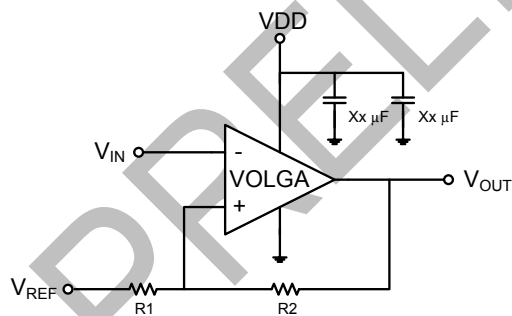


Figure 9

By increasing the hysteresis, sensitivity to noise (external noise, switching noise) is decreased.

Input overvoltage protection

VOLGA inputs are protected by ESD diodes; those will conduct if the input voltage exceeds power supply voltage by more than 500 mV.

If in the application, input voltage can exceed power supply voltage, an external current limit (set to 10 mA) should be implemented by adding a small resistance in serie with the comparator input as shown by Figure 10.

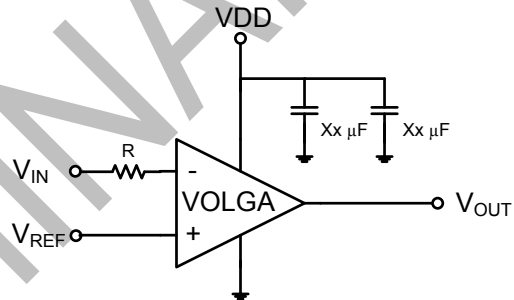


Figure 10

PCB Layout

For a high-speed comparator, proper design and printed circuit board (PCB) layout are key to get optimal performance.

To minimize the propagation delay of the complete circuit, it is essential to reduce as much as possible the resistance from the signal source and VOLGA input and as well the stray capacitance on the input (at PCB level).

Proper decoupling of the power supply is critical for reaching best VOLGA performance (mainly in applications where overdrive is very small). Recommendation is to work with a 2 stages decoupling:

- a 1 μ F to buffer the power supply line against ripple
- a 10nF to provide VOLGA with the required charges when switching (if the capacitance on the VOLGA output is larger than 30pF, the value of this decoupling capacitance should be increased).

Inputs (VIN_P, VIN_N) tracks should be as far as possible from the output (VOUT) to avoid coupling of the fast changing output into the high impedance inputs signals.

In a high-speed circuit, fast rising and falling switching transients create voltage differences across lines that would be at the same potential at DC. To reduce this effect, a ground plane should be used to reduce difference in voltage potential within the circuit board.

Figure 11 shows an example of optimized PCB layout for CMT-VOLGA:

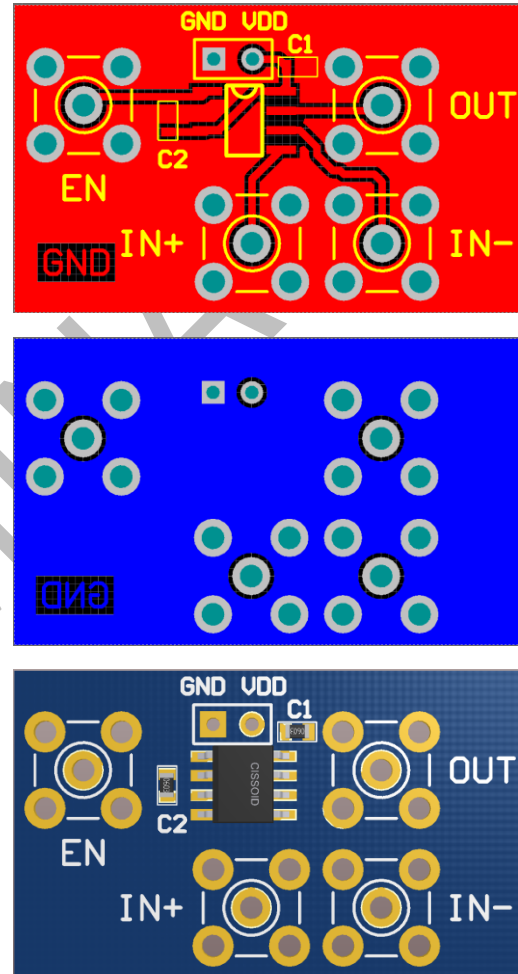
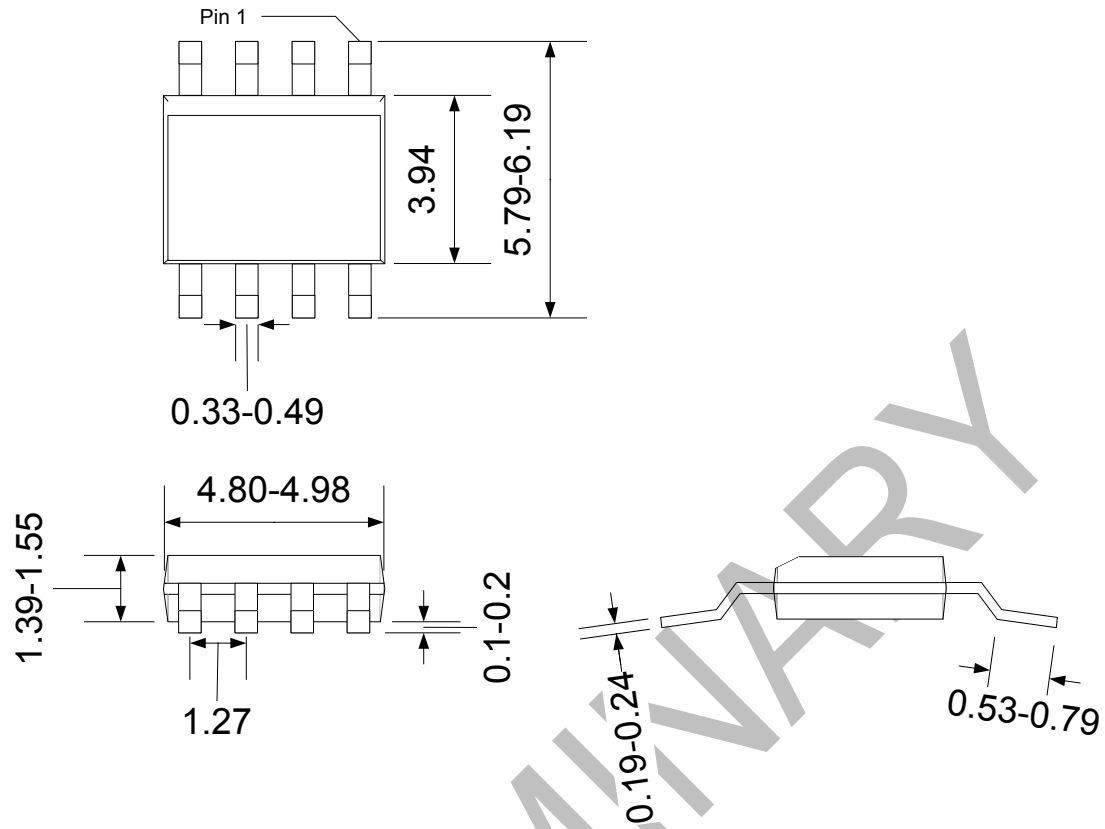


Figure 11

Package Dimensions


PSOIC8 physical dimensions (mm +/- 10%)

Ordering Information

Product Name	Ordering Reference	Package	Marking
CMT-VOLGA	CMT-RIV1675A-PSOIC8-T	PSOIC8	CMT-RIV1675A

Contact & Ordering

CISSOID S.A.

Headquarters and contact EMEA:	CISSOID S.A. – Rue Francqui, 3 – 1435 Mont Saint Guibert - Belgium T : +32 10 48 92 10 - F: +32 10 88 98 75 Email: sales@cissoid.com
Sales Representatives:	Visit our website: http://www.cissoid.com

PRELIMINARY

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