

CHT-74132 DATASHEET

Version: 3.7
8-Jul-14
(Last Modification Date)

High-Temperature, Quad 2-Input NAND Schmitt Trigger

General Description

The CHT-74132 contains four independent 2-input NAND gates with Schmitt Trigger, performing the Boolean function :

$$Y = \overline{A \cdot B}$$

The gate switches at different points for positive and negative going signals. The difference between the positive voltage V_{T+} and the negative voltage V_{T-} is defined as the hysteresis voltage V_H

The CHT-74132 can operate with supply voltages from 3.3 to 5V ($\pm 10\%$).

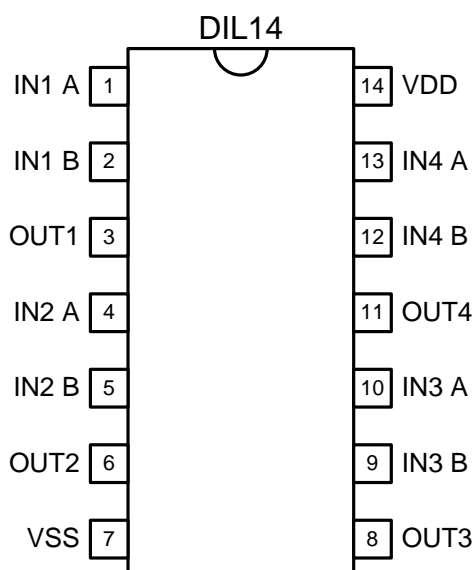
Features

- Qualified from -55 to +225°C (Tj)
- 3.3 to 5V ($\pm 10\%$) supply voltages
- Latchup-free at any supply and temperature condition
- Validated at 225°C for 30000 hours (CDIL14) and 20000 hours (CSOIC16) (and still on-going)
- Available in CDIL14 and CSOIC 16 hermetic standard package

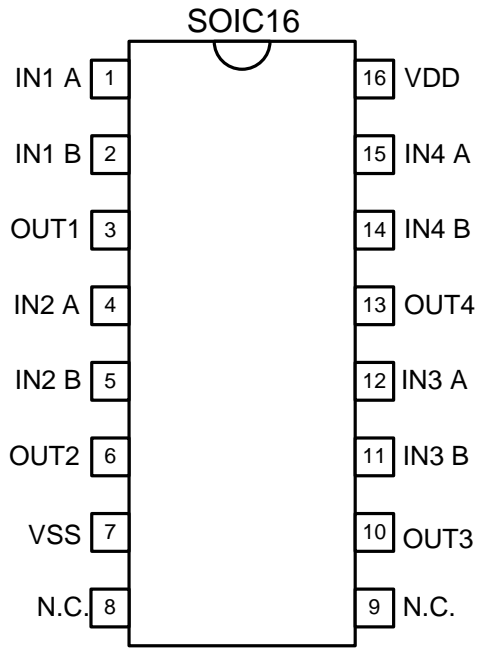
Applications

- High temperature logic
- Noise immunity function
- Sensor interface
- Signal processing/conditioning

Package and Pin Configuration



Pin	Symbol	Description
1	IN1 A	Input A of the NAND gate number 1
2	IN1 B	Input B of the NAND gate number 1
3	OUT1	Output of the NAND gate number 1
4	IN2 A	Input A of the NAND gate number 2
5	IN2 B	Input B of the NAND gate number 2
6	OUT2	Output of the NAND gate number 2
7	VSS	Circuit core ground terminal.
8	OUT3	Output of the NAND gate number 3
9	IN3 B	Input B of the NAND gate number 3
10	IN3 A	Input A of the NAND gate number 3
11	OUT4	Output of the NAND gate number 4
12	IN4 B	Input B of the NAND gate number 4
13	IN4 A	Input A of the NAND gate number 4
14	VDD	Circuit core power supply terminal.



Pin	Symbol	Description
1	IN1 A	Input A of the NAND gate number 1
2	IN1 B	Input B of the NAND gate number 1
3	OUT1	Output of the NAND gate number 1
4	IN2 A	Input A of the NAND gate number 2
5	IN2 B	Input B of the NAND gate number 2
6	OUT2	Output of the NAND gate number 2
7	VSS	Circuit core ground terminal.
8	NC	Not connected
9	NC	Not connected
10	OUT3	Output of the NAND gate number 3
11	IN3 B	Input B of the NAND gate number 3
12	IN3 A	Input A of the NAND gate number 3
13	OUT4	Output of the NAND gate number 4
14	IN4 B	Input B of the NAND gate number 4
15	IN4 A	Input A of the NAND gate number 4
16	VDD	Circuit core power supply terminal.

Function Table

INPUT		OUTPUT
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

Function and Logical Diagrams

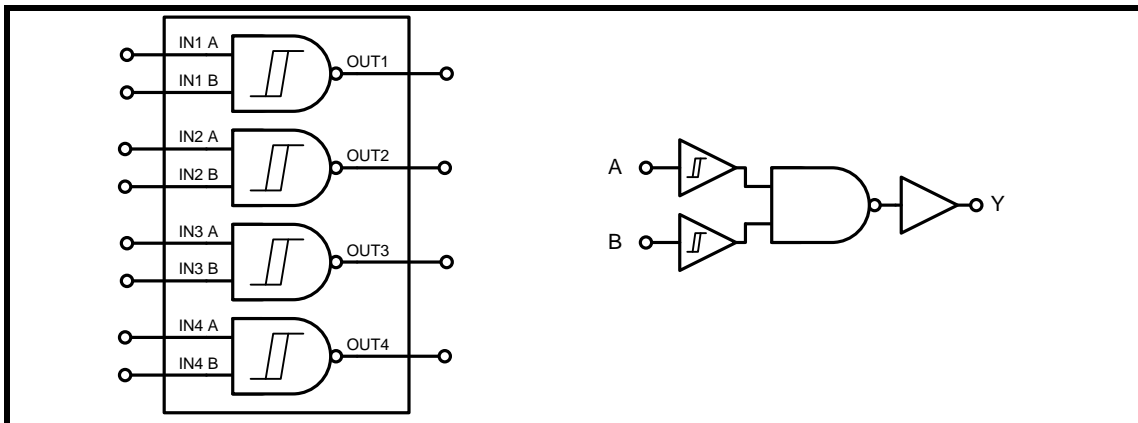


Figure 1. CHT-74132: simplified block diagram.

Absolute Maximum Ratings

 Supply Voltage V_{DD} to GND -0.5 to 5.5V
 Voltage on any Pin to GND -0.5 to $V_{DD}+0.5V$
Operating Conditions

 Supply Voltage V_{DD} to GND 3.3V to 5V ($\pm 10\%$)
 Junction temperature -55°C to +225°C

ESD Rating (expected)

Human Body Model >1kV

DC Electrical Characteristics

 Unless otherwise stated: $V_{DD}=5V$, $T_j=25^\circ C$. **Bold** figures indicate values valid over the whole temperature range ($-55^\circ C < T_j < +225^\circ C$).

Parameter	Condition	Min	Typ	Max	Units
Supply voltage V_{DD}			5V		V
Quiescent current I_{DD}	$T_j=-55^\circ C$		0.02		nA
	$T_j=225^\circ C$		1240		
Minimum HIGH level output voltage V_{OH}	$I_{OH}<4mA$ (source)	4.4			V
Maximum LOW level output voltage V_{OL}	$I_{OL}<4mA$ (sink)			0.63	V
Minimum HIGH level input voltage V_{T+}	$T_j=-55^\circ C$		3.30		V
	$T_j=25^\circ C$		3.30		
	$T_j=225^\circ C$		3.19		
Maximum LOW level input voltage V_{T-}	$T_j=-55^\circ C$		2.12		V
	$T_j=25^\circ C$		2.14		
	$T_j=225^\circ C$		2.18		
Hysteresis voltage V_H	$T_j=-55^\circ C$		1.18		V
	$T_j=25^\circ C$		1.16		
	$T_j=225^\circ C$		1.01		

DC Electrical Characteristics (cntd)

Unless otherwise stated: VDD=3.3V, T_j=25°C. **Bold** figures indicate values valid over the whole temperature range (-55°C < T_j < +225°C).

Parameter	Condition	Min	Typ	Max	Units
Supply voltage V _{DD}			3.3		V
Quiescent current I _{DD}	T _j =-55°C		0.015		nA
	T _j =225°C		940		
Minimum HIGH level output voltage V _{OH}	I _{OH} <2mA (source)	2.4			V
Maximum LOW level output voltage V _{OL}	I _{OL} <2mA (sink)			0.44	V
Minimum HIGH level input voltage V _{T+}	T _j =-55°C		2.28		V
	T _j =25°C		2.23		
	T _j =225°C		2.17		
Maximum LOW level input voltage V _{T-}	T _j =-55°C		1.23		V
	T _j =25°C		1.28		
	T _j =225°C		1.43		
Hysteresis voltage V _H	T _j =-55°C		1.05		V
	T _j =25°C		0.95		
	T _j =225°C		0.74		

AC Electrical Characteristics

Unless otherwise stated: $V_{DD}=5V$, $T_j=25^\circ C$. **Bold** figures indicate values valid over the whole temperature range ($-55^\circ C < T_j < +225^\circ C$).

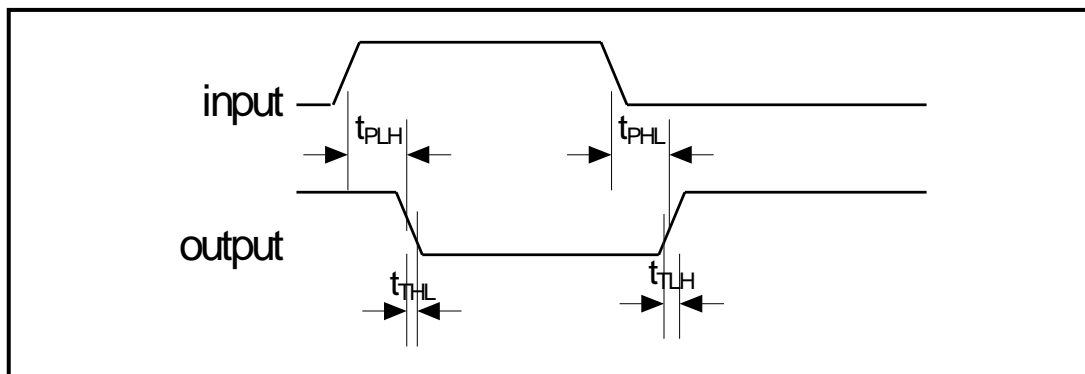
Parameter	Condition	Temperature	Min	Typ	Max	Units
Propagation delay time from A or B to Y ¹ t_{PHL}	$C_L=50pF$	$T_j=-55^\circ C$		8.8		ns
		$T_j=25^\circ C$		10.23		
		$T_j=225^\circ C$		13.68		
Propagation delay time from A or B to Y t_{PLH}	$C_L=50pF$	$T_j=-55^\circ C$		9.69		ns
		$T_j=25^\circ C$		11.42		
		$T_j=225^\circ C$		16.1		
Output transition time High to Low t_{THL}	$C_L=50pF$	$T_j=-55^\circ C$		8.17		ns
		$T_j=25^\circ C$		11.47		
		$T_j=225^\circ C$		16.39		
Output transition time Low to High t_{TLH}	$C_L=50pF$	$T_j=-55^\circ C$		9.92		ns
		$T_j=25^\circ C$		12		
		$T_j=225^\circ C$		15.4		

¹ Input A is 1% to 2% faster than input B.

AC Electrical Characteristics (cntd)

 Unless otherwise stated: $V_{DD}=3.3V$, $T_j=25^\circ C$. **Bold** figures indicate values valid over the whole temperature range ($-55^\circ C < T_j < +225^\circ C$).

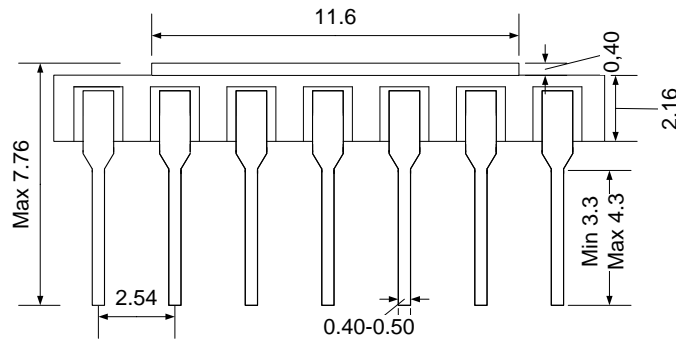
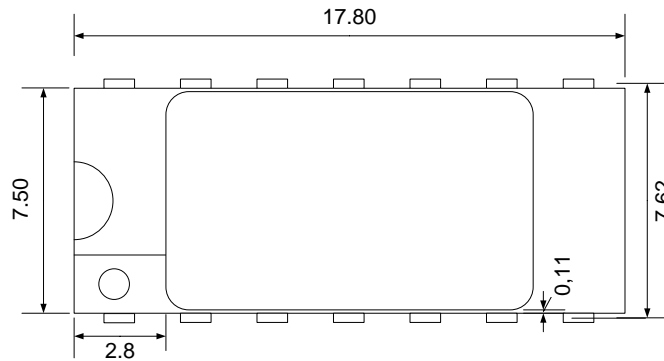
Parameter	Condition	Temperature	Min	Typ	Max	Units
Propagation delay time from A or B to Y t_{PHL}	$C_L=50pF$	$T_j=-55^\circ C$		13.81		ns
		$T_j=25^\circ C$		16.25		
		$T_j=225^\circ C$		21.14		
Propagation delay time from A or B to Y t_{PLH}	$C_L=50pF$	$T_j=-55^\circ C$		15.6		ns
		$T_j=25^\circ C$		19.3		
		$T_j=225^\circ C$		25.19		
Output transition time High to Low t_{THL}	$C_L=50pF$	$T_j=-55^\circ C$		14.04		ns
		$T_j=25^\circ C$		18.21		
		$T_j=225^\circ C$		23.46		
Output transition time Low to High t_{TLH}	$C_L=50pF$	$T_j=-55^\circ C$		13.78		ns
		$T_j=25^\circ C$		14.65		
		$T_j=225^\circ C$		21.3		

AC Waveforms

Figure 2. AC Waveforms

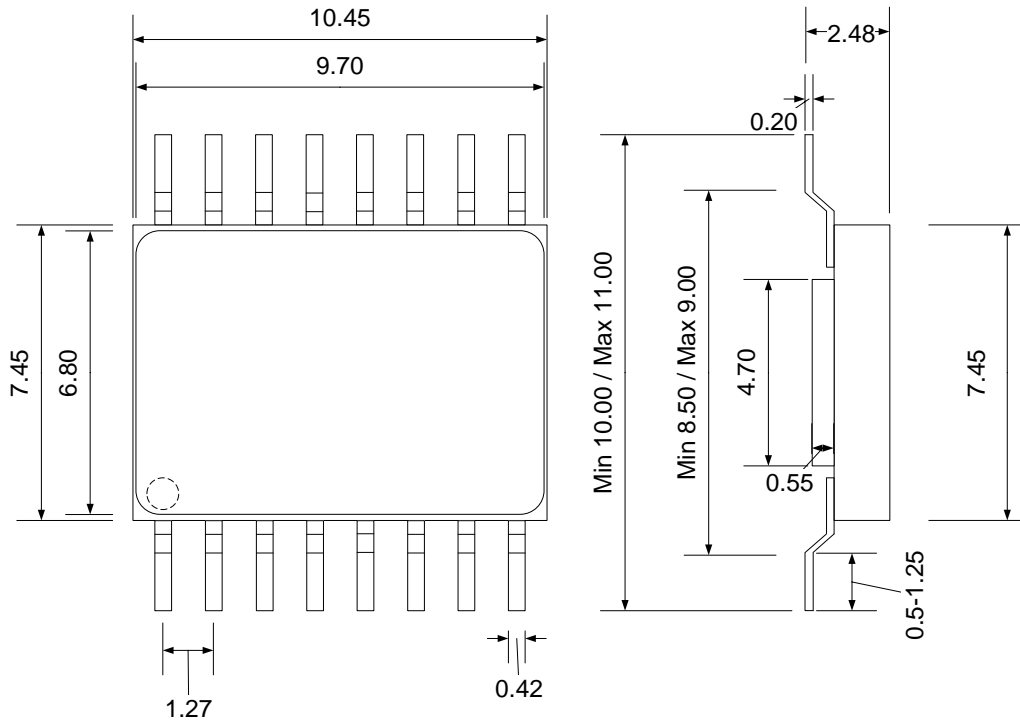
Ordering Information

Ordering Reference	Package	Temperature Range	Marking
CHT-74132-CDIL14-T	Ceramic DIL14	-55°C to +225°C	CHT-74132
CHT-74132-CSOIC16-T	Ceramic SOIC16	-55°C to +225°C	CHT-74132

Package Dimensions



Drawing CDIL14 (mm +/- 10%)



Drawing CSOIC16 (mm +/- 10%)

Contact & Ordering

CISSOID S.A.

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