CMT-7474 DATASHEET

Revision: 01.4
23-Dec-13
(Last Modified Date)

High-Temperature, Dual D-Flip-Flop

General Description

The CMT-7474 is a dual positive-edge-triggered D type Flip-flop. Data on the D input is transferred to the output on a rising edge of the clock impulse.

Rn and Sn are asynchronous reset and set. On a low state, they operate on the outputs regardless of the other inputs.

The CMT-7474 can operate with supply voltages from 3.3 to 5V (±10%).

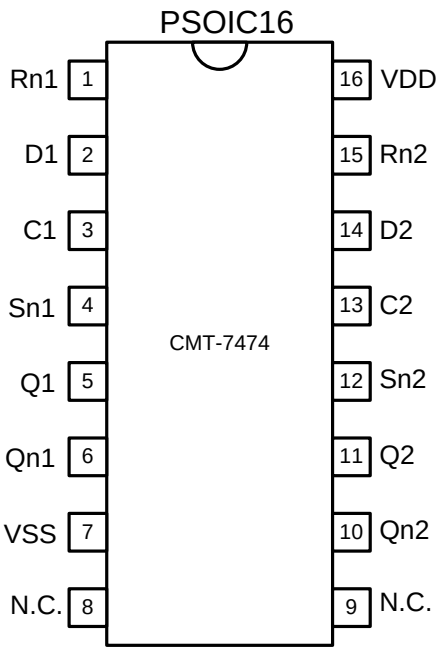
Features

- Qualified from -55 to +175°C (Tj)
- 3.3 to 5V (±10%) supply voltages
- Latchup-free at any supply and temperature condition
- Validated at 175°C for 20000 hours (and still on-going)
- Available in plastic SOIC16 standard package

Applications

- Well logging,
- Automotive, Aeronautics & Aerospace
- Harsh Environments

Package and Pin Configuration



Pin	Symbol	Description
1	**RN1**	Reset of D-flip-flop 1
2	**D1**	Input of D-flip-flop 1
3	**C1**	Clock pulse of D-flip-flop 1
4	**SN1**	Set of D-flip-flop 1
5	**Q1**	Output of D-flip-flop 1
6	**QN1**	Inverted output of D-flip-flop 1
7	**VSS**	Circuit core ground terminal.
8	**N.C.**	No connected terminal
9	**N.C.**	No connected terminal
10	**QN2**	Inverted output of D-flip-flop 2
11	**Q2**	Output of D-flip-flop 2
12	**SN2**	Set of D-flip-flop 2
13	**C2**	Clock pulse of D-flip-flop 2
14	**D2**	Input of D-flip-flop 2
15	**RN2**	Reset of D-flip-flop 2
16	**VDD**	Circuit core power supply terminal.

Function Table

INPUT				OUTPUT	
Sn	**Rn**	**C**	**D**	**Q**	**Qn**
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	L	X[1]
Sn	**Rn**	**C**	**D**	**Q(n+1)**	**Qn(n+1)**
H	H	↑	L	L	H
H	H	↑	H	H	L

[1] Having Sn=Rn=LOW at the same time should be avoided. The only known output is Q.

Logical Diagram

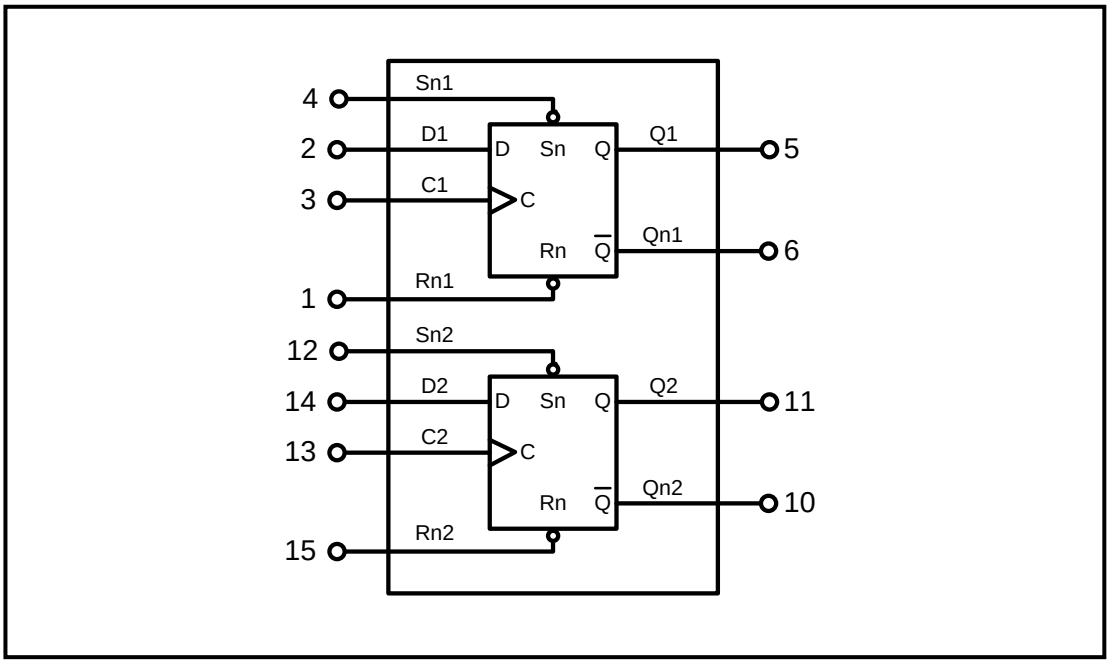


Figure 1. CMT-7474: simplified logical diagram.

Absolute Maximum Ratings

Supply Voltage V_{DD} to GND	-0.5 to 6.0V
Voltage on any Pin to GND	-0.5 to V_{DD}+0.5V

ESD Rating (expected)

Human Body Model	1kV

Operating Conditions

Supply Voltage V_{DD} to GND	3.3V to 5V (±10%)
Junction temperature	-55°C to +175°C

DC Electrical Characteristics

Unless otherwise stated: T_j=25°C. **Bold underlined** figures indicate values valid over the whole temperature range (-55°C < T_j < +175°C).

Parameter	Condition	Min	Typ	Max	Units
Supply voltage **V_{DD}**		3.3	5V		V
Quiescent current **I_{DD}**	V_{DD} = 3.3V, T_j=-55°C			4	nA
	V_{DD} = 5V, T_j=-55°C			6	
	V_{DD} = 3.3V, T_j=175°C			**438**	
	V_{DD} = 5V, T_j=175°C			**538**	
Minimum HIGH level output voltage **V_{OH}**	V_{DD} = 3.3V, I_{OH}<2mA (source)	**2.46**			V
	V_{DD} = 5V, I_{OH}<4mA (source)	**4.47**			
Maximum LOW level output voltage **V_{OL}**	V_{DD} = 3.3V, I_{OL}<2mA (sink)			**0.41**	V
	V_{DD} = 5V, I_{OL}<4mA (sink)			**0.59**	
Minimum HIGH level input voltage **V_{IH}**	V_{DD} = 3.3V	**2.2**			V
	V_{DD} = 5V	**3.3**			
Maximum LOW level input voltage **V_{IL}**	V_{DD} = 3.3V			**1.5**	V
	V_{DD} = 5V			**2.2**	

AC Electrical Characteristics

Unless otherwise stated: VDD=5V, T_j=25°C. **Bold underlined** figures indicate values valid over the whole temperature range (-55°C < T_j < +175°C).

Parameter	Condition	Temperature	Min	Typ	Max	Units
Propagation delay time from D to Y t_{PHL}	C_L=50pF	T_j=-55°C		10	13.6	ns
		T_j=25°C		15.2	20.4	
		T_j=175°C		14	18.8	
Propagation delay time from Rn to Y t_{PHL}	C_L=50pF	T_j=-55°C		9.3	12.9	ns
		T_j=25°C		15.1	20.2	
		T_j=175°C		13.8	18.4	
Propagation delay time from D to Y t_{PLH}	C_L=50pF	T_j=-55°C		5.6	8	ns
		T_j=25°C		8.6	12.4	
		T_j=175°C		8	11.4	
Propagation delay time from Sn to Y t_{PLH}	C_L=50pF	T_j=-55°C		12	517	ns
		T_j=25°C		18.4	26.6	
		T_j=175°C		16.8	24.4	
Output transition time High to Low t_{THL}	C_L=50pF	T_j=-55°C		6.7	9.1	ns
		T_j=25°C		10.7	15.1	
		T_j=175°C		9.8	13.6	
Output transition time Low to High t_{TLH}	C_L=50pF	T_j=-55°C		8.2	11.2	ns
		T_j=25°C		12.5	17	
		T_j=175°C		11	15.5	
Clock pulse width t_w	C_L=50pF	T_j=-55°C	3	1		ns
		T_j=25°C	3	1		
		T_j=175°C	4	2		
Set or reset pulse width t_w	C_L=50pF	T_j=-55°C	3	2		ns
		T_j=25°C	3	3		
		T_j=175°C	4	4		
Removal time set or reset t_{rem}	C_L=50pF	T_j=-55°C	0	0		ns
		T_j=25°C	0	0		
		T_j=175°C	0	0		
Set-up time D to C t_{su}	C_L=50pF	T_j=-55°C	1	1		ns
		T_j=25°C	2	1		
		T_j=175°C	2	2		
Hold time C to D t_h	C_L=50pF	T_j=-55°C	0	0		ns
		T_j=25°C	0	0		
		T_j=175°C	0	0		
Maximum clock pulse frequency f_{max}	C_L=50pF	T_j=-55°C	100	121		MHz
		T_j=25°C	73	100		
		T_j=175°C	55	75		

AC Electrical Characteristics (cntd)

Unless otherwise stated: VDD=3.3V, T_j=25°C. **Bold underlined** figures indicate values valid over the whole temperature range (-55°C < T_j < +175°C).

Parameter	Condition	Temperature	Min	Typ	Max	Units
Propagation delay time from D to Y t_{PHL}	C_L=50pF	T_j=-55°C		16.2	26	ns
		T_j=25°C		19.4	31.4	
		T_j=175°C		25	40.5	
Propagation delay time from Rn to Y t_{PHL}	C_L=50pF	T_j=-55°C		15	23.8	ns
		T_j=25°C		18	28.8	
		T_j=175°C		23.2	37	
Propagation delay time from D to Y t_{PLH}	C_L=50pF	T_j=-55°C		15.7	25.5	ns
		T_j=25°C		19.2	31.2	
		T_j=175°C		24.8	40	
Propagation delay time from Sn to Y t_{PLH}	C_L=50pF	T_j=-55°C		18.8	30.8	ns
		T_j=25°C		23.1	37.5	
		T_j=175°C		29.8	48.5	
Output transition time High to Low t_{THL}	C_L=50pF	T_j=-55°C		11.1	17.4	ns
		T_j=25°C		13.2	21.1	
		T_j=175°C		18	28	
Output transition time Low to High t_{TLH}	C_L=50pF	T_j=-55°C		10.7	16.7	ns
		T_j=25°C		13.3	20.5	
		T_j=175°C		17	26.8	
Clock pulse width t_w	C_L=50pF	T_j=-55°C	3	2		ns
		T_j=25°C	4	2		
		T_j=175°C	6	4		
Set or reset pulse width t_w	C_L=50pF	T_j=-55°C	3	3		ns
		T_j=25°C	5	3		
		T_j=175°C	7	5		
Removal time set or reset t_{rem}	C_L=50pF	T_j=-55°C	0	0		ns
		T_j=25°C	1	0		
		T_j=175°C	1	0		
Set-up time D to C t_{su}	C_L=50pF	T_j=-55°C	2	2		ns
		T_j=25°C	3	2		
		T_j=175°C	4	3		
Hold time C to D t_h	C_L=50pF	T_j=-55°C	0	0		ns
		T_j=25°C	1	0		
		T_j=175°C	1	0		
Maximum clock pulse frequency f_{max}	C_L=50pF	T_j=-55°C	38	62	95	MHz
		T_j=25°C	32	51		
		T_j=175°C	25	40		

AC Waveforms

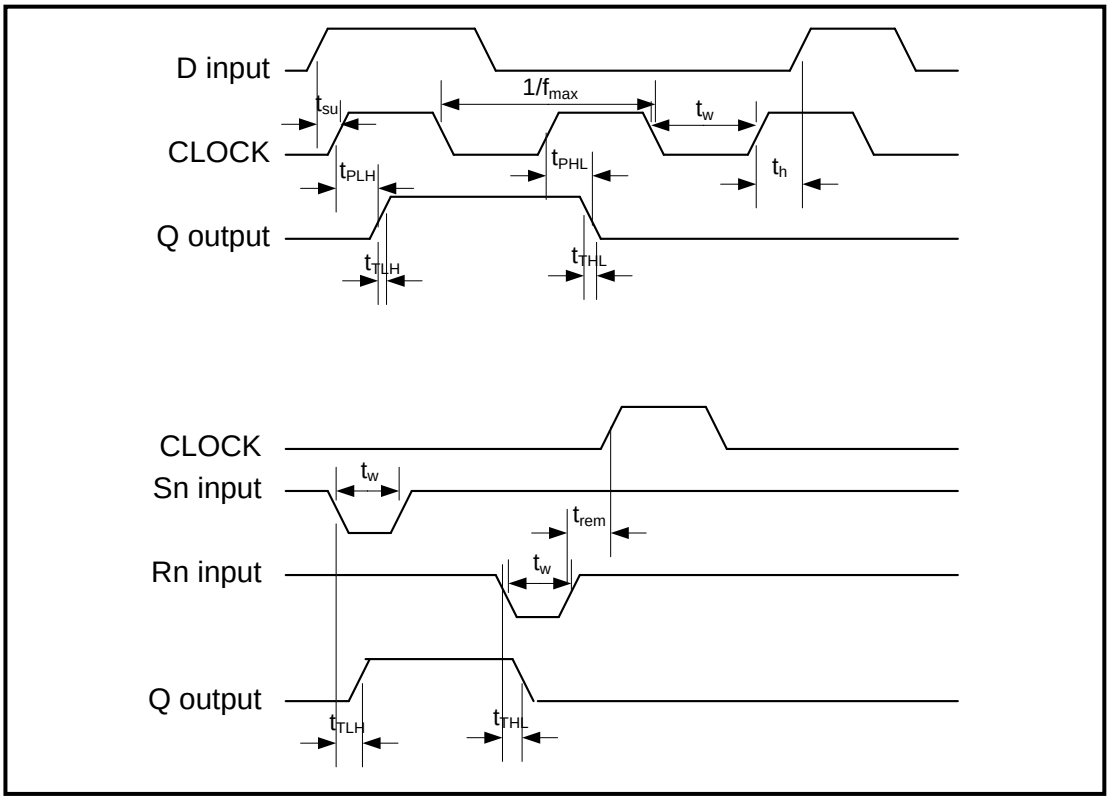
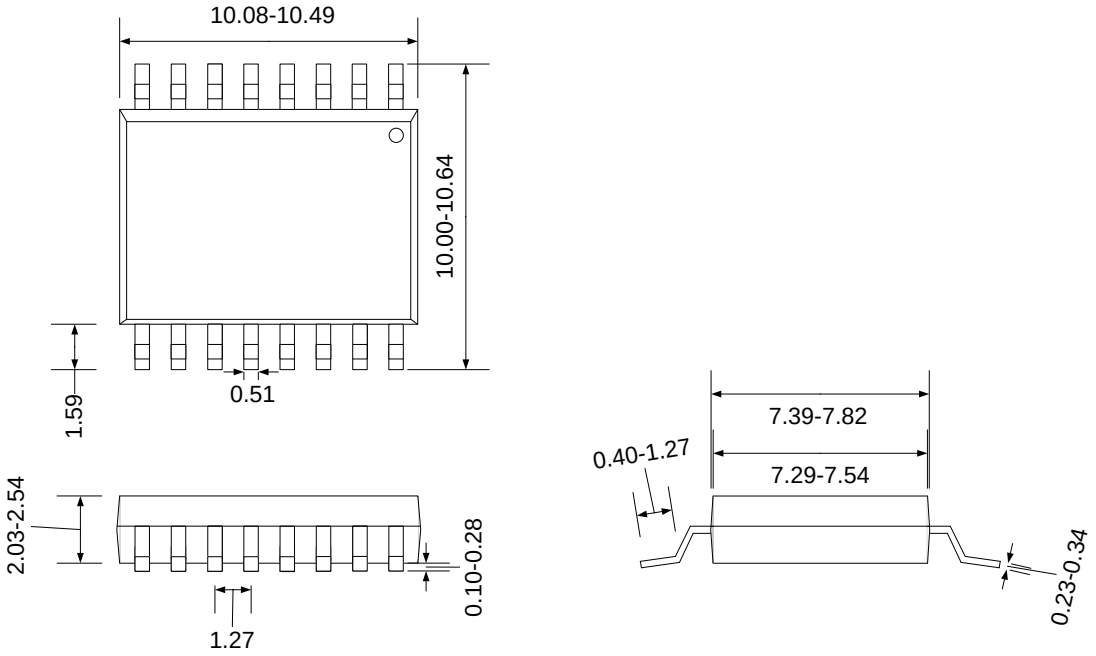


Figure 2. AC Waveforms

Ordering Information

Ordering Reference	Package	Temperature Range	Marking
CMT-7474-PSOIC16-T	Plastic SOIC16	-55°C to +175°C	CMT-7474

Package Dimensions



Drawing PSOIC16 (mm +/- 10%)

Contact & Ordering

CISSOID S.A.

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