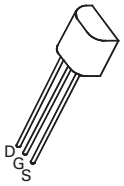
N-CHANNEL ENHANCEMENT MODE VERTICAL DMOS FET

ZVN4206A

ISSUE 2 – JUNE 94

FEATURES

* 60 Volt V_{DS}
* $R_{DS(on)}$ = 1 Ω



E-LINE
TO92 COMPATIBLE

ABSOLUTE MAXIMUM RATINGS.

PARAMETER	SYMBOL	VALUE	UNIT
Drain-Source Voltage	V_{DS}	60	V
Continuous Drain Current at T_{amb}=25°C	I_D	600	mA
Pulsed Drain Current	I_{DM}	8	A
Gate-Source Voltage	V_{GS}	± 20	V
Power Dissipation at T_{amb}=25°C	P_{tot}	0.7	W
Operating and Storage Temperature Range	T_j:T_{stg}	-55 to +150	°C

ELECTRICAL CHARACTERISTICS (at T_{amb} = 25°C unless otherwise stated).

PARAMETER	SYMBOL	MIN.	MAX.	UNIT	CONDITIONS.
Drain-Source Breakdown Voltage	BV_{DSS}	60		V	I_D=1mA, V_{GS}=0V
Gate-Source Threshold Voltage	$V_{GS(th)}$	1.3	3	V	ID=1mA, V_{DS}= V_{GS}
Gate-Body Leakage	I_{GSS}		100	nA	V_{GS}=± 20V, V_{DS}=0V
Zero Gate Voltage Drain Current	I_{DSS}		10 100	µA µA	V_{DS}=60V, V_{GS}=0 V_{DS}=48V, V_{GS}=0V, T=125°C(2)
On-State Drain Current(1)	$I_{D(on)}$	3		A	V_{DS}=25V, V_{GS}=10V
Static Drain-Source On-State Resistance (1)	$R_{DS(on)}$		1 1.5	Ω Ω	V_{GS}=10V,I_D=1.5A V_{GS}=5V,I_D=500mA
Forward Transconductance(1)(2)	g_{fs}	300		mS	V_{DS}=25V,I_D=1.5A
Input Capacitance (2)	C_{iss}		100	pF	V_{DS}=25V, V_{GS}=0V, f=1MHz
Common Source Output Capacitance (2)	C_{oss}		60	pF	
Reverse Transfer Capacitance (2)	C_{rss}		20	pF	
Turn-On Delay Time (2)(3)	$t_{d(on)}$		8	ns	V_{DD} ≈25V, I_D=1.5A
Rise Time (2)(3)	t_r		12	ns	
Turn-Off Delay Time (2)(3)	$t_{d(off)}$		12	ns	
Fall Time (2)(3)	t_f		15	ns	

(1) Measured under pulsed conditions. Width=300µs. Duty cycle ≤2% (2) Sample test.
(3) Switching times measured with 50Ω source impedance and <5ns rise time on a pulse generator

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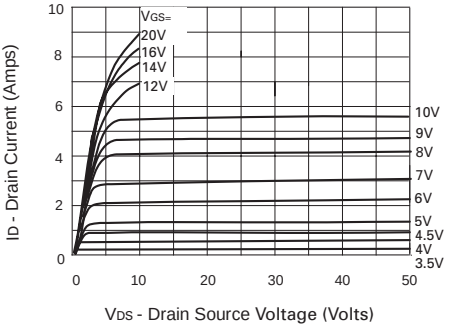
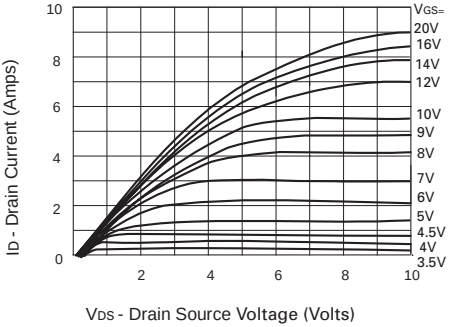
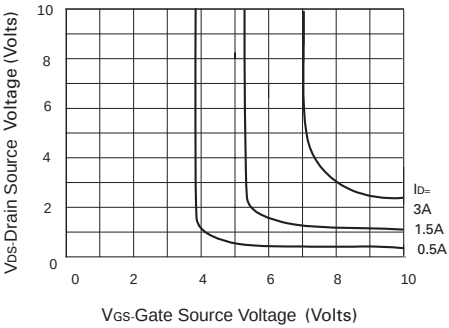
TYPICAL CHARACTERISTICS



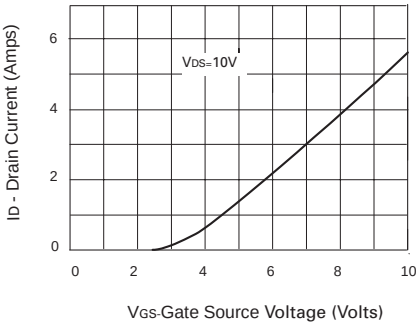
Output Characteristics



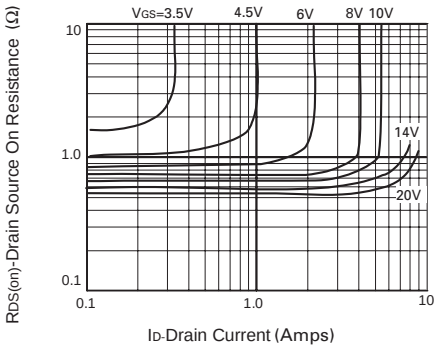
Saturation Characteristics



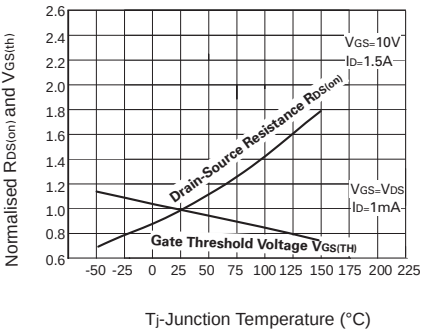
Voltage Saturation Characteristics



Transfer Characteristics

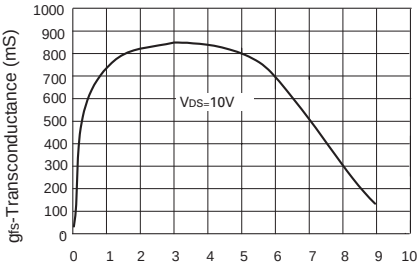


On-resistance v drain current

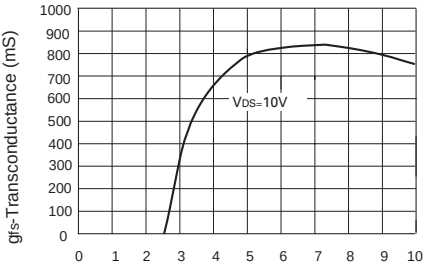


Normalised $R_{DS(on)}$ and $V_{GS(th)}$ v Temperature

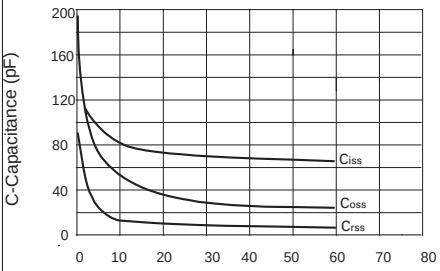
TYPICAL CHARACTERISTICS



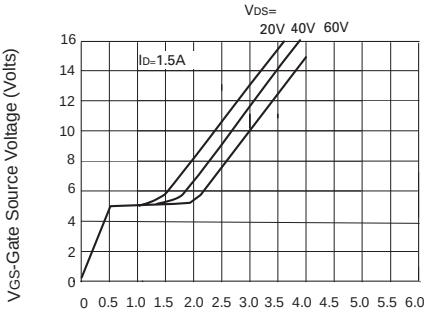
Transconductance v drain current



Transconductance v gate-source voltage



Capacitance v drain-source voltage



Gate charge v gate-source voltage