DYNEX

TA329..Q

Asymmetric Thyristor

Replaces January 2000 version, DS4680-3.0

DS4680-3.1 July 2002

APPLICATIONS

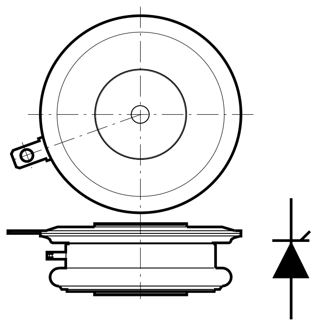
- High Frequency Applications
- High Power Choppers And Inverters
- Welding
- Ultrasonic Generators
- Induction Heating
- 400Hz UPS
- PWM Inverters

KEY PARAMETERS

V_{DRM}	**1400V**
$I_{T(RMS)}$	**370A**
I_{TSM}	**2000A**
dVdt	**1000V/µs**
dI/dt	**1000A/µs**
t_q	**7.0µs**

FEATURES

- Low Loss Asymmetrical Diffusion Structure
- High Interdigitated Amplifying Gate
- Gate Assisted Turn-off With Exclusive Bypass Diode
- Fully Characterised For Operation up to 40kHz
- Directly Compatible With 220-480 A.c. Mains



Outline type code: MU86.
See Package Details for further information.

VOLTAGE RATINGS

Type Number	Repetitive Peak Off-state Voltage V_{DRM} V	Repetitive Peak Reverse Voltage V_{RRM} V
TA329 14 Q	1400	10
TA329 12 Q	1200	10
TA329 10 Q	1000	10

Lower voltage grades available.

CURRENT AND SURGE RATINGS

Symbol	Parameter	Conditions	Max.	Units
Double Side Cooled				
$I_{T(RMS)}$	RMS value	Half sine wave, duty cycle 50%, T_{case} = 80°C, T_j = 125°C.	370	A
I_{TSM}	Surge (non-repetitive) on-state current	T_j = 125°C, t_p = 1ms, V_R = 0	2000	A
I^2t	I^2t for fusing	$t_p \geq$ 10ms	20 x 10^3	A^2s

THERMAL AND MECHANICAL DATA

Symbol	Parameter	Conditions		Min.	Max.	Units
$R_{th(j-c)}$	Thermal resistance - junction to case	Double side cooled	dc	-	0.085	°C/W
		Single side cooled	Anode dc	-	0.153	°C/W
			Cathode dc	-	0.204	°C/W
$R_{th(c-h)}$	Thermal resistance - case to heatsink	Clamping force 4.0kN with mounting compound	Double side	-	0.02	°C/W
			Single side	-	0.04	°C/W
T_{vj}	Virtual junction temperature	On-state (conducting)		-	135	°C
		Reverse (blocking)		-	125	°C
T_{stg}	Storage temperature range			-40	150	°C
-	Clamping force			3.6	4.4	kN

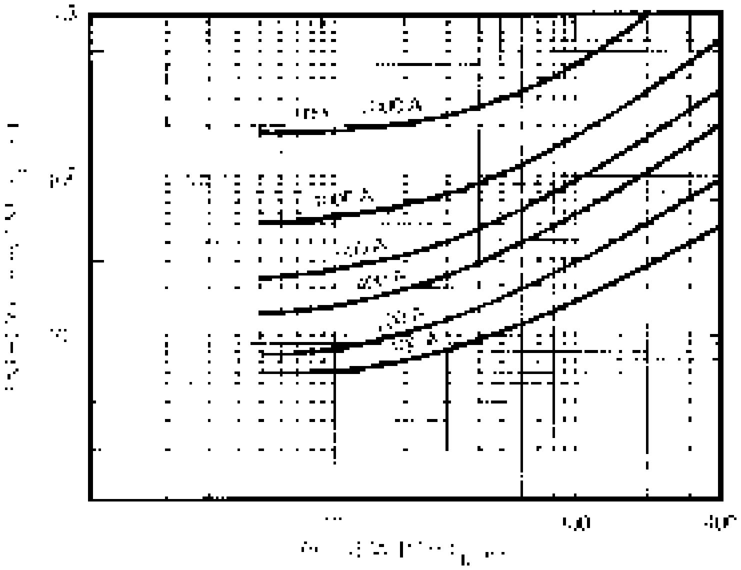
DYNAMIC CHARACTERISTICS

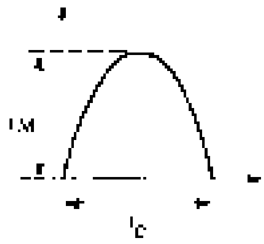
Symbol	Parameter	Conditions		Min.	Max.	Units
V_{TM}	Maximum on-state voltage	At 600A peak, T_{case} = 125°C		-	2.5	V
I_{RRM}	Peak reverse current	At V_{RRM}, T_{case} = 125°C		-	30	mA
I_{DRM}	Off-state current	At V_{DRM}, T_{case} = 125°C		-	1	mA
dV/dt	Maximum linear rate of rise of off-state voltage	To 60% V_{DRM} T_j = 125°C, Gate open circuit		-	1000	V/µs
dI/dt	Rate of rise of on-state current	Gate source 20V, 20Ω $t_r \le$ 5µs.	Non-repetitive	-	1000	A/µs
			Repetitive	-	500	A/µs
t_q†	Max. gate assisted turn-off time (with feedback diode)	T_j = 125°C, $I_{T(PK)}$ = 200A, t_p = 25µs (half sine wave), V_R = DF451 Diode voltage drop, dV/dt = 600V/µs (linear to 60% V_{DRM}), V_{GK} = -5V		-	7	µs
t_q	Max. turn-off time (with feedback diode)	T_j = 125°C, I_{TM} = 100A, t_p > 100µs, dI_R/dt = 30A/µs, V_R = 1V, dV/dt = 600V/µs (linear to 60% V_{DRM}), Gate open.		-	10	µs

GATE TRIGGER CHARACTERISTICS AND RATINGS

Symbol	Parameter	Conditions	Typ.	Max.	Units
V_{GT}	Gate trigger voltage	V_{DWM} = 12V, R_L = 3Ω, T_{case} = 25°C	-	4	V
I_{GT}	Gate trigger current	V_{DWM} = 12V, R_L = 3Ω, T_{case} = 25°C	-	250	mA
V_{RGM}	Peak reverse gate voltage	-	-	7	V
I_{FGM}	Peak forward gate current	-	-	10	A
P_{GM}	Peak gate power	-	-	50	W
$P_{G(AV)}$	Average gate power	-	-	15	W

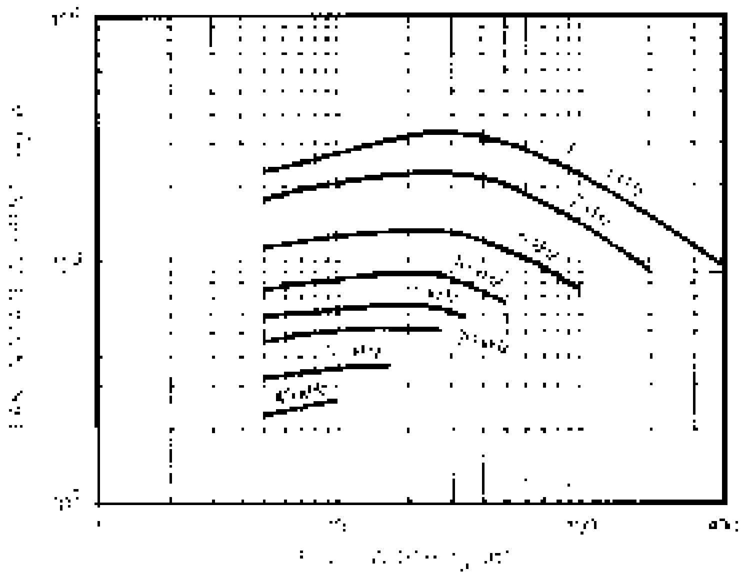
CURVES

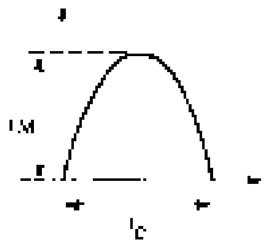




Notes:
1. VD ≤ 600V.
2. VR = DF451 Diode voltage drop.
3. R.C. snubber. C = 0.1μF, R = 33Ω.
4. Double side cooled.

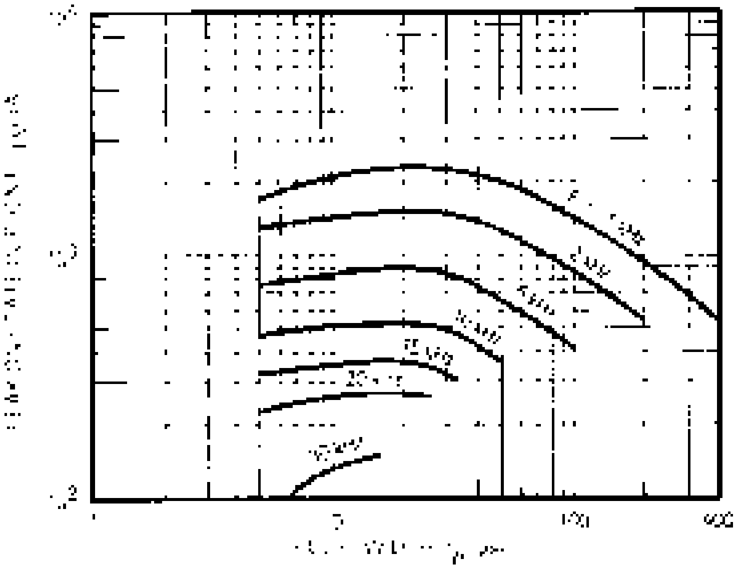
Fig.1 Energy per pulse for sinusoidal pulses.

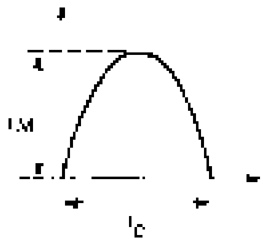




Notes:
1. VD ≤ 600V.
2. VR = DF451 Diode voltage drop.
3. R.C. snubber. C = 0.1μF, R = 33Ω.
4. Double side cooled.

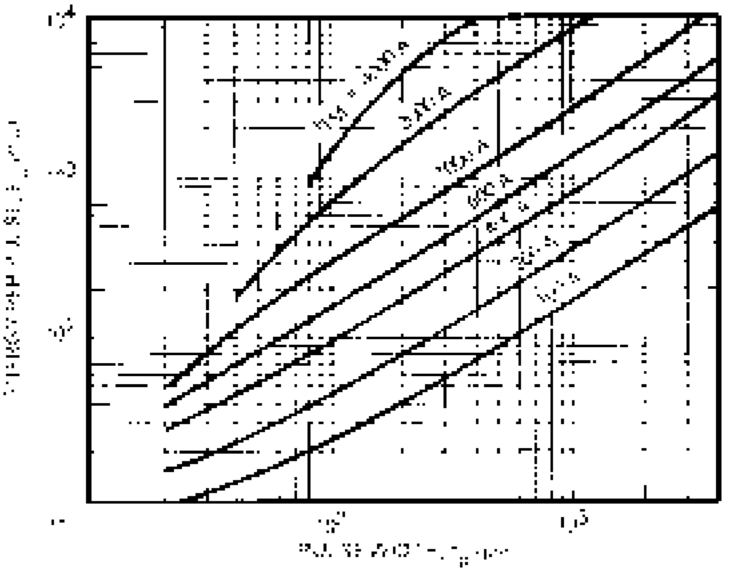
Fig.2 Maximum allowable peak on-state current vs pulse width for Tcase = 65˚C.

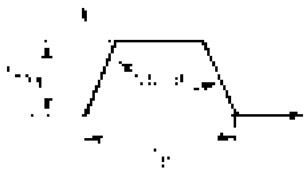




Notes:
1. VD ≤ 600V.
2. VR = DF451 Diode voltage drop.
3. R.C. snubber. C = 0.1µF, R = 33Ω.
4. Double side cooled.

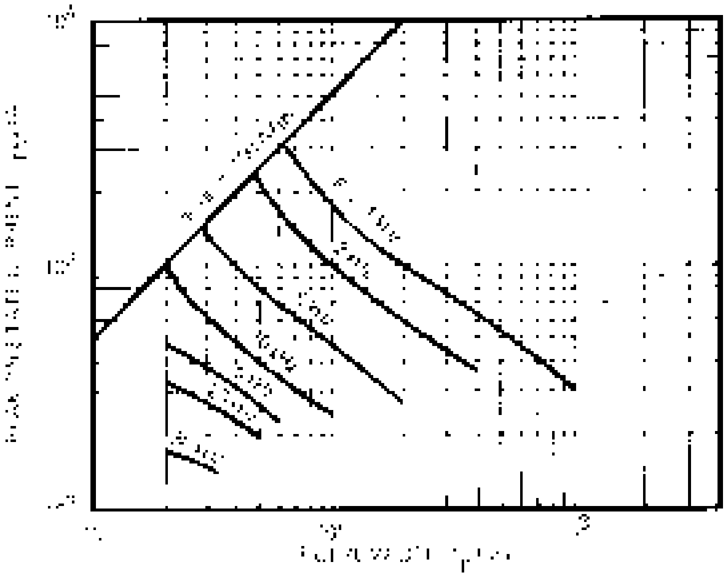
Fig.3 Maximum allowable peak on-state current vs pulse width for Tcase = 90˚C.





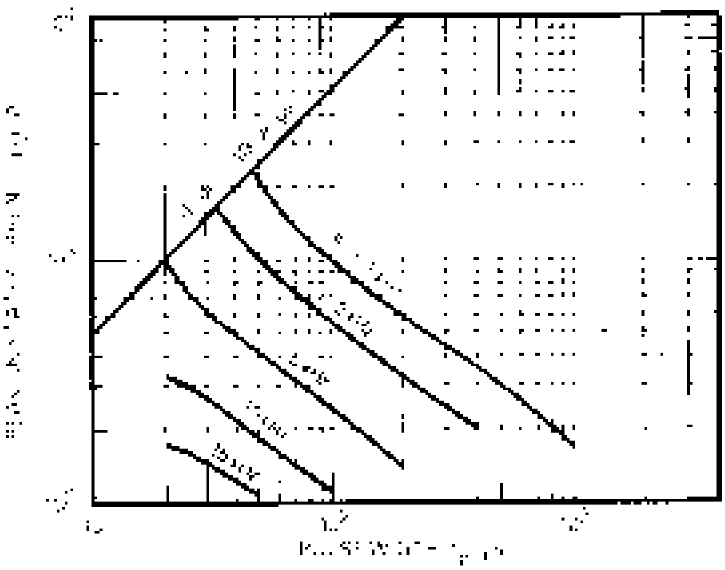
Notes:
1. dI/dt = 100A/µs.
2. VD ≤ 600V.
3. VR = DF451 Diode voltage drop.
4. R.C. snubber. C = 0.1µF, R = 33Ω.
5. Double side cooled.

Fig.4 Energy per pulse for trapezoidal pulses



Notes:
1. dI/dt = 100A/µs.
2. VD ≤ 600V.
3. VR = DF451 Diode voltage drop.
4. R.C. snubber. C = 0.1µF, R = 33Ω.
5. Double side cooled.

Fig.5 Maximum allowable peak on-state current vs pulse width for Tcase = 65˚C.



Notes:
1. dI/dt = 100A/µs.
2. VD ≤ 600V.
3. VR = DF451 Diode voltage drop.
4. R.C. snubber. C = 0.1µF, R = 33Ω.
5. Double side cooled.

Fig.6 Maximum allowable peak on-state current vs pulse width for Tcase = 90˚C.

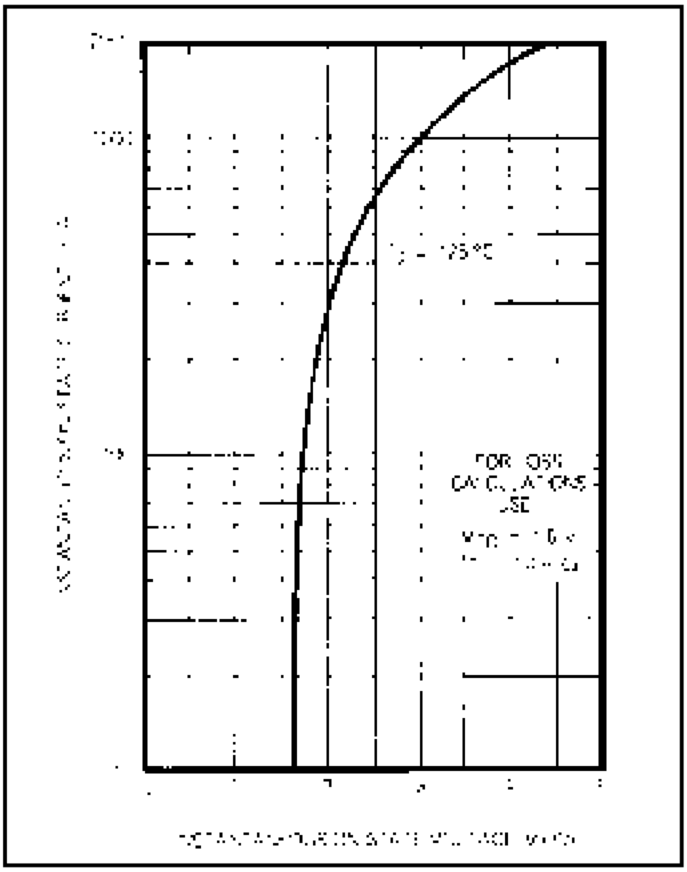


Fig.7 Maximum on-state conduction characteristic

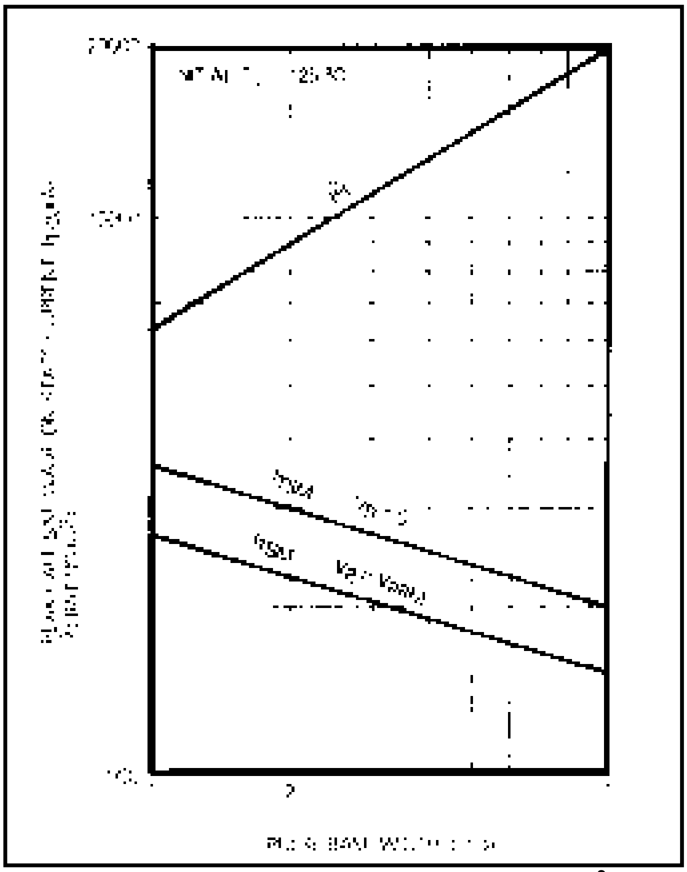


Fig.8 Non-repetitive sub-cycle surge on-state current and I^2t rating.

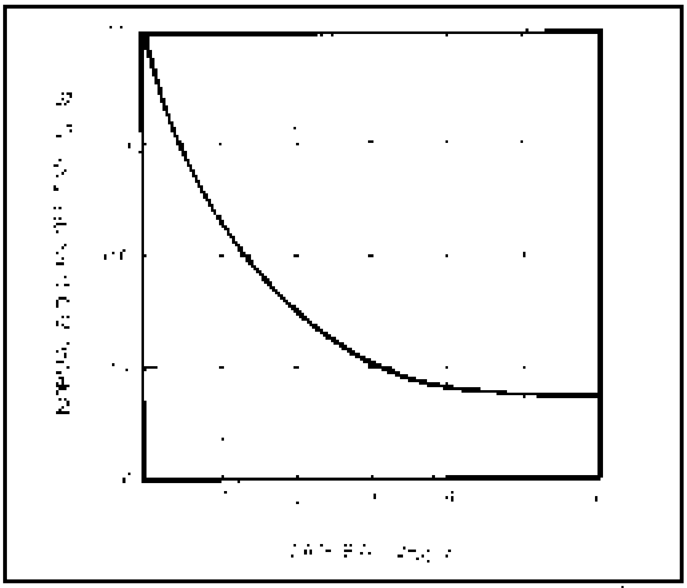


Fig.9 Typical variation of effective turn-off time (t_q†) with negative gate bias.

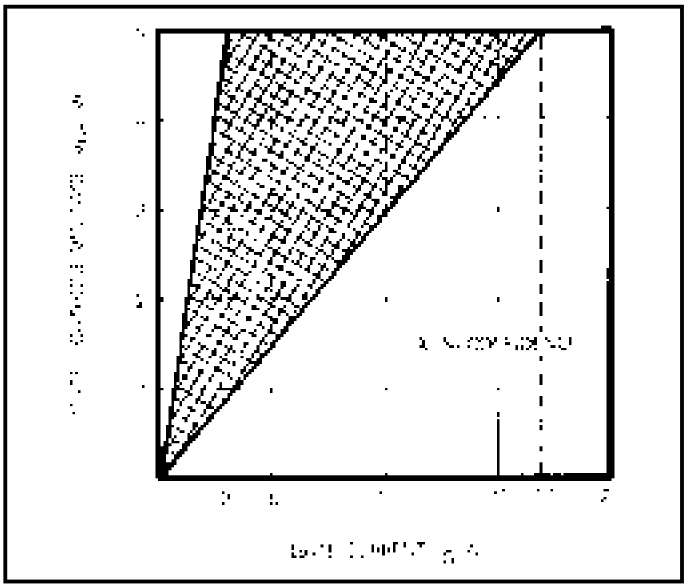


Fig.10 Reverse gate characteristics

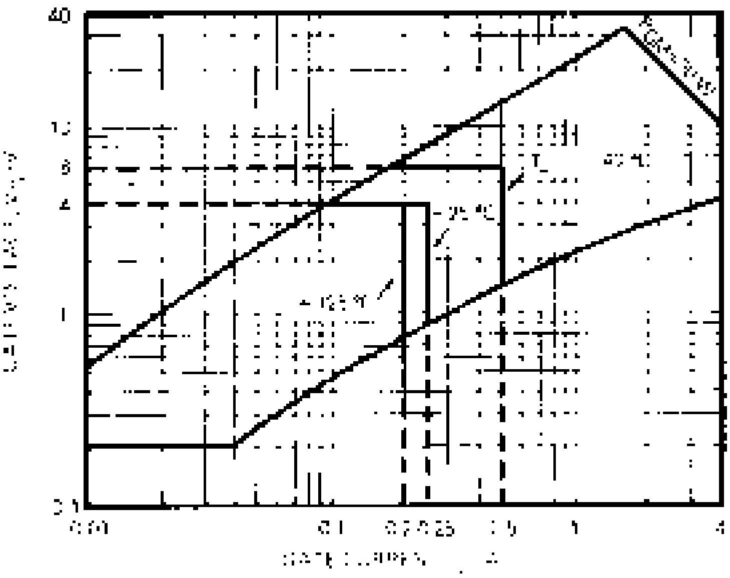


Fig.11 Gate trigger characteristics

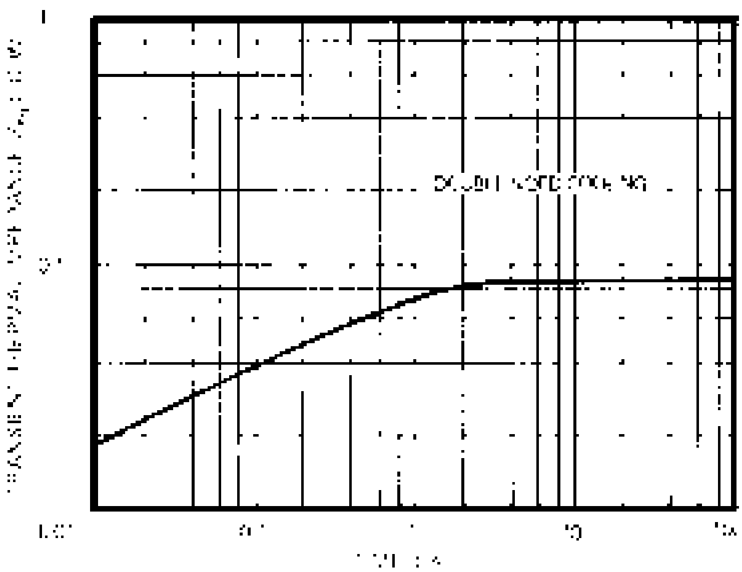
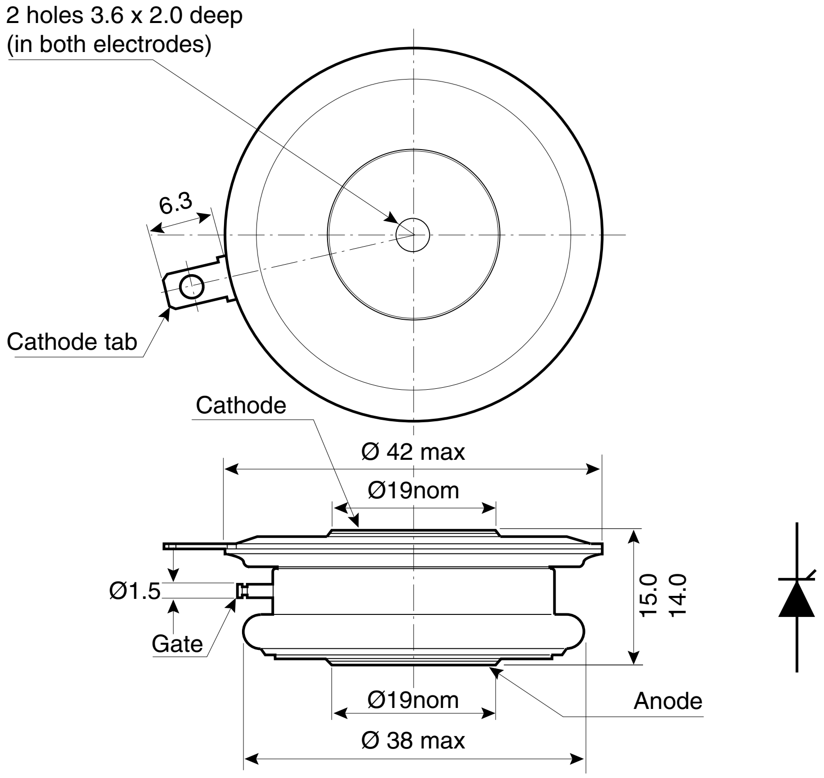


Fig.12 Transient thermal impedance - junction to case

PACKAGE DETAILS

For further package information, please contact Customer Services. All dimensions in mm, unless stated otherwise.
DO NOT SCALE.



Nominal weight: 50g
Clamping force: 3.5kN ±10%
Lead length: 250mm

Package outline type code: MU86

POWER ASSEMBLY CAPABILITY

The Power Assembly group was set up to provide a support service for those customers requiring more than the basic semiconductor, and has developed a flexible range of heatsink and clamping systems in line with advances in device voltages and current capability of our semiconductors.

We offer an extensive range of air and liquid cooled assemblies covering the full range of circuit designs in general use today. The Assembly group offers high quality engineering support dedicated to designing new units to satisfy the growing needs of our customers.

Using the latest CAD methods our team of design and applications engineers aim to provide the Power Assembly Complete Solution (PACs).

HEATSINKS

The Power Assembly group has its own proprietary range of extruded aluminium heatsinks which have been designed to optimise the performance of Dynex semiconductors. Data with respect to air natural, forced air and liquid cooling (with flow rates) is available on request.

For further information on device clamps, heatsinks and assemblies, please contact your nearest sales representative or Customer Services.

Stresses above those listed in this data sheet may cause permanent damage to the device. In extreme conditions, as with all semiconductors, this may include potentially hazardous rupture of the package. Appropriate safety precautions should always be followed.

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