8M x 32 Mobile LPDDR2 Synchronous DRAM (SDRAM)

Etron Confidential **Advance (Rev. 1.1, Dec. /2017)**

Features

- Fast clock rate: 333/400/533 MHz
- Differential Clock inputs CK/CK#
- JEDEC standard Compliant
- Four-bit prefetch DDR architecture
- Four internal banks, 2M x 32-bit for each bank
- Double data rate architecture for command, address and data Bus
- Bidirectional/differential data strobe per byte of data DQS/DQS#
- Programmable Mode Registers
  - READ and WRITE latencies (RL/WL)
  - Burst length: 4, 8, or 16
  - PASR (Partial Array Self Refresh)
- Auto TCSR (Temperature Compensated Self Refresh)
- Auto Refresh and Self Refresh
- Deep power-down
- 4096 refresh cycles / 32ms
- Power supplies:
  - V_{DD1} = 1.8V (1.7V~1.95V)
  - V_{DD2} = 1.2V (1.14V~1.3V)
  - V_{DDCA} /V_{DDQ} = 1.2V (1.14V~1.3V)
- Interface: HSUL_12
- Operating Temperature: T_C = -25 ~ 85°C
- Package: 134-ball 10 x 11.5 x 1.0mm (max) FBGA
  - Pb Free and Halogen Free

Overview

The EM6KA32H LPDDR2 SDRAM is a high-speed CMOS, dynamic random-access memory containing 268,435,456 bits. It is internally configured as a 4 banks of 2,097,152 words by 32 bits memory device. The devices use double data rate architecture on the command/address (CA) bus to reduce the number of input pins in the system. The 10-bit CA bus contains command, address, and Bank/Row Buffer information. Each command uses one clock cycle, during which command information is transferred on both the positive and negative edge of the clock. LPDDR2 also use double data rate architecture on the DQ pins to achieve high speed operation. The double data rate architecture is essentially a 4n prefetch architecture with an interface designed to transfer two data bits per DQ every clock cycle at the I/O pins. A single read or write access for the LPDDR2 effectively consists of a single 4n-bit wide, one clock cycle data transfer at the internal SDRAM/NVM core and four corresponding n-bit wide, one-half-clock-cycle data transfers at the I/O pins. Read and write accesses to the LPDDR2 are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence.

Table 1. Ordering Information

Part Number	Clock Frequency	Data Rate	Power Supply	Package
EM6KA32HVAFA-18H	533MHz	1066Mbps/pin	V_{DD1} 1.8V, V_{DDCA} /V_{DDQ} /V_{DD2} 1.2V	FBGA
EM6KA32HVAFA-25H	400MHz	800Mbps/pin	V_{DD1} 1.8V, V_{DDCA} /V_{DDQ} /V_{DD2} 1.2V	FBGA
EM6KA32HVAFA-3H	333MHz	667Mbps/pin	V_{DD1} 1.8V, V_{DDCA} /V_{DDQ} /V_{DD2} 1.2V	FBGA

VAF: indicates 10 x 11.5 x 1.0mm FBGA Package
A(11^{th} digit): indicates Generation Code
H(Last digit): indicates Pb Free and Halogen Free

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Figure 1. Ball Assignment (FBGA Top View)

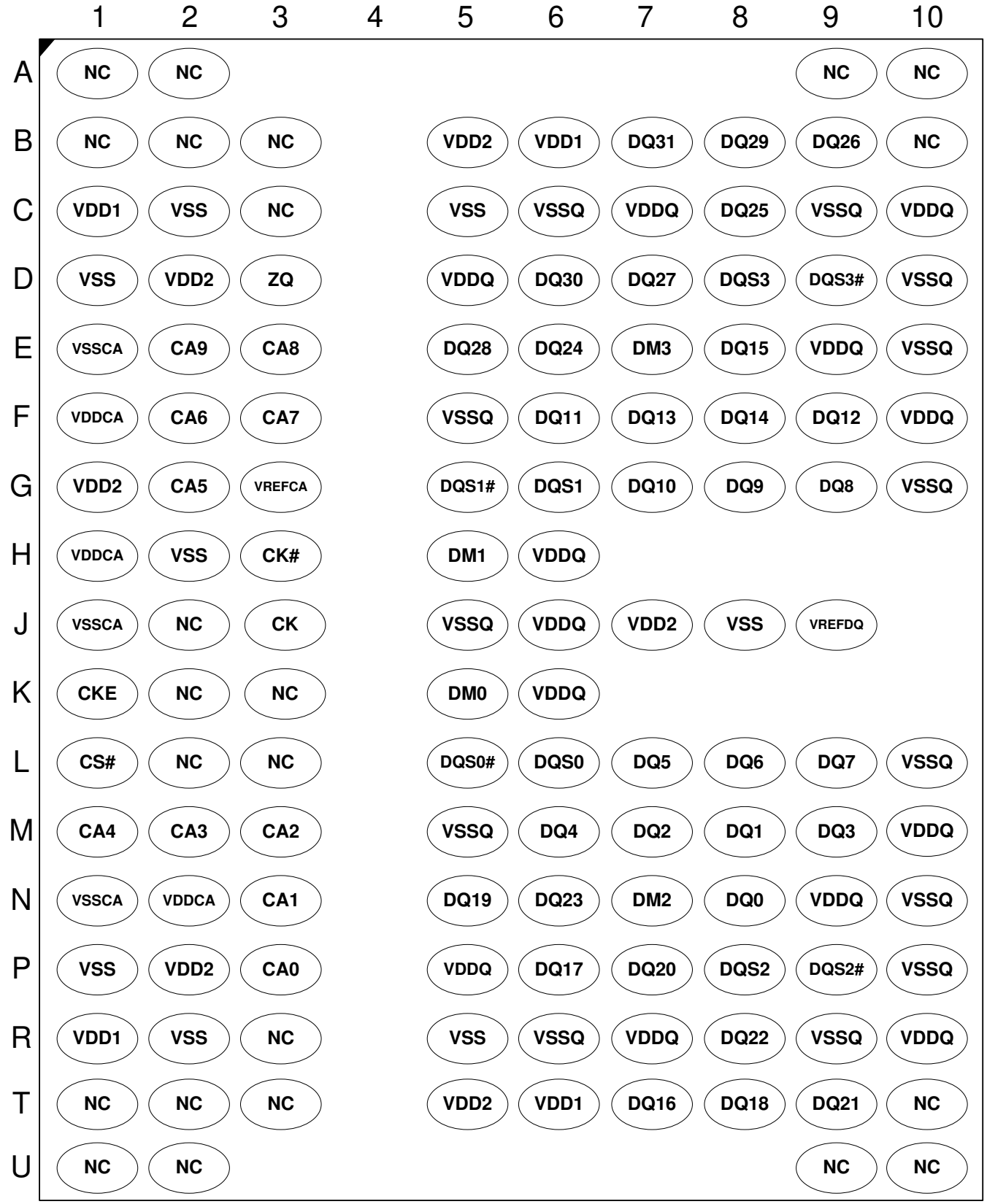


Figure 2. Block Diagram

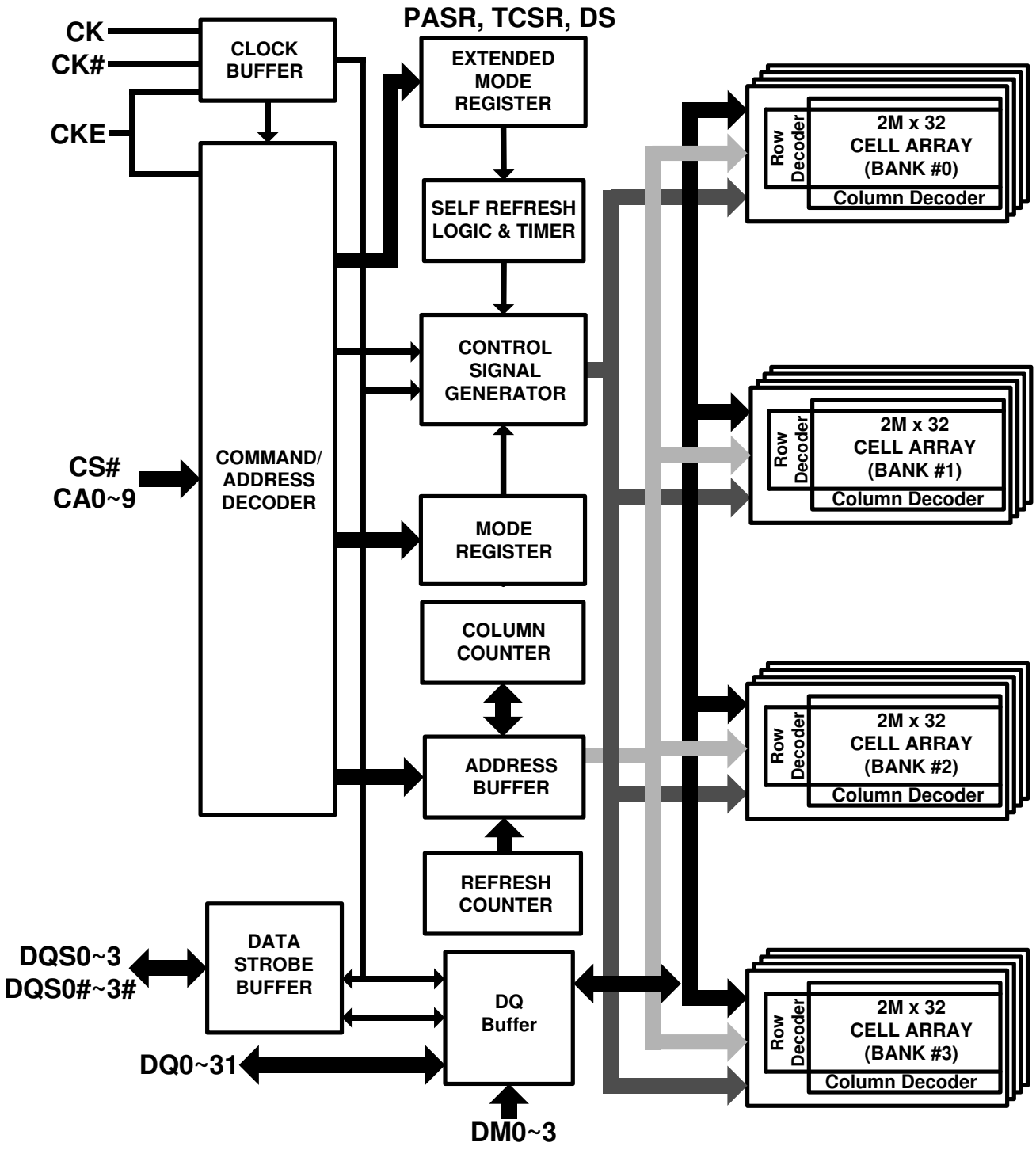
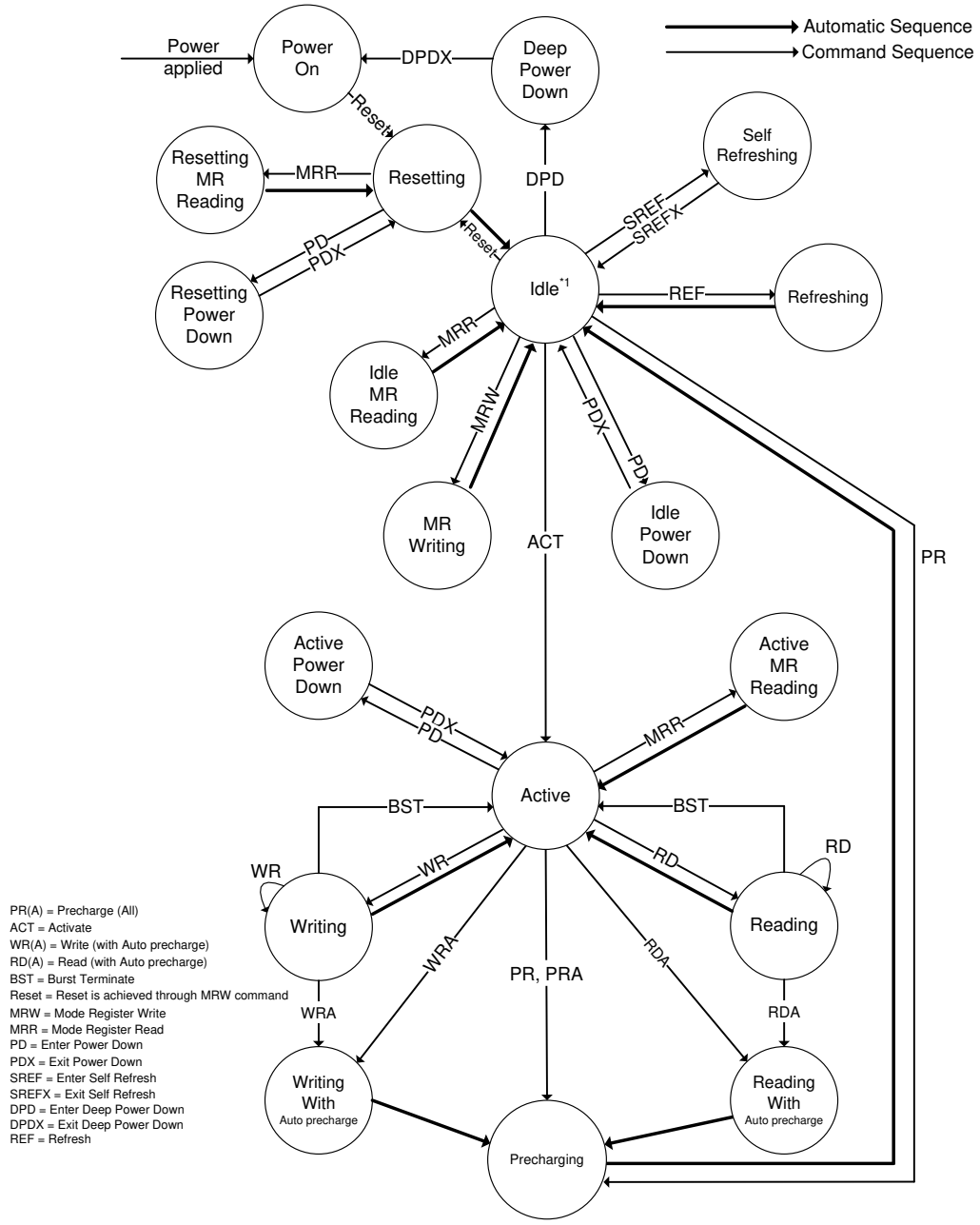


Figure 3. State Diagram



NOTE 1. All banks are precharged in the idle state.

Ball Descriptions

Table 2. Ball Details

Symbol	Type	Description
CK, CK#	Input	**Differential Clock:** CK and CK# are differential clock inputs. All CA inputs are sampled on both rising and falling edges of CK. CS# and CKE inputs are sampled at the rising edge of CK. AC timings are referenced to clock.
CKE	Input	**Clock Enable:** CKE HIGH activates and CKE LOW deactivates the internal clock signals, input buffers, and output drivers. Power-saving modes are entered and exited via CKE transitions. CKE is considered part of the command code. CKE is sampled at the rising edge of CK.
CS#	Input	**Chip Select:** CS# is considered part of the command code and is sampled at the rising edge of CK.
CA0 – CA9	Input	**DDR Command/Address Inputs:** Provide the command and address inputs according to the command truth table.
DQ0 – DQ31	Input / Output	**Data input/output:** Bidirectional data bus.
DQS0 – DQS3 DQS0# – DQS3#	Input / Output	**Data Strobe:** The data strobe is bi-directional (used for read and write data) and differential (DQS and DQS#). It is output with read data and input with write data. DQS is edge-aligned to read data and centered with write data. DQS0 and DQS0# correspond to the data on DQ0 - DQ7. DQS1 and DQS1# correspond to the data on DQ8 - DQ15. DQS2 and DQS2# correspond to the data on DQ16 – DQ23. DQS3 and DQS3# correspond to the data on DQ24 – DQ31.
DM0 – DM3	Input	**Input Data Mask:** DM is an input mask signal for write data. Although DM balls are input-only, the DM loading is designed to match that of DQ and DQS balls. DM0 is the input data mask signal for the data on DQ0-7. DM1 is the input data mask signal for the data on DQ8-15. DM2 is the input data mask signal for the data on DQ16 – DQ23. DM3 is the input data mask signal for the data on DQ24 – DQ31.
V_{DDQ}	Supply	**DQ Power Supply:** Provide isolated power to DQs for improved noise immunity.
V_{SSQ}	Supply	**DQ Ground:** Provide isolated ground to DQs for improved noise immunity.
V_{DDCA}	Supply	**Command/address power supply:** Command/address power supply.
V_{SSCA}	Supply	**Ground for Input Receivers**
V_{DD1}	Supply	**Core power:** Supply 1.
V_{DD2}	Supply	**Core power:** Supply 2.
V_{SS}	Supply	**Ground**
V_{REFCA}, V_{REFDQ}	Supply	**Reference voltage:** V_{REFCA} is reference for command/address input buffers, V_{REFDQ} is reference for DQ input buffers.
ZQ	Reference	**Reference Pin for Output Drive Strength Calibration**
NC	-	**No Connect:** No internal connection.

Truth Tables

Operation or timing that is not specified is illegal and after such an event, in order to guarantee proper operation, the device must be powered down and then restarted through the specified initialization sequence before normal operation can continue.

Table 3. Command Truth Table

Command	Command Pins			CA Pins										CK Edge
	CKE		CS#	CA0	CA1	CA2	CA3	CA4	CA5	CA6	CA7	CA8	CA9	
	CK_{n-1}	CK_n												
MRW	H	H	L	L	L	L	L	MA0	MA1	MA2	MA3	MA4	MA5	↑
			X	MA6	MA7	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7	↓
MRR	H	H	L	L	L	L	H	MA0	MA1	MA2	MA3	MA4	MA5	↑
			X	MA6	MA7	X	X	X	X	X	X	X	X	↓
Refresh (All bank)	H	H	L	L	L	H	H	X	X	X	X	X	X	↑
			X	X	X	X	X	X	X	X	X	X	X	↓
Enter Self Refresh	H	L	L	L	L	H	X	X	X	X	X	X	X	↑
	X		X	X	X	X	X	X	X	X	X	X	X	↓
Activate	H	H	L	L	H	R8	R9	R10	R11	R12	BA0	BA1	X	↑
			X	R0	R1	R2	R3	R4	R5	R6	R7	X	X	↓
Write	H	H	L	H	L	L	RFU	RFU	C1	C2	BA0	BA1	X	↑
			X	AP	C3	C4	C5	C6	C7	X	X	X	X	↓
Read	H	H	L	H	L	H	RFU	RFU	C1	C2	BA0	BA1	X	↑
			X	AP	C3	C4	C5	C6	C7	X	X	X	X	↓
Precharge	H	H	L	H	H	L	H	AB	X	X	BA0	BA1	X	↑
			X	X	X	X	X	X	X	X	X	X	X	↓
BST	H	H	L	H	H	L	L	X	X	X	X	X	X	↑
			X	X	X	X	X	X	X	X	X	X	X	↓
Enter DPD	H	L	L	H	H	L	X	X	X	X	X	X	X	↑
	X		X	X	X	X	X	X	X	X	X	X	X	↓
NOP	H	H	L	H	H	H	X	X	X	X	X	X	X	↑
			X	X	X	X	X	X	X	X	X	X	X	↓
Maintain PD, SREF, DPD (NOP)	L	L	L	H	H	H	X	X	X	X	X	X	X	↑
			X	X	X	X	X	X	X	X	X	X	X	↓
NOP	H	H	H	X	X	X	X	X	X	X	X	X	X	↑
			X	X	X	X	X	X	X	X	X	X	X	↓
Maintain PD, SREF, DPD (NOP)	L	L	H	X	X	X	X	X	X	X	X	X	X	↑
			X	X	X	X	X	X	X	X	X	X	X	↓
Enter Power Down	H	L	H	X	X	X	X	X	X	X	X	X	X	↑
	X		X	X	X	X	X	X	X	X	X	X	X	↓
Exit PD, SREF, DPD	L	H	H	X	X	X	X	X	X	X	X	X	X	↑
	X		X	X	X	X	X	X	X	X	X	X	X	↓

Notes:

1. All commands are defined by the current state of CS#, CA0, CA1, CA2, CA3, and CKE at the rising edge of the clock.
2. Bank addresses (BA) determine which bank will be operated upon.
3. AP HIGH during a READ or WRITE command indicates that an auto precharge will occur to the bank associated with the READ or WRITE command.
4. "X" indicates a "Don't Care" state, with a defined logic level, either HIGH (H) or LOW (L).
5. Self refresh exit and DPD exit are asynchronous.
6. VREF must be between 0 and VDDQ during self refresh and DPD operation.
7. CAxr refers to command/address bit "X" on the rising edge of clock.
8. CAxf refers to command/address bit "X" on the falling edge of clock.
9. CS# and CKE are sampled on the rising edge of the clock.
10. The least-significant column address C0 is not transmitted on the CA bus, and is inferred to be zero.

Table 4. CKE Truth Table

Notes 1 – 5 apply to all parameters and conditions; L = LOW, H = HIGH, X = "Don't Care"

Current State	CK_{n-1}	CK_n	CS#	Command n	Operation n	Next State	Note
Active power-down	L	L	X	X	Maintain active power-down	Active power-down	
	L	H	H	NOP	Exit active power-down	Active	6, 7
Idle power-down	L	L	X	X	Maintain active power-down	Idle power-down	
	L	H	H	NOP	Exit idle power-down	Idle	6, 7
Resetting idle power-down	L	L	X	X	Maintain resetting power-down	Resetting power-down	
	L	H	H	NOP	Exit resetting power-down	Idle or resetting	6, 7, 8
Deep power-down	L	L	X	X	Maintain deep power-down	Deep power-down	
	L	H	H	NOP	Exit deep power-down	Power-on	9
Self refresh	L	L	X	X	Maintain self refresh	Self refresh	
	L	H	H	NOP	Exit self refresh	Idle	10, 11
Bank active	H	L	H	NOP	Enter active power-down	Active power-down	
All banks idle	H	L	H	NOP	Enter idle power-down	Idle power-down	
	H	L	L	Enter self refresh	Enter self refresh	Self refresh	
	H	L	L	DPD	Enter self refresh	Deep power-down	
Resetting	H	L	H	NOP	Enter resetting power-down	Resetting power-down	
Other states	H	H	Refer to the command truth table				

Notes:

1. Current state = the state of the device immediately prior to the clock rising edge n.
2. All states and sequences not shown are illegal or reserved unless explicitly described elsewhere in this document.
3. CKEn = the logic state of CKE at clock rising edge n; CKEn-1 was the state of CKE at the previous clock edge.
4. CS# = the logic state of CS# at the clock rising edge n.
5. Command n = the command registered at clock edge n, and operation n is a result of command n.
6. Power-down exit time (tXP) must elapse before any command other than NOP is issued.
7. The clock must toggle at least twice prior to the tXP period.
8. Upon exiting the resetting power-down state, the device will return to the idle state if tINIT5 has expired.
9. The DPD exit procedure must be followed as described in Deep Power-Down.
10. Self refresh exit time (tXSR) must elapse before any command other than NOP is issued.
11. The clock must toggle at least twice prior to the tXSR time.

Table 5. Current State Bank n - Command to Bank n

Notes 1 – 5 apply to all parameters and conditions

Current State	Command	Operation	Next State	Note
Any	NOP	Continue previous operation	Current state	
Idle	ACTIVATE	Select and activate row	Active	
	Refresh (all banks)	Begin to refresh	Refreshing (all banks)	6
	MRW	Load value to mode register	MR writing	6
	MRR	Read value from mode register	Idle, MR reading	
	RESET	Begin device auto initialization	Resetting	6, 7
	PRECHARGE	Deactivate row(s) in bank or banks	Precharging	8, 9
Row active	READ	Select column and start read burst	Reading	
	WRITE	Select column and start write burst	Writing	
	MRR	Read value from mode register	Active MR reading	
	PRECHARGE	Deactivate row(s) in bank or banks	Precharging	8
Reading	READ	Select column and start new read burst	Reading	10, 11
	WRITE	Select column and start write burst	Writing	10, 11, 12
	BST	Read burst terminate	Active	13
Writing	WRITE	Select column and start new write burst	Writing	10, 11
	READ	Select column and start read burst	Reading	10, 11, 14
	BST	Write burst terminate	Active	13
Power-on	MRW RESET	Begin device auto initialization	Resetting	6, 8
Resetting	MRR	Read value from mode register	Resetting MR reading	

Notes:

1. Values in this table apply when both CKE n-1 and CKEn are HIGH, and after tXSR or tXP has been met, if the previous state was power-down.
2. All states and sequences not shown are illegal or reserved.
3. Current state definitions:
   Idle: The bank or banks have been precharged, and tRP has been met.
   Active: A row in the bank has been activated, and tRCD has been met. No data bursts or accesses and no register accesses are in progress.
   Reading: A READ burst has been initiated with auto precharge disabled and has not yet terminated or been terminated.
   Writing: A WRITE burst has been initiated with auto precharge disabled and has not yet terminated or been terminated.
4. The states listed below must not be interrupted by a command issued to the same bank. NOP commands or supported commands to the other bank must be issued on any clock edge occurring during these states. Supported commands to the other banks are determined by that banks current state.
   Precharge: Starts with registration of a PRECHARGE command and ends when tRP is met. After tRP is met, the bank is in the idle state.
   Row activate: Starts with registration of an ACTIVATE command and ends when tRCD is met. After tRCD is met, the bank is in the active state.
   READ with AP enabled: Starts with registration of a READ command with auto precharge enabled and ends when tRP is met. After tRP is met, the bank is in the idle state.
   WRITE with AP enabled: Starts with registration of a WRITE command with auto precharge enabled and ends when tRP is met. After tRP is met, the bank is in the idle state.

5. The states listed below must not be interrupted by any executable command. NOP commands must be applied to each rising clock edge during these states.
   Refresh (all banks): Starts with registration of a REFRESH (all banks) command and ends when tRFCab is met. After tRFCab is met, the device is in the all banks idle state.
   Idle MR reading: Starts with registration of the MRR command and ends when tMRR is met. After tMRR is met, the device is in the all banks idle state.
   Resetting MR reading: Starts with registration of the MRR command and ends when tMRR is met. After tMRR is met, the device is in the all banks idle state.
   Active MR reading: Starts with registration of the MRR command and ends when tMRR is met. After tMRR is met, the bank is in the active state.
   MR writing: Starts with registration of the MRW command and ends when tMRW is met. After tMRW is met, the device is in the all banks idle state.
   Precharging all: Starts with registration of a PRECHARGE ALL command and ends when tRP is met. After tRP is met, the device is in the all banks idle state.
6. Not bank-specific; requires that all banks are idle and no bursts are in progress.
7. Not bank-specific.
8. This command may or may not be bank specific. If all banks are being precharged, they must be in a valid state for precharging.
9. If a PRECHARGE command is issued to a bank in the idle state, tRP still applies.
10. A command other than NOP should not be issued to the same bank while a burst READ or burst WRITE with auto precharge is enabled.
11. The new READ or WRITE command could be auto precharge enabled or auto precharge disabled.
12. A WRITE command can be issued after the completion of the READ burst; otherwise, a BST must be issued to end the READ prior to asserting a WRITE command.
13. Not bank-specific. The BST command affects the most recent READ/WRITE burst started by the most recent READ/WRITE command, regardless of bank.
14. A READ command can be issued after completion of the WRITE burst; otherwise, a BST must be used to end the WRITE prior to asserting another READ command.

Table 6. Current State Bank n - Command to Bank m

Notes 1 – 6 apply to all parameters and conditions

Current State of Bank n	Command to Bank m	Operation	Next State for Bank m	Note
Any	NOP	Continue previous operation	Current state of bank m	
Idle	Any	Any command supported to bank m	-	7
Row activating, Active or precharging	ACTIVATE	Select and activate row in bank m	Active	8
	READ	Select column and start READ burst from bank m	Reading	9
	WRITE	Select column and start WRITE burst to bank m	Writing	9
	PRECHARGE	Deactivate row(s) in bank or banks	Precharging	10
	MRR	READ value from mode register	Idle MR reading or active MR reading	11, 12, 13
	BST	READ or WRITE burst terminates an ongoing READ/WRITE from/to bank m	Active	7
Reading (auto precharge disabled)	READ	Select column and start READ burst from bank m	Reading	9
	WRITE	Select column and start WRITE burst to bank m	Writing	9, 14
	ACTIVATE	Select and activate row in bank m	Active	
	PRECHARGE	Deactivate row(s) in bank or banks	Precharging	10
Writing (auto precharge disabled)	READ	Select column and start READ burst from bank m	Reading	9, 15
	WRITE	Select column and start WRITE burst to bank m	Writing	9
	ACTIVATE	Select and activate row in bank m	Active	
	PRECHARGE	Deactivate row(s) in bank or banks	Precharging	10
Reading with auto precharge	READ	Select column and start READ burst from bank m	Reading	9, 16
	WRITE	Select column and start WRITE burst to bank m	Writing	9, 14, 16
	ACTIVATE	Select and activate row in bank m	Active	
	PRECHARGE	Deactivate row(s) in bank or banks	Precharging	10
Writing with auto precharge	READ	Select column and start READ burst from bank m	Reading	9, 15, 16
	WRITE	Select column and start WRITE burst to bank m	Writing	9, 16
	ACTIVATE	Select and activate row in bank m	Active	
	PRECHARGE	Deactivate row(s) in bank or banks	Precharging	10
Power-on	MRW RESET	Begin device auto initialization	Resetting	17, 18
Resetting	MRR	Read value from mode register	Resetting MR reading	

Notes:

1. This table applies when: the previous state was self refresh or power-down; after tXSR or tXP has been met; and both CKEn -1 and CKEn are HIGH.
2. All states and sequences not shown are illegal or reserved.
3. Current state definitions:
   Idle: The bank has been precharged and tRP has been met.
   Active: A row in the bank has been activated, tRCD has been met, no data bursts or accesses and no register accesses are in progress.
   Read: A READ burst has been initiated with auto precharge disabled and the READ has not yet terminated or been terminated.
   Write: A WRITE burst has been initiated with auto precharge disabled and the WRITE has not yet terminated or been terminated.
4. Refresh, self refresh, and MRW commands can only be issued when all banks are idle.
5. A BST command cannot be issued to another bank; it applies only to the bank represented by the current state.

6. The states listed below must not be interrupted by any executable command. NOP commands must be applied during each clock cycle while in these states:
   Idle MRR: Starts with registration of the MRR command and ends when tMRR has been met. After tMRR is met, the device is in the all banks idle state.
   Reset MRR: Starts with registration of the MRR command and ends when tMRR has been met. After tMRR is met, the device is in the all banks idle state.
   Active MRR: Starts with registration of the MRR command and ends when tMRR has been met. After tMRR is met, the bank is in the active state.
   MRW: Starts with registration of the MRW command and ends when tMRW has been met. After tMRW is met, the device is in the all banks idle state.
7. BST is supported only if a READ or WRITE burst is ongoing.
8. tRRD must be met between the ACTIVATE command to bank n and any subsequent ACTIVATE command to bank m.
9. READs or WRITEs listed in the command column include READs and WRITEs with or without auto precharge enabled.
10. A command other than NOP should not be issued to the same bank while a burst READ or burst WRITE with auto precharge is enabled.
11. MRR is supported in the row-activating state.
12. MRR is supported in the precharging state.
13. The next state for bank m depends on the current state of bank m (idle, row-activating, precharging, or active).
14. A WRITE command can be issued after the completion of the READ burst; otherwise a BST must be issued to end the READ prior to asserting a WRITE command.
15. A READ command can be issued after the completion of the WRITE burst; otherwise, a BST must be issued to end the WRITE prior to asserting another READ command.
16. A READ with auto precharge enabled or a WRITE with auto precharge enabled can be followed by any valid command to other banks provided that the timing restrictions in the PRECHARGE and Auto Precharge clarification table are met.
17. Not bank-specific; requires that all banks are idle and no bursts are in progress.
18. RESET command is achieved through MODE REGISTER WRITE command.

Table 7. DM Truth Table

Functional Name	DM	DQ	Note
Write enable	L	Valid	1
Write inhibit	H	X	1

Notes:
1. Used to mask write data, and is provided simultaneously with the corresponding input data.

Functional Description

This 256Mb Mobile LPDDR2 is a high-speed SDRAM internally configured as a 4 bank memory device. LPDDR2 devices use a double data rate architecture on the command/address (CA) bus to reduce the number of input pins in the system. The 10-bit CA bus is used to transmit command, address, and bank information. Each command uses one clock cycle, during which command information is transferred on both the rising and falling edges of the clock.

LPDDR2-S4 devices use a double data rate architecture on the DQ pins to achieve highspeed operation. The double data rate architecture is essentially a 4n prefetch architecture with an interface designed to transfer two data bits per DQ every clock cycle at the I/O pins. A single read or write access for the LPDDR2-S4 effectively consists of a single 4n-bit-wide, one-clock-cycle data transfer at the internal SDRAM core and four corresponding n-bit-wide, one-half-clock-cycle data transfers at the I/O pins.

Read and write accesses are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence.

Accesses begin with the registration of an ACTIVATE command followed by a READ or WRITE command. The address and BA bits registered coincident with the ACTIVATE command are used to select the row and bank to be accessed. The address bits registered coincident with the READ or WRITE command are used to select the bank and the starting column location for the burst access.

● Power-Up and Initialization

The following sequence must be used to power up the device. Unless specified otherwise, this procedure is mandatory. Power-up and initialization by means other than those specified will result in undefined operation.

1. Voltage Ramp

While applying power (after Ta), CKE must be held LOW ($\leqq 0.2 \times$ VDDCA), and all other inputs must be between VILmin and VIHmax. The device outputs remain at High-Z while CKE is held LOW.

On or before the completion of the voltage ramp (Tb), CKE must be held LOW. DQ, DM, DQS, and DQS# voltage levels must be between VSSQ and VDDQ during voltage ramp to avoid latchup. CK, CK#, CS#, and CA input levels must be between VSSCA and VDDCA during voltage ramp to avoid latchup.

The following conditions apply for voltage ramp:

- Ta is the point when any power supply first reaches 300mV.
- Noted conditions apply between Ta and power-down (controlled or uncontrolled).
- Tb is the point at which all supply and reference voltages are within their defined operating ranges.
- Power ramp duration tINIT0 (Tb - Ta) must not exceed 20ms.
- For supply and reference voltage operating conditions, see the Recommended DC Operating Conditions table.
- The voltage difference between any of VSS, VSSQ, and VSSCA pins must not exceed 100mV.

Voltage Ramp Completion

After Ta is reached:

- VDD1 must be greater than VDD2 - 200mV
- VDD1 and VDD2 must be greater than VDDCA - 200mV
- VDD1 and VDD2 must be greater than VDDQ - 200mV
- VREF must always be less than all other supply voltages

Beginning at Tb, CKE must remain LOW for at least tINIT1 = 100ns, after which CKE can be asserted HIGH. The clock must be stable at least tINIT2 = 5 $\times$ tCK prior to the first CKE LOW-to-HIGH transition (Tc). CKE, CS#, and CA inputs must observe setup and hold requirements (tIS, tIH) with respect to the first rising clock edge (and to subsequent falling and rising edges).

If any MRRs are issued, the clock period must be within the range defined for tCKb (18ns to 100ns). MRWs can be issued at normal clock frequencies as long as all AC timings are met. Some AC parameters (for example, tDQSCK) could have relaxed timings (such as tDQSCKb) before the system is appropriately configured. While keeping CKE HIGH, NOP commands must be issued for at least tINIT3 = 200us (Td).

2. RESET Command

After tINIT3 is satisfied, the MRW RESET command must be issued (Td). An optional PRECHARGE ALL command can be issued prior to the MRW RESET command. Wait at least tINIT4 while keeping CKE asserted and issuing NOP commands.

3. MRRs and Device Auto Initialization (DAI) Polling

After tINIT4 is satisfied (Te), only MRR commands and power-down entry/exit commands are supported. After Te, CKE can go LOW in alignment with power-down entry and exit specifications.

The MRR command can be used to poll the DAI bit, which indicates when device auto initialization is complete; otherwise, the controller must wait a minimum of tINIT5, or until the DAI bit is set, before proceeding.

Because the memory output buffers are not properly configured by Te, some AC parameters must use relaxed timing specifications before the system is appropriately configured.

After the DAI bit (MR0, DAI) is set to zero by the memory device (DAI complete), the device is in the idle state (Tf). DAI status can be determined by issuing the MRR command to MR0.

The device sets the DAI bit no later than tINIT5 after the RESET command. The controller must wait at least tINIT5 or until the DAI bit is set before proceeding.

4. ZQ Calibration

After tINIT5 (Tf), the MRW initialization calibration (ZQ calibration) command can be issued to the memory (MR10). This command is used to calibrate output impedance over process, voltage, and temperature. In systems where more than one Mobile LPDDR2 device exists on the same bus, the controller must not overlap MRW ZQ calibration commands. The device is ready for normal operation after tZQINIT.

5. Normal Operation

After (Tg), MRW commands must be used to properly configure the memory (output buffer drive strength, latencies, etc.). Specifically, MR1, MR2, and MR3 must be set to configure the memory for the target frequency and memory configuration.

After the initialization sequence is complete, the device is ready for any valid command.

After Tg, the clock frequency can be changed using the procedure described in Input Clock Frequency Changes and Clock Stop with CKE HIGH.

Figure 4. Power Ramp and Initialization Sequence

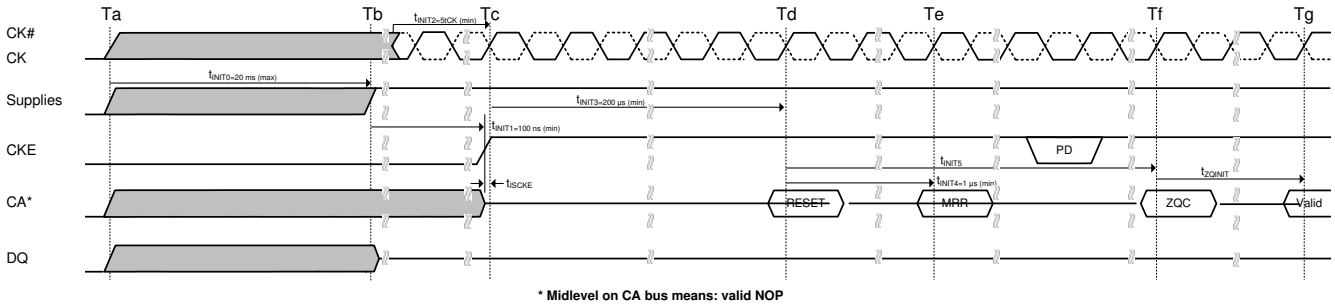


Table 8. Initialization Timing Parameters

Parameter	Value		Unit	Comment
	Min	Max		
t_{INIT0}	-	20	ms	Maximum voltage ramp time
t_{INIT1}	100	-	ns	Minimum CKE LOW time after completion of voltage ramp
t_{INIT2}	5	-	t_{CK}	Minimum stable clock before first CKE HIGH
t_{INIT3}	200	-	us	Minimum idle time after first CKE assertion
t_{INIT4}	1	-	us	Minimum idle time after RESET command
t_{INIT5}	-	10	us	Maximum duration of device auto initialization
t_{ZQINIT}	1	-	us	ZQ initial calibration (S4 devices only)
t_{CKb}	18	100	ns	Clock cycle time during boot

● Initialization After RESET (Without Voltage Ramp)

If the RESET command is issued before or after the power-up initialization sequence, the reinitialization procedure must begin at Td.

● Power-Off

While powering off, CKE must be held LOW ($\leqq$0.2 $\times$ VDDCA); all other inputs must be between VILmin and VIHmax. The device outputs remain at High-Z while CKE is held LOW.
DQ, DM, DQS, and DQS# voltage levels must be between VSSQ and VDDQ during the power-off sequence to avoid latchup. CK, CK#, CS#, and CA input levels must be between VSSCA and VDDCA during the power-off sequence to avoid latchup.
Tx is the point where any power supply drops below the minimum value specified in the Recommended DC Operating Conditions table.
Tz is the point where all power supplies are below 300mV. After Tz, the device is powered off.
Required Power Supply Conditions Between Tx and Tz:

- VDD1 must be greater than VDD2 - 200mV
- VDD1 must be greater than VDDCA - 200mV
- VDD1 must be greater than VDDQ - 200mV
- VREF must always be less than all other supply voltages

The voltage difference between VSS, VSSQ, and VSSCA must not exceed 100mV.
For supply and reference voltage operating conditions, see Recommended DC Operating Conditions table.

Uncontrolled Power-Off

When an uncontrolled power-off occurs, the following conditions must be met:

- At Tx, when the power supply drops below the minimum values specified in the Recommended DC Operating Conditions table, all power supplies must be turned off and all power-supply current capacity must be at zero, except for any static charge remaining in the system.
- After Tz (the point at which all power supplies first reach 300mV), the device must power off. The time between Tx and Tz must not exceed tPOFF. During this period, the relative voltage between power supplies is uncontrolled. VDD1 and VDD2 must decrease with a slope lower than 0.5 V/us between Tx and Tz.

An uncontrolled power-off sequence can occur a maximum of 400 times over the life of the device.

Table 9. Power-Off Timing

Parameter	Symbol	Min	Max	Unit
Maximum power-off ramp time	t_{POFF}	-	2	sec

● Mode Register Definition

The MRR command is used to read from a register. The MRW command is used to write to a register. An “R” in the access column of the mode register assignment table indicates read-only; a “W” indicates write-only; “R/W” indicates read or write capable or enabled.

Table 10. Mode Register Assignments

MR#	MA[7:0]	Function	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
0	00h	Device info	R	RFU			RZQI		DNVI	DI	DAI
1	01h	Device feature 1	W	nWR (for AP)			WC	BT	BL		
2	02h	Device feature 2	W	RFU				RL and WL			
3	03h	I/O config-1	W	RFU				DS			
4	04h	SDRAM refresh rate	R	TUF	RFU				Refresh rate		
5	05h	Basic config-1	R	LPDDR2 Manufacturer ID							
6	06h	Basic config-2	R	Revision ID1							
7	07h	Basic config-3	R	Revision ID2							
8	08h	Basic config-4	R	I/O width		Density				Type	
9	09h	Test mode	W	Vendor-specific test mode							
10	0Ah	I/O calibration	W	Calibration code							
11-15	0Bh-0Fh	Reserved	-	RFU							
16	10h	PASR_Bank	W	Bank mask							
17	11h	Do not use	W	RFU							
18-19	12h-13h	Reserved	-	RFU							
20-31	14h-1Fh	RFU									
32	20h	DQ calibration pattern A	R	See “DQ Calibration”							
33-39	21h-27h	Do not use									
40	28h	DQ calibration pattern B	R	See “DQ Calibration”							
41-47	29h-2Fh	Do not use									
48-62	30h-3Eh	Reserved	-	RFU							
63	3Fh	RESET	W	X							
64-126	40h-7Eh	Reserved	-	RFU							
127	7Fh	Do not use									
128-190	80h-BEh	Reserved for vendor use		RFU							
191	BFh	Do not use									
192-254	C0h-FEh	Reserved for vendor use		RFU							
255	FFh	Do not use									

Notes:

1. RFU bits must be set to 0 during MRW.
2. RFU bits must be read as 0 during MRR.
3. For READs to a write-only or RFU register, DQS will be toggled and undefined data is returned.
4. RFU mode registers must not be written.
5. WRITEs to read-only registers must have no impact on the functionality of the device.

Table 11. MR0 Device Information

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
RFU			RZQI (Optional)		DNVI	DI	DAI

DAI (Device Auto-Initialization Status)	Read-only	OP0	0b: DAI complete 1b: DAI still in progress
DI (Device Information)	Read-only	OP1	0b: SDRAM
DNVI (Data Not Valid Information)	Read-only	OP2	0b: DNV not supported
RZQI (Built in Self Test for RZQ Information)	Read-only	OP[4:3]	00b: ZQ self test not supported 01b: ZQ-pin may connect to V_{DDCA} or float 10b: ZQ-pin may short to GND 11b: ZQ-pin self test completed, no error condition detected (ZQ-pin may not connect to V_{DD} or float nor short to GND)

Notes:
1. RZQI, if supported, will be set upon completion of the MRW ZQ Initialization Calibration command.
2. If ZQ is connected to V_{DDCA} to set default calibration, OP[4:3] shall be set to 01. If ZQ is not connected to V_{DDCA}, either OP[4:3]=01 or OP[4:3]=10 might indicate a ZQ-pin assembly error. It is recommended that the assembly error is corrected.
3. In the case of possible assembly error (either OP[4:3]=01 or OP[4:3]=10 per Note 4), the LPDDR2 device will default to factory trim settings for RON, and will ignore ZQ calibration commands. In either case, the system may not function as intended.
4. In the case of the ZQ self-test returning a value of 11b, this result indicates that the device has detected a resistor connection to the ZQ pin. However, this result cannot be used to validate the ZQ resistor value or that the ZQ resistor tolerance meets the specified limits (i.e. 240-ohm +/-1%).

Table 12. MR1 Device Information

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
nWR (for AP)			WC	BT	BL		

BL	Write-only	OP[2:0]	010b: BL4 (default) 011b: BL8 100b: BL16 All others: reserved
BT	Write-only	OP3	0b: Sequential (default) 1b: Interleaved
WC	Write-only	OP4	0b: Wrap (default) 1b: No wrap
nWR = number of tWR clock cycles	Write-only	OP[7:5][1]	001b: nWR=3 (default) 010b: nWR=4 011b: nWR=5 100b: nWR=6 101b: nWR=7 110b: nWR=8 All others: reserved

Notes:
1. The programmed value in nWR register is the number of clock cycles that determines when to start internal precharge operation for a WRITE burst with AP enabled. It is determined by RU (t_{WR}/t_{CK}).

Table 13. Burst Sequence by BL, BT, and WC

BL	BT	C3	C2	C1	C0	WC	Burst Cycle Number and Burst Address Sequence															
							1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
4	Any	X	X	0b	0b	W	0	1	2	3												
		X	X	1b	0b		2	3	0	1												
	Any	X	X	X	0b	NW	y	y_{+1}	y_{+2}	y_{+3}												
8	Seq	X	0b	0b	0b	W	0	1	2	3	4	5	6	7								
		X	0b	1b	0b		2	3	4	5	6	7	0	1								
		X	1b	0b	0b		4	5	6	7	0	1	2	3								
		X	1b	1b	0b		6	7	0	1	2	3	4	5								
	Int	X	0b	0b	0b		0	1	2	3	4	5	6	7								
		X	0b	1b	0b		2	3	0	1	6	7	4	5								
		X	1b	0b	0b		4	5	6	7	0	1	2	3								
		X	1b	1b	0b		6	7	4	5	2	3	0	1								
	Any	X	X	X	0b	NW	Illegal (not supported)															
16	Seq	0b	0b	0b	0b	W	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
		0b	0b	1b	0b		2	3	4	5	6	7	8	9	A	B	C	D	E	F	0	1
		0b	1b	0b	0b		4	5	6	7	8	9	A	B	C	D	E	F	0	1	2	3
		0b	1b	1b	0b		6	7	8	9	A	B	C	D	E	F	0	1	2	3	4	5
		1b	0b	0b	0b		8	9	A	B	C	D	E	F	0	1	2	3	4	5	6	7
		1b	0b	1b	0b		A	B	C	D	E	F	0	1	2	3	4	5	6	7	8	9
		1b	1b	0b	0b		C	D	E	F	0	1	2	3	4	5	6	7	8	9	A	B
		1b	1b	1b	0b		E	F	0	1	2	3	4	5	6	7	8	9	A	B	C	D
	Int	X	X	X	0b		Illegal (not supported)															
	Any	X	X	X	0b	NW	Illegal (not supported)															

Notes:
1. C0 input is not present on CA bus. It is implied zero.
2. “W” means Wrap, “NW” means No Wrap, “Any” means Sequential and interleaved.”Seq” means sequential and “Int” means interleaved.
3. For No-wrap (NW), BL4, the burst shall not cross the page boundary and shall not cross sub-page boundary. The variable y may start at any address with C0 equal to 0 and may not start at any address in Table. Non Wrap Restrictions below for the respective density and bus width combinations.

Table 14. No-Wrap Restrictions

Width	256Mb
Cannot cross full-page boundary	
x32	FE, FF, 00, 01
Cannot cross sub-page boundary	
x32	None

Notes:
1. No-wrap BL = 4 data orders shown are prohibited.

Table 15. MR2 Device Feature 2

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
RFU				RL and WL			

RL and WL	Write-only	OP[3:0]	0001b: RL3/WL1 (default) 0010b: RL4/WL2 0011b: RL5/WL2 0100b: RL6/WL3 0101b: RL7/WL4 0110b: RL8/WL4 All others: Reserved

Table 16. MR3 I/O Configuration 1

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
RFU				DS			

DS	Write-only	OP[3:0]	0000b: Reserved 0001b: 34.3 ohm typical 0010b: 40 ohm typical (default) 0011b: 48 ohm typical 0100b: 60 ohm typical 0101b: Reserved 0110b: 80 ohm typical 0111b: 120 ohm typical All others: Reserved

Table 17. MR4 Device Temperature

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
TUF	RFU				SDRAM refresh rate		

SDRAM refresh rate	Read-only	OP[2:0]	000b: Reserved 001b: 4 × t_{REFI}, 4 × t_{REFI}pb, 4 × t_{REFW} 010b: 2 × t_{REFI}, 2 × t_{REFI}pb, 2 × t_{REFW} 011b: 1 × t_{REFI}, 1 × t_{REFI}pb, 1 × t_{REFW} (≦85°C) 100b: Reserved 101b: 0.25 × t_{REFI}, 0.25 × t_{REFI}pb, 0.25 × t_{REFW}, do not derate SDRAM AC timing 110b: 0.25 × t_{REFI}, 0.25 × t_{REFI}pb, 0.25 × t_{REFW}, derate SDRAM AC timing 111b: SDRAM high temperature operating limit exceeded
Temperature update flag	Read-only	OP7	0b: OP[2:0] value has not changed since last read of MR4 1b: OP[2:0] value has changed since last read of MR4

Notes:
1. A Mode Register Read from MR4 will reset OP7 to 0.
2. OP7 is reset to 0 at power-up.
3. If OP2 = 1, the device temperature is greater than 85°C.
4. OP7 is set to 1 if OP[2:0] has changed at any time since the last read of MR4.
5. The device might not operate properly when OP[2:0] = 000b or 111b.
6. For specified operating temperature range and maximum operating temperature, refer to the Operating Temperature Range table.
7. LPDDR2 devices must be derated by adding 1.875ns to the following core timing parameters: t_{RCD}, t_{RC}, t_{RAS}, t_{RP}, and t_{RRD}. The t_{DQSCK} parameter must be derated as specified in AC Timing. Prevailing clock frequency specifications and related setup and hold timings remain unchanged.
8. The recommended frequency for reading MR4 is provided in Temperature Sensor.

Table 18. MR5 LPDDR2 Manufacturer ID

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
LPDDR2 Manufacturer ID							

Manufacturer ID	Read-only	OP[7:0]	0000 0100b: Etron

Table 19. MR8 Basic Configuration 4

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
I/O width		Density				Type	

Type	Read-only	OP[1:0]	00b: S4 SDRAM
Density	Read-only	OP[5:2]	0010b: 256Mb
I/O width	Read-only	OP[7:6]	00b: x32

Table 20. MR10 ZQ Calibration

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Calibration Code							

Calibration Code	Write Only		1111 1111b: Calibration command after initialization 1010 1011b: Long Calibration 0101 0110b: Short Calibration 1100 0011b: ZQ Reset others: reserved

Notes:
1. Host processor must not write MR10 with reserved values.
2. The device ignores calibration commands when a reserved value is written into MR10.
3. See AC timing table for the calibration latency.
4. If ZQ is connected to V_{SSCA} through RZQ, either the ZQ calibration function (see the section of "Mode Register Write ZQ Calibration Command") or default calibration (through the ZQRESET command) is supported. If ZQ is connected to V_{DDCA}, the device operates with default calibration, and ZQ calibration commands are ignored. In both cases, the ZQ connection shall not change after power is applied to the device.

Table 21. MR16 Bank Mask

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
RFU				Bank Mask			

Bank Mask	Write-only	OP[3:0]	0b: refresh enable to the bank (default) 1b: refresh blocked (masked)

OP	Bank Mask	4-Bank
0	XXXXXXX1	Bank 0
1	XXXXXX1X	Bank 1
2	XXXXX1XX	Bank 2
3	XXXX1XXX	Bank 3

● ACTIVATE Command

The ACTIVATE command is issued by holding CS# LOW, CA0 LOW, and CA1 HIGH at the rising edge of the clock. The bank addresses BA0 - BA1 are used to select the desired bank. Row addresses are used to determine which row to activate in the selected bank. The ACTIVATE command must be applied before any READ or WRITE operation can be executed. The device can accept a READ or WRITE command at tRCD after the ACTIVATE command is issued. After a bank has been activated, it must be precharged before another ACTIVATE command can be applied to the same bank. The bank active and precharge times are defined as tRAS and tRP, respectively. The minimum time interval between successive ACTIVATE commands to the same bank is determined by the RAS cycle time of the device (tRC). The minimum time interval between ACTIVATE commands to different banks is tRRD.

● Read and Write Access Modes

After a bank is activated, a READ or WRITE command can be issued with CS# LOW, CA0 HIGH, and CA1 LOW at the rising edge of the clock. CA2 must also be defined at this time to determine whether the access cycle is a READ operation (CA2 HIGH) or a WRITE operation (CA2 LOW). A single READ or WRITE command initiates a burst READ or burst WRITE operation on successive clock cycles.
A new burst access must not interrupt the previous 4-bit burst operation when BL = 4. When BL = 8 or BL = 16, READs can be interrupted by READs and WRITEs can be interrupted by WRITEs, provided that the interrupt occurs on a 4-bit boundary and that tCCD is met.

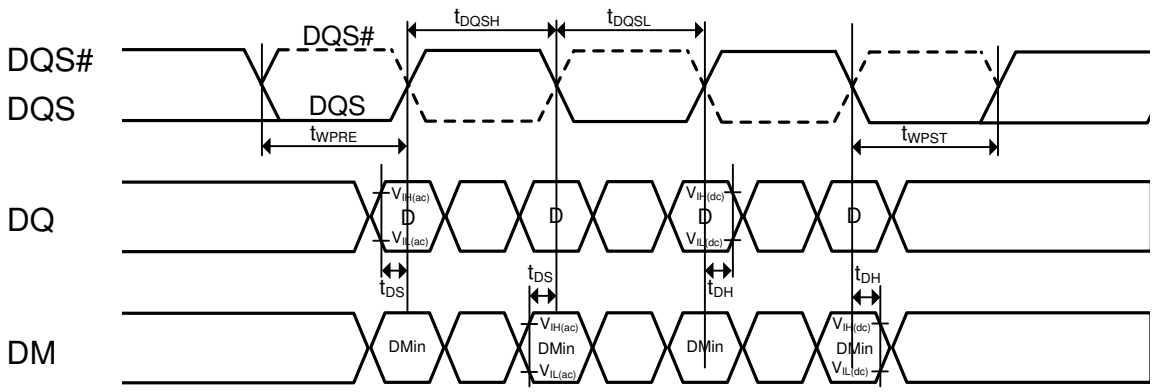
- Burst READ Command

The burst READ command is initiated with CS# LOW, CA0 HIGH, CA1 LOW, and CA2 HIGH at the rising edge of the clock. The command address bus inputs, CA5r – CA6r and CA1f – CA9f, determine the starting column address for the burst. The read latency (RL) is defined from the rising edge of the clock on which the READ command is issued to the rising edge of the clock from which the tDQSCK delay is measured. The first valid data is available RL × tCK + tDQSCK + tDQSQ after the rising edge of the clock when the READ command is issued. The data strobe output is driven LOW tRPRE before the first valid rising strobe edge. The first bit of the burst is synchronized with the first rising edge of the data strobe. Each subsequent data-out appears on each DQ pin, edgealigned with the data strobe. The RL is programmed in the mode registers.
Pin input timings for the data strobe are measured relative to the crosspoint of DQS and its complement, DQS#.

- Burst WRITE Command

The burst WRITE command is initiated with CS# LOW, CA0 HIGH, CA1 LOW, and CA2 LOW at the rising edge of the clock. The command address bus inputs, CA5r – CA6r and CA1f – CA9f, determine the starting column address for the burst. Write latency (WL) is defined from the rising edge of the clock on which the WRITE command is issued to the rising edge of the clock from which the tDQSS delay is measured. The first valid data must be driven WL × tCK + tDQSS from the rising edge of the clock from which the WRITE command is issued. The data strobe signal (DQS) must be driven LOW tWPRE prior to data input. The burst cycle data bits must be applied to the DQ pins tDS prior to the associated edge of the DQS and held valid until tDH after that edge. Burst data is sampled on successive edges of the DQS until the 4-, 8-, or 16-bit burst length is completed. After a burst WRITE operation, tWR must be satisfied before a PRECHARGE command to the same bank can be issued.
Pin input timings are measured relative to the crosspoint of DQS and its complement, DQS#.

Figure 5. Data input (write) timing



● BURST TERMINATE Command

The BURST TERMINATE (BST) command is initiated with CS# LOW, CA0 HIGH, CA1 HIGH, CA2 LOW, and CA3 LOW at the rising edge of the clock. A BST command can only be issued to terminate an active READ or WRITE burst. Therefore, a BST command can only be issued up to and including BL/2 - 1 clock cycles after a READ or WRITE command.

The effective burst length of a READ or WRITE command truncated by a BST command is as follows:

- Effective burst length = 2 × (number of clock cycles from the READ or WRITE command to the BST command).
- If a READ or WRITE burst is truncated with a BST command, the effective burst length of the truncated burst should be used for BL when calculating the minimum READ to WRITE or WRITE to READ delay.
- The BST command only affects the most recent READ or WRITE command. The BST command truncates an ongoing READ burst RL × tCK + tDQSCK + tDQSQ after the rising edge of the clock where the BST command is issued. The BST command truncates an ongoing WRITE burst WL × tCK + tDQSS after the rising edge of the clock where the BST command is issued.
- The 4-bit prefetch architecture enables BST command assertion on even clock cycles following a WRITE or READ command. The effective burst length of a READ or WRITE command truncated by a BST command is thus an integer multiple of four.

● PRECHARGE Command

The PRECHARGE command is used to precharge or close a bank that has been activated. The PRECHARGE command is initiated with CS# LOW, CA0 HIGH, CA1 HIGH, CA2 LOW, and CA3 HIGH at the rising edge of the clock. The PRECHARGE command can be used to precharge each bank independently or all banks simultaneously. For 4-bank devices, the AB flag and bank address bits BA0 and BA1 are used to determine which bank(s) to precharge. The precharged bank(s) will be available for subsequent row access tRPab after an all bank PRECHARGE command is issued, or tRPpb after a single-bank PRECHARGE command is issued.

For 4-bank devices, tRPab is equal to tRPpb.

ACTIVATE to PRECHARGE timing is shown in ACTIVATE Command.

Table 22. Bank selection for Precharge by address bits

AB (CA4r)	BA1 (CA8r)	BA0 (CA7r)	Precharged Bank(s) 4-bank device
0	0	0	Bank 0 only
0	0	1	Bank 1 only
0	1	0	Bank 2 only
0	1	1	Bank 3 only
1	X	X	All Banks

● READ Burst Followed by PRECHARGE

For the earliest possible precharge, the PRECHARGE command can be issued BL/2 clock cycles after a READ command. A new bank ACTIVATE command can be issued to the same bank after the row precharge time (tRP) has elapsed. A PRECHARGE command cannot be issued until after tRAS is satisfied.

The minimum READ-to-PRECHARGE time (tRTP) must also satisfy a minimum analog time from the rising clock edge that initiates the last 4-bit prefetch of a READ command. tRTP begins BL/2 - 2 clock cycles after the READ command.

If the burst is truncated by a BST command, the effective BL value is used to calculate when tRTP begins.

● WRITE Burst Followed by PRECHARGE

For WRITE cycles, a WRITE recovery time (tWR) must be provided before a PRECHARGE command can be issued. tWR delay is referenced from the completion of the burst WRITE. The PRECHARGE command must not be issued prior to the tWR delay. For WRITE to PRECHARGE timings see PRECHARGE and Auto Precharge Clarification table.
These devices write data to the array in prefetch quadruples (prefetch = 4). An internal WRITE operation can only begin after a prefetch group has been completely latched.
The minimum WRITE-to-PRECHARGE time for commands to the same bank is WL + BL/2 + 1 + RU (tWR/tCK) clock cycles. For an untruncated burst, BL is the value from the Mode Register. For an truncated burst, BL is the effective burst length.

● Auto Precharge

Before a new row can be opened in an active bank, the active bank must be precharged using either the PRECHARGE command or the auto precharge function. When a READ or WRITE command is issued to the device, the auto precharge bit (AP) can be set to enable the active bank to automatically begin precharge at the earliest possible moment during the burst READ or WRITE cycle.
If AP is LOW when the READ or WRITE command is issued, then normal READ or WRITE burst operation is executed and the bank remains active at the completion of the burst.
If AP is HIGH when the READ or WRITE command is issued, the auto precharge function is engaged. This feature enables the PRECHARGE operation to be partially or completely hidden during burst READ cycles (dependent upon READ or WRITE latency), thus improving system performance for random data access.

● READ Burst with Auto Precharge

If AP (CA0f) is HIGH when a READ command is issued, the READ with auto precharge function is engaged.
These devices start an auto precharge on the rising edge of the clock BL/2 or BL/2 - 2 + RU(tRTP/tCK) clock cycles later than the READ with auto precharge command, whichever is greater. For auto precharge calculations see see PRECHARGE and Auto Precharge Clarification table.
Following an auto precharge operation, an ACTIVATE command can be issued to the same bank if the following two conditions are satisfied simultaneously:
- The RAS precharge time (tRP) has been satisfied from the clock at which the auto precharge begins.
- The RAS cycle time (tRC) from the previous bank activation has been satisfied.

● WRITE Burst with Auto Precharge

If AP (CA0f) is HIGH when a WRITE command is issued, the WRITE with auto precharge function is engaged. The device starts an auto precharge at the clock rising edge tWR cycles after the completion of the burst WRITE.
Following a WRITE with auto precharge, an ACTIVATE command can be issued to the same bank if the following two conditions are met:
- The RAS precharge time (tRP) has been satisfied from the clock at which the auto precharge begins.
- The RAS cycle time (tRC) from the previous bank activation has been satisfied.

Table 23. PRECHARGE and Auto Precharge Clarification

From Command	To Command	Minimum Delay Between Commands	Unit	Note
READ	PRECHARGE to same bank as READ	BL/2 + max (2, RU(t_{RTP}/t_{CK})) - 2	t_{CK}	1
	PRECHARGE ALL	BL/2 + max (2, RU(t_{RTP}/t_{CK})) - 2	t_{CK}	1
BST (for READ)	PRECHARGE to same bank as READ	1	t_{CK}	1
	PRECHARGE ALL	1	t_{CK}	1
READ w/AP	PRECHARGE to same bank as READ w/AP	BL/2 + max (2, RU(t_{RTP}/t_{CK})) - 2	t_{CK}	1,2
	PRECHARGE ALL	BL/2 + max (2, RU(t_{RTP}/t_{CK})) - 2	t_{CK}	1
	ACTIVATE to same bank as READ w/AP	BL/2 + max (2, RU(t_{RTP}/t_{CK})) - 2 + RU(t_{RPpb}/t_{CK})	t_{CK}	1
	WRITE or WRITE w/AP (same bank)	Illegal	t_{CK}	3
	WRITE or WRITE w/AP (different bank)	RL + BL/2 + RU($t_{DQSCKmax}/t_{CK}$) - WL + 1	t_{CK}	3
	READ or READ w/AP (same bank)	Illegal	t_{CK}	3
	READ or READ w/AP (different bank)	BL/2	t_{CK}	3
WRITE	PRECHARGE to same bank as WRITE	WL + BL/2 + RU(t_{WR}/t_{CK}) + 1	t_{CK}	1
	PRECHARGE ALL	WL + BL/2 + RU(t_{WR}/t_{CK}) + 1	t_{CK}	1
BST (for WRITE)	PRECHARGE to same bank as WRITE	WL + RU(t_{WR}/t_{CK}) + 1	t_{CK}	1
	PRECHARGE ALL	WL + RU(t_{WR}/t_{CK}) + 1	t_{CK}	1
WRITE w/AP	PRECHARGE to same bank as WRITE w/AP	WL + BL/2 + RU(t_{WR}/t_{CK}) + 1	t_{CK}	1,2
	PRECHARGE ALL	WL + BL/2 + RU(t_{WR}/t_{CK}) + 1	t_{CK}	1
	ACTIVATE to same bank as WRITE w/AP	WL + BL/2 + RU(t_{WR}/t_{CK}) + 1 + RU(t_{RPpb}/t_{CK})	t_{CK}	1
	WRITE or WRITE w/AP (same bank)	Illegal	t_{CK}	3
	WRITE or WRITE w/AP (different bank)	BL/2	t_{CK}	3
	READ or READ w/AP (same bank)	Illega	t_{CK}	3
	READ or READ w/AP (different bank)	WL + BL/2 + RU(t_{WTR}/t_{CK}) +1	t_{CK}	3
PRECHARGE	PRECHARGE to same bank as PRECHARG	1	t_{CK}	1
	PRECHARGE ALL	1	t_{CK}	1
PRECHARGE ALL	PRECHARG	1	t_{CK}	1
	PRECHARGE ALL	1	t_{CK}	1

Notes:

1. For a given bank, the PRECHARGE period should be counted from the latest PRECHARGE Command, either a one-bank PRECHARGE or PRECHARGE ALL, issued to that bank. The PRECHARGE period is satisfied after tRP, depending on the latest PRECHARGE command issued to that bank.
2. Any command issued during the specified minimum delay time is illegal.
3. After READ with auto precharge, seamless READ operations to different banks are supported. After WRITE with auto precharge, seamless WRITE operations to different banks are supported. READ with auto precharge and WRITE with auto precharge must not be interrupted or truncated.

● REFRESH Command

The REFRESH command is initiated with CS# LOW, CA0 LOW, CA1 LOW, CA2 HIGH and CA3 HIGH at the rising edge of the clock.
A REFRESH command (REF) issues a REFRESH command to all banks. All banks must be idle when REF is issued (for instance, by issuing a PRECHARGE ALL command prior to issuing REFRESH command). The REF command must not be issued to the device until the following conditions have been met:
- tRFC has been satisfied following the prior REF command.
- tRP has been satisfied following the prior PRECHARGE commands.

After REFRESH cycle has completed, all banks will be idle. After issuing REF:
- tRFC latency must be satisfied before issuing an ACTIVATE command
- tRFC latency must be satisfied before issuing a REF command.

Table 24. REFRESH Command Scheduling Separation Requirements

Symbol	Minimum Delay From	To	Note
tRFC	REF	REF	
		ACTIVATE command to any bank	

In the most straightforward implementations, a REFRESH command should be scheduled every tREFI. In this case, self refresh can be entered at any time.
Users may choose to deviate from this regular refresh pattern, for instance, to enable a period in which no refresh is required. As an example, using a 256Mb LPDDR2 device, the user can choose to issue a refresh burst of 4096 REFRESH commands at the maximum supported rate (limited by tREFBW), followed by an extended period without issuing any REFRESH commands, until the refresh window is complete. The maximum supported time without REFRESH commands is calculated as follows: tREFW - (R/8) × tREFBW = tREFW - R × 4 × tRFCab.
For example, a 256Mb device at TC ≦ 85°C can be operated without a refresh for up to 32ms - 4096 × 4 × 90ns ≈ 30ms.
Both the regular and the burst/pause patterns can satisfy refresh requirements if they are repeated in every 32ms window. It is critical to satisfy the refresh requirement in every rolling refresh window during refresh pattern transitions. The supported transition from a burst pattern to a regular distributed pattern. If this transition occurs immediately after the burst refresh phase, all rolling tREFW intervals will meet the minimum required number of REFRESH commands.
The regular refresh pattern starts after the completion of the pause phase of the burst/pause refresh pattern. For several rolling tREFW intervals, the minimum number of REFRESH commands is not satisfied.
Understanding this pattern transition is extremely important, even when only one pattern is employed. In self refresh mode, a regular distributed refresh pattern must be assumed.

- REFRESH Requirements

1. Minimum Number of REFRESH Commands

Mobile LPDDR2 requires a minimum number, R, of REFRESH (REFab) commands within any rolling refresh window (tREFW = 32 ms @ MR4[2:0] = 011 or TC ≦ 85°C). For actual values per density and the resulting average refresh interval (tREFI).
For tREFW and tREFI refresh multipliers at different MR4 settings, see the MR4 Device Temperature (MA[7:0] = 04h) table.

2. Burst REFRESH Limitation

To limit current consumption, a maximum of eight REF commands can be issued in any rolling tREFBW (tREFBW = 4 × 8 × tRFC).

3. REFRESH Requirements and Self Refresh

If any time within a refresh window is spent in self refresh mode, the number of required REFRESH commands in that window is reduced to the following:
R' = RU {tSRF/tREFI} = R – RU {R * tSRF/ tREFW}
Where RU represents the round-up function.

● SELF REFRESH Operation

The SELF REFRESH command can be used to retain data in the array, even if the rest of the system is powered down. When in the self refresh mode, the device retains data without external clocking. The device has a built-in timer to accommodate SELF REFRESH operation. The SELF REFRESH command is executed by taking CKE LOW, CS# LOW, CA0 LOW, CA1 LOW, and CA2 HIGH at the rising edge of the clock.
CKE must be HIGH during the clock cycle preceding a SELF REFRESH command. A NOP command must be driven in the clock cycle following the SELF REFRESH command. After the power-down command is registered, CKE must be held LOW to keep the device in self refresh mode.
Mobile LPDDR2 devices can operate in self refresh mode in both the standard and extended temperature ranges. These devices also manage self refresh power consumption when the operating temperature changes, resulting in the lowest possible power consumption across the operating temperature range.
After the device has entered self refresh mode, all external signals other than CKE are “Don’t Care”. For proper self refresh operation, power supply pins (VDD1, VDD2, VDDQ, and VDDCA) must be at valid levels. VDDQ can be turned off during self refresh. If VDDQ is turned off, VREFDQ must also be turned off. Prior to exiting self refresh, both VDDQ and VREFDQ must be within their respective minimum/maximum operating ranges.
VREFDQ can be at any level between 0 and VDDQ; VREFCA can be at any level between 0 and VDDCA during self refresh.
Before exiting self refresh, VREFDQ and VREFCA must be within specified limits. After entering self refresh mode, the device initiates at least one all-bank REFRESH command internally during tCKESR. The clock is internally disabled during SELF REFRESH operation to save power. The device must remain in self refresh mode for at least tCKESR. The user can change the external clock frequency or halt the external clock one clock after self refresh entry is registered; however, the clock must be restarted and stable before the device can exit SELF REFRESH operation.
Exiting self refresh requires a series of commands. First, the clock must be stable prior to CKE returning HIGH. After the self refresh exit is registered, a minimum delay, at least equal to the self refresh exit interval (tXSR), must be satisfied before a valid command can be issued to the device. This provides completion time for any internal refresh in progress. For proper operation, CKE must remain HIGH throughout tXSR, except during self refresh re-entry. NOP commands must be registered on each rising clock edge during tXSR.
Using self refresh mode introduces the possibility that an internally timed refresh event could be missed when CKE is driven HIGH for exit from self refresh mode. Upon exiting self refresh, at least one REFRESH command (one all-bank command) must be issued before issuing a subsequent SELF REFRESH command.

- Partial Array Self Refresh – Bank Masking

Each bank of LPDDR2 SDRAM can be independently configured whether a self refresh operation is taking place. One mode register unit of 4 bits accessible via MRW command is assigned to program the bank masking status of each bank up to 4 banks. For bank masking bit assignments, see Mode Register 16 (MR16).
The mask bit to the bank controls a refresh operation of entire memory within the bank. If a bank is masked via MRW, a refresh operation to the entire bank is blocked and data retention by a bank is not guaranteed in self refresh mode. To enable a refresh operation to a bank, a coupled mask bit has to be programmed, "unmasked". When a bank mask bit is unmasked, a refresh to a bank is determined by the programmed status of segment mask bits.

● MODE REGISTER READ

The MODE REGISTER READ (MRR) command is used to read configuration and status data from SDRAM mode registers. The MRR command is initiated with CS# LOW, CA0 LOW, CA1 LOW, CA2 LOW, and CA3 HIGH at the rising edge of the clock. The mode register is selected by CA1f – CA0f and CA9r – CA4r. The mode register contents are available on the first data beat of DQ[7:0] after RL × tCK + tDQSCK + tDQSQ and following the rising edge of the clock where MRR is issued. Subsequent data beats contain valid but undefined content, except in the case of the DQ calibration function, where subsequent data beats contain valid content as described in Data Calibration Pattern Description. All DQS are toggled for the duration of the mode register READ burst. The MRR command has a burst length of four. MRR operation (consisting of the MRR command and the corresponding data traffic) must not be interrupted. The MRR command period (tMRR) is two clock cycles.

● Temperature Sensor

Mobile LPDDR2 devices feature a temperature sensor whose status can be read from MR4. This sensor can be used to determine an appropriate refresh rate, determine whether AC timing derating is required in the extended temperature range, and/or monitor the operating temperature. Either the temperature sensor or the device operating temperature can be used to determine whether operating temperature requirements are being met (see Operating Temperature Range table).
Temperature sensor data can be read from MR4 using the mode register read protocol. Upon exiting self-refresh or power-down, the device temperature status bits will be no older than tTSI.
When using the temperature sensor, the actual device case temperature may be higher than the operating temperature specification that applies for the standard or extended temperature ranges. For example, TCASE could be above 85°C when MR4[2:0] equals 011b.
To ensure proper operation using the temperature sensor, applications must accommodate the parameters in the temperature sensor definitions table.

Table 25. Temperature Sensor Definitions and Operating Conditions

Parameter	Description	Symbol	Min/Max	Value	Unit
System temperature gradient	Maximum temperature gradient experienced by the memory device at the temperature of interest over a range of 2°C	TempGradient	Max	System-dependent	°C/s
MR4 READ interval	Time period between MR4 READs from the system	ReadInterval	Max	System-dependent	ms
Temperature sensor interval	Maximum delay between internal updates of MR4	tTSI	Max	32	ms
System response delay	Maximum response time from an MR4 READ to the system response	SysRespDelay	Max	System-dependent	ms
Device temperature margin	Margin above maximum temperature to support controller response	TempMargin	Max	2	°C

Moblie LPDDR2 devices accommodate the temperature margin between the point at which the device temperature enters the extended temperature range and the point at which the controller reconfigures the system accordingly. To determine the required MR4 polling frequency, the system must use the maximum TempGradient and the maximum response time of the system according to the following equation:
TempGradient × (ReadInterval + tTSI + SysRespDelay) ≦ 2°C
For example, if TempGradient is 10°C/s and the SysRespDelay is 1ms:
10°C/s * (ReadInterval + 32ms + 1ms) ≦ 2°C
In this case, ReadInterval must not exceed 167ms

● DQ Calibration

Mobile LPDDR2 devices feature a DQ Calibration function that outputs one of two predefined system timing calibration patterns. A Mode Register Read to MR32 (Pattern “A”) or MR40 (Pattern “B”) will return the specified pattern on DQ[0], DQ[8], DQ[16], and DQ[24] for x32 devices. For x32 devices, DQ[7:1], DQ[15:9], DQ[23:17], and DQ[31:25] may optionally drive the same information as DQ[0] or may drive 0b during the MRR burst. For LPDDR2 devices, MRR DQ Calibration commands may only occur in the idle state.

Table 26. Data Calibration Pattern Description

Pattern	MR#	Bit Time 0	Bit Time 1	Bit Time 2	Bit Time 3
Pattern A	MR32	1	0	1	0
Pattern B	MR40	0	0	1	1

● MODE REGISTER WRITE Command

The MODE REGISTER WRITE (MRW) command is used to write configuration data to the mode registers. The MRW command is initiated with CS# LOW, CA0 LOW, CA1 LOW, CA2 LOW, and CA3 LOW at the rising edge of the clock. The mode register is selected by CA1f – CA0f, CA9r – CA4r. The data to be written to the mode register is contained in CA9f – CA2f. The MRW command period is defined by tMRW. MRWs to read-only registers have no impact on the functionality of the device.
MRW can only be issued when all banks are in the idle precharge state. One method of ensuring that the banks are in this state is to issue a PRECHARGE ALL command.

Table 27. Truth Table for MRR and MRW

Current State	Command	Intermediate State	Next State
All banks idle	MRR	Reading mode register, all banks idle	All banks idle
	MRW	Writing mode register, all banks idle	
	MRW (RESET)	Resetting, device auto initialization	
Bank(s) active	MRR	Reading mode register, bank(s) idle	Bank(s) active
	MRW	Not allowed	Not allowed
	MRW (RESET)	Not allowed	Not allowed

● MRW RESET Command

The MRW RESET command brings the device to the device auto initialization (resetting) state in the power-on initialization sequence (see RESET Command). The MRW RESET command can be issued from the idle state. This command resets all mode registers to their default values. Only the NOP command is supported during tINIT4. After MRW RESET, boot timings must be observed until the device initialization sequence is complete and the device is in the idle state. Array data is undefined after the MRW RESET command has completed.
For MRW RESET timing, refer to “Power Ramp and Initialization Sequence” figure.

● MRW ZQ Calibration Command

The MRW command is also used to initiate the ZQ Calibration command. The ZQ Calibration command is used to calibrate the LPDDR2 ouput drivers (RON) over process, temperature, and voltage. LPDDR2-S4 devices support ZQ Calibration.
There are four ZQ Calibration commands and related timings, tZQINIT, tZQRESET, tZQCL, and tZQCS. tZQINIT corresponds to the initialization calibration, tZQRESET for resetting ZQ setting to default, tZQCL is for long calibration, and tZQCS is for short calibration. See Mode Register 10 (MR10) for description on the command codes for the different ZQ Calibration commands.
The Initialization ZQ Calibration (ZQINIT) shall be performed for LPDDR2-S4 devices. This Initialization Calibration achieves a RON accuracy of ±15%. After initialization, the ZQ Long Calibration may be used to re-calibrate the system to a RON accuracy of ±15%. A ZQ Short Calibration may be used periodically to compensate for temperature and voltage drift in the system.
The ZQReset Command resets the RON calibration to a default accuracy of ±30% across process, voltage, and temperature. This command is used to ensure RON accuracy to ±30% when ZQCS and ZQCL are not used.
One ZQCS command can effectively correct a minimum of 1.5% (ZQCorrection) of RON impedance error within tZQCS for all speed bins assuming the maximum sensitivities specified in the ‘Output Driver Voltage and Temperature Sensitivity’. The appropriate interval between ZQCS commands can be determined from these tables and other application-specific parameters.
One method for calculating the interval between ZQCS commands, given the temperature (Tdriftrate) and voltage (Vdriftrate) drift rates that the LPDDR2 is subject to in the application, is illustrated. The interval could be defined by the following formula:

$$\frac{\text{ZQCorrection}}{(\text{Tsens} \times \text{Tdriftrate}) + (\text{Vsens} \times \text{Vdriftrate})}$$

Where TSens = max(dRONdT) and VSens = max(dRONdV) define the LPDDR2 temperature and voltage sensitivities.

For example, if Tsens = 0.75%/°C, Vsens = 0.20%/mV, Tdriftrate = 1°C/sec, and Vdriftrate = 15 mV/sec, then the interval between ZQCS commands is calculated as:

$$\frac{1.5}{(0.75 \times 1) + (0.20 \times 15)} = 0.4s$$

For LPDDR2-S4 devices, a ZQ Calibration command may only be issued when the device is in Idle state with all banks precharged.
No other activities can be performed on the LPDDR2 data bus during the calibration period (tZQINIT, tZQCL, tZQCS). The quiet time on the LPDDR2 data bus helps to accurately calibrate RON. There is no required quiet time after the ZQ Reset command. If multiple devices share a single ZQ Resistor, only one device may be calibrating at any given time. After calibration is achieved, the LPDDR2 device shall disable the ZQ ball's current consumption path to reduce power.
In systems that share the ZQ resistor between devices, the controller must not allow overlap of tZQINIT, tZQCS, or tZQCL between the devices. ZQ Reset overlap is allowed. If the ZQ resistor is absent from the system, ZQ shall be connected permanently to VDDCA. In this case, the LPDDR2 device shall ignore ZQ calibration commands and the device will use the default calibration settings (See the Output Driver DC Electrical Characteristics without ZQ Calibration table)

- ZQ External Resistor Value, Tolerance, and Capacitive Loading

To use the ZQ calibration function, a 240 ohm (±1% tolerance) external resistor must be connected between the ZQ pin and ground. A single resistor can be used for each device or one resistor can be shared between multiple devices if the ZQ calibration timings for each device do not overlap. The total capacitive loading on the ZQ pin must be limited (see the Capacitance table).

● Power-Down

Power-down is entered synchronously when CKE is registered LOW and CS# is HIGH at the rising edge of clock. A NOP command must be driven in the clock cycle following power-down entry. CKE must not go LOW while MRR, MRW, READ, or WRITE operations are in progress. CKE can go LOW while any other operations such as ACTIVATE, PRECHARGE, auto precharge, or REFRESH are in progress, but the power-down IDD specification will not be applied until such operations are complete.
If power-down occurs when all banks are idle, this mode is referred to as idle powerdown; if power-down occurs when there is a row active in any bank, this mode is referred to as active power-down.
Entering power-down deactivates the input and output buffers, excluding CK, CK#, and CKE. In power-down mode, CKE must be held LOW; all other input signals are "Don't Care." CKE LOW must be maintained until tCKE is satisfied. VREFCA must be maintained at a valid level during power-down.
VDDQ can be turned off during power-down. If VDDQ is turned off, VREFDQ must also be turned off. Prior to exiting power-down, both VDDQ and VREFDQ must be within their respective minimum/maximum operating ranges.
No refresh operations are performed in power-down mode. The maximum duration in power-down mode is only limited by the refresh requirements outlined in REFRESH Command.
The power-down state is exited when CKE is registered HIGH. The controller must drive CS# HIGH in conjunction with CKE HIGH when exiting the power-down state. CKE HIGH must be maintained until tCKE is satisfied. A valid, executable command can be applied with power-down exit latency tXP after CKE goes HIGH. Power-down exit latency is defined in the AC Timing section.

● Deep Power-Down

Deep power-down (DPD) is entered when CKE is registered LOW with CS# LOW, CA0 HIGH, CA1 HIGH, and CA2 LOW at the rising edge of the clock. The NOP command must be driven in the clock cycle following power-down entry. CKE must not go LOW while MRR or MRW operations are in progress. CKE can go LOW while other operations such as ACTIVATE, auto precharge, PRECHARGE, or REFRESH are in progress, however, deep power-down IDD specifications will not be applied until those operations complete. The contents of the array will be lost upon entering DPD mode.
In DPD mode, all input buffers except CKE, all output buffers, and the power supply to internal circuitry are disabled within the device. VREFDQ can be at any level between 0 and VDDQ, and VREFCA can be at any level between 0 and VDDCA during DPD. All power supplies (including VREF) must be within the specified limits prior to exiting DPD.
To exit DPD, CKE must be HIGH, tISCKE must be complete, and the clock must be stable. To resume operation, the device must be fully reinitialized using the power-up initialization sequence.

● Input Clock Frequency Changes and Stop Events

- Input Clock Frequency Changes and Clock Stop with CKE LOW

During CKE LOW, Mobile LPDDR2 devices support input clock frequency changes and clock stop under the following conditions:

- Refresh requirements are met
- Only REFab commands can be in process
- Any ACTIVATE or PRECHARGE commands have completed prior to changing the frequency
- Related timing conditions,tRCD and tRP, have been met prior to changing the frequency
- The initial clock frequency must be maintained for a minimum of two clock cycles after CKE goes LOW
- The clock satisfies tCH(abs) and tCL(abs) for a minimum of two clock cycles prior to CKE going HIGH

For input clock frequency changes, tCK(MIN) and tCK(MAX) must be met for each clock cycle.
After the input clock frequency is changed and CKE is held HIGH, additional MRW commands may be required to set the WR, RL, etc. These settings may require adjustment to meet minimum timing requirements at the target clock frequency.
For clock stop, CK is held LOW and CK# is held HIGH.

- Input Clock Frequency Changes and Clock Stop with CKE HIGH

During CKE HIGH, LPDDR2 devices support input clock frequency changes and clock stop under the following conditions:

- REFRESH requirements are met
- Any ACTIVATE, READ, WRITE, PRECHARGE, MRW, or MRR commands must have completed, including any associated data bursts, prior to changing the frequency
- Related timing conditions, tRCD, tWR, tWRA, tRP, tMRW, and tMRR, etc., are met
- CS# must be held HIGH
- Only REFab commands can be in process

The device is ready for normal operation after the clock satisfies tCH(abs) and tCL(abs) for a minimum of $2 \times tCK + tXP$.
For input clock frequency changes, tCK(MIN) and tCK(MAX) must be met for each clock cycle.
After the input clock frequency is changed, additional MRW commands may be required to set the WR, RL, etc. These settings may require adjustment to meet minimum timing requirements at the target clock frequency.
For clock stop, CK is held LOW and CK# is held HIGH.

● NO OPERATION Command

The NO OPERATION (NOP) command prevents the device from registering any unwanted commands issued between operations. A NOP command can only be issued at clock cycle N when the CKE level is constant for clock cycle N-1 and clock cycle N. The NOP command has two possible encodings: CS# HIGH at the clock rising edge N; and CS# LOW with CA0, CA1, CA2 HIGH at the clock rising edge N.
The NOP command will not terminate a previous operation that is still in process, such as a READ burst or WRITE burst cycle.

Table 28. Absolute Maximum Rating

Symbol	Parameter	Values	Unit	Note
V_{IN}, V_{OUT}	Voltage on any I/O relative to V_{SS}	-0.4~1.6	V	
V_{DD1}	V_{DD1} supply voltage relative to V_{SS}	-0.4~2.3	V	2
V_{DD2}	V_{DD2} supply voltage relative to V_{SS}	-0.4~1.6	V	2
V_{DDCA}	V_{DDCA} supply voltage relative to V_{SSCA}	-0.4~1.6	V	2,4
V_{DDQ}	V_{DDQ} supply voltage relative to V_{SSQ}	-0.4~1.6	V	2,3
T_{STG}	Storage Temperature	-55~125	°C	5

Notes:
1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. See "Power-Ramp" in section "Power-Up and Initialization" for relationships between power supplies.
3. V_{REFCA} 0.6 ≦ V_{DDCA}; however, V_{REFCA} may be ≧ V_{DDCA} provided that V_{REFCA} ≦ 300mV.
4. V_{REFDQ} 0.6 ≦ V_{DDQ}; however, V_{REFDQ} may be ≧ V_{DDQ} provided that V_{REFDQ} ≦ 300mV.
5. Storage Temperature is the case surface temperature on the center/top side of the LPDDR2 device. For the measurement conditions, please refer to JESD51-2 standard.

Table 29. Operating Temperature Condition

Symbol	Parameter	Values	Unit	Note
T_{OPER}	Operating Temperature Range	-25~85	°C	

Notes:
1. Operating temperature is the case surface temperature at the center of the top side of the device.
2. Either the device operating temperature or the temperature sensor can be used to set an appropriate refresh rate, determine the need for AC timing derating, and/or monitor the operating temperature. When using the temperature sensor, the actual device case temperature may be higher than the TCASE rating that applies for the operating temperature range. For example, TCASE could be above 85˚C when the temperature sensor indicates a temperature of less than 85˚C.

Table 30. Recommended Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit	Note
V_{DD1} (DC)	Core power 1	1.7	1.8	1.95	V	1
V_{DD2} (DC)	Core power 2	1.14	1.2	1.3	V	
V_{DDCA} (DC)	Input buffer power	1.14	1.2	1.3	V	
V_{DDQ} (DC)	I/O buffer power	1.14	1.2	1.3	V	
I_L	Input leakage current	-2	-	2	μA	2
I_{VREF}	V_{REF} supply leakage current	-1	-	1	μA	3

Notes:
1. V_{DD1} uses significantly less power than V_{DD2}.
2. The minimum limit requirement is for testing purposes. The leakage current on V_{REFCA} and V_{REFDQ} pins should be minimal.
3. Although DM is for input only, the DM leakage shall match the DQ and DQS/DQS# output leakage specification.

● AC and DC Logic Input Measurement Levels for Single-Ended Signals

Table 31. Single-Ended AC and DC Input Levels for CA and CS# Inputs

Symbol	Parameter	Min.	Max.	Unit	Note
V_{IHCA} (AC)	AC input logic HIGH for CA/CS#	V_{REF} + 0.22	-	V	1,2
V_{ILCA} (AC)	AC input logic LOW for CA/CS#	-	V_{REF} - 0.22	V	1,2
V_{IHCA} (DC)	DC input logic HIGH for CA/CS#	V_{REF} + 0.13	V_{DDCA}	V	1
V_{ILCA} (DC)	DC input logic LOW for CA/CS#	V_{SSCA}	V_{REF} - 0.13	V	1
V_{REFCA} (DC)	Reference voltage for CA/CS# inputs	0.49 * V_{DDCA}	0.51 * V_{DDCA}	V	3,4

Notes:
1. For CA and CS# input only pins. V_{REF} = V_{REFCA} (DC).
2. See “Overshoot and Undershoot Specifications”.
3. The ac peak noise on V_{REFCA} may not allow V_{REFCA} to deviate from V_{REFCA} (DC) by more than ±1% V_{DDCA} (for reference: approx. ±12 mV).
4. For reference: approx. V_{DDCA}/2 ±12 mV.

Table 32. Single-Ended AC and DC Input Levels for CKE

Symbol	Parameter	Min.	Max.	Unit	Note
V_{IHCKE}	CKE Input High Level	0.8 * V_{DDCA}	-	V	1
V_{ILCKE}	CKE Input Low Level	-	0.2 * V_{DDCA}	V	1

Notes:
1. See “Overshoot and Undershoot Specifications”.

Table 33. Single-Ended AC and DC Input Levels for DQ and DM

Symbol	Parameter	Min.	Max.	Unit	Note
V_{IHDQ}(AC)	AC input logic high for DQ/DM	V_{REF} + 0.22	-	V	1,2
V_{ILDQ}(AC)	AC input logic low for DQ/DM	-	V_{REF} - 0.22	V	1,2
V_{IHDQ}(DC)	DC input logic high for DQ/DM	V_{REF} + 0.13	V_{DDQ}	V	1
V_{ILDQ}(DC)	DC input logic low for DQ/DM	V_{SSQ}	V_{REF} - 0.13	V	1
V_{REFDQ}(DC)	Reference Voltage for DQ/DM inputs	0.49 * V_{DDQ}	0.51 * V_{DDQ}	V	3,4

Notes:
1. For DQ input only pins. V_{REF} = V_{REFDQ} (DC).
2. See “Overshoot and Undershoot Specifications”.
3. The ac peak noise on V_{REFDQ} may not allow V_{REFDQ} to deviate from V_{REFDQ} (DC) by more than ±1% V_{DDQ} (for reference: approx. ±12 mV).
4. For reference: approx. VDDQ/2 ±12 mV.

● AC and DC Logic Input Measurement Levels for Differential Signals

Table 34. Differential AC and DC Input Levels

Symbol	Parameter	LPDDR2-1066 to LPDDR2-667		Unit	Note
		Min	Max		
V_{IH},diff(DC)	Differential input HIGH	2 × (V_{IH}(DC) - V_{REF})	-	V	1
V_{IL},diff(DC)	Differential input LOW	-	2 × (V_{REF} - V_{IL}(DC))	V	1
V_{IH},diff(AC)	Differential input HIGH AC	2 × (V_{IH}(AC) - V_{REF})	-	V	2
V_{IL},diff(AC)	Differential input LOW AC	-	2 × (V_{REF} - V_{IL}(AC))	V	2

Notes:
1. Used to define a differential signal slew-rate. For CK - CK# use V_{IH}/V_{IL}(DC) of CA and V_{REFCA}; for DQS - DQS#, use V_{IH}/V_{IL}(DC) of DQs and V_{REFDQ}; if a reduced dc-high or dc-low level is used for a signal group, then the reduced level applies also here.
2. For CK - CK# use V_{IH}/V_{IL}(AC) of CA and V_{REFCA}; for DQS - DQS#, use V_{IH}/V_{IL}(AC) of DQs and V_{REFDQ}; if a reduced ac-high or ac-low level is used for a signal group, then the reduced level applies also here.
3. These values are not defined, however the single-ended signals CK, CK#, DQS, and DQS# need to be within the respective limits (V_{IH}(DC)max, V_{IL}(DC)min) for single-ended signals as well as the limitations for overshoot and undershoot. Refer to “Overshoot and Undershoot Specifications”.
4. For CK and CK#, V_{REF} = V_{REFCA}(DC); For DQS and DQS# V_{REF} = V_{REFDQ}(DC)

- Single-Ended Requirements for Differential Signals

Each individual component of a differential signal (CK, CK#, DQS, and DQS#) must also comply with certain requirements for single-ended signals.
CK and CK# must meet V_{SEH}(AC)min/V_{SEL}(AC)max in every half cycle.
DQS, DQS# must meet V_{SEH}(AC)min /V_{SEL}(AC)max in every half cycle preceding and following a valid transition.
The applicable AC levels for CA and DQ differ by speed bin.

Table 35. Single-Ended Levels for CK, CK#, DQS, DQS#

Symbol	Parameter	LPDDR2-1066 to LPDDR2-667		Unit	Note
		Min	Max		
V_{SEH}(AC)	Single-ended HIGH level for strobes	(V_{DDQ}/2) + 0.22	-	V	1, 2
	Single-ended HIGH level for CK, CK#	(V_{DDCA}/2) + 0.22	-	V	1, 2
V_{SEL}(AC)	Single-ended LOW level for strobes	-	(V_{DDQ}/2) - 0.22	V	1, 2
	Single-ended LOW level for CK, CK#	-	(V_{DDCA}/2) - 0.22	V	1, 2

Notes:
1. For CK and CK#, use V_{SEH}/V_{SEL}(AC) of CA; for strobes (DQS[3:0] and DQS#[3:0]), use V_{IH}/V_{IL}(AC) of DQ.
2. V_{IH}(AC) and V_{IL}(AC) for DQ are based on V_{REFDQ}; V_{SEH}(AC) and V_{SEL}(AC) for CA are based on V_{REFCA}. If a reduced AC HIGH or AC LOW is used for a signal group, the reduced level applies.
3. These values are not defined, however the single-ended signals CK, CK#, DQS[3:0] and DQS#[3:0] need to be within the respective limits (V_{IH}(DC)max, V_{IL}(DC)min) for single-ended signals as well as the limitations for overshoot and undershoot. Refer to “Overshoot and Undershoot Specifications”.

- Differential Input Crosspoint Voltage

The differential input crosspoint voltage (V_{IX}) is measured from the actual crosspoint of the true signal and it's and complement to the midlevel between V_{DD} and V_{SS}.

Table 36. Crosspoint Voltage for Differential Input Signals (CK, CK#, DQS, DQS#)

Symbol	Parameter	LPDDR2-1066 to LPDDR2-667		Unit	Note
		Min	Max		
V_{IXCA}(AC)	Differential input crosspoint voltage relative to V_{DDCA}/2 for CK and CK#	-120	120	mV	1, 2
V_{IXDQ}(AC)	Differential input crosspoint voltage relative to V_{DDQ}/2 for DQS and DQ#	-120	120	mV	1, 2

Notes:

1. The typical value of V_{IX}(AC) is expected to be about 0.5 × V_{DD} of the transmitting device, and it is expected to track variations in V_{DD}. V_{IX}(AC) indicates the voltage at which differential input signals must cross.
2. For CK and CK#, V_{REF} = V_{REFCA}(DC). For DQS and DQS#, V_{REF} = V_{REFDQ}(DC).

- Input Slew Rate

Table 37. Differential Input Slew Rate Definition

Description	Measured		Defined by
	From	To	
Differential input slew rate for rising edge (CK/CK# and DQS/DQS#)	V_{IL},diff,max	V_{IH},diff,min	[V_{IH},diff,min - V_{IL},diff,max] / Δ TRdiff
Differential input slew rate for falling edge (CK/CK# and DQS/DQS#)	V_{IH},diff,min	V_{IL},diff,max	[V_{IH},diff,min - V_{IL},diff,max] / Δ TFdiff

- Output Characteristics and Operating Conditions

Table 38. Single-Ended AC and DC Output Levels

Symbol	Parameter		Value	Unit	Note
V_{OH}(AC)	AC output HIGH measurement level (for output slew rate)		V_{REF} + 0.12	V	
V_{OL}(AC)	AC output LOW measurement level (for output slew rate)		V_{REF} - 0.12	V	
V_{OH}(DC)	DC output HIGH measurement level (for I-V curve linearity)		0.9 x V_{DDQ}	V	I_{OH} = -0.1mA
V_{OL}(DC)	DC output LOW measurement level (for I-V curve linearity)		0.1 x V_{DDQ}	V	I_{OL} = 0.1mA
I_{OZ}	Output leakage current (DQ, DM, DQS, DQS#); DQ, DQS, DQS# are disabled; 0V ≦ V_{OUT} ≦ V_{DDQ}	Min	-5	uA	
		Max	5	uA	
MMpupd	Delta output impedance between pull-up and pulldown for DQ/DM	Min	-15	%	
		Max	15	%	

Table 39. Differential AC and DC Output Levels

Symbol	Parameter	Value	Unit	Note
V_{OH}diff(AC)	AC differential output HIGH measurement level (for output SR)	0.2 x V_{DDQ}	V	I_{OH} = -0.1mA
V_{OL}diff(AC)	AC differential output LOW measurement level (for output SR)	-0.2 x V_{DDQ}	V	I_{OL} = 0.1mA

- Single-Ended Output Slew Rate

Table 40. Single-Ended Output Slew Rate Definition

Description	Measured		Defined by
	From	To	
Single-ended output slew rate for rising edge	V_{OL}(AC)	V_{OH}(AC)	[V_{OH}(AC) - V_{OL}(AC)] / ΔTR_{SE}
Single-ended output slew rate for falling edge	V_{OH}(AC)	V_{OL}(AC)	[V_{OH}(AC) - V_{OL}(AC)] / ΔTF_{SE}

Table 41. Single-Ended Output Slew Rate

Symbol	Parameter	Value		Unit
		Min	Max	
SRQ_{SE}	Single-ended output slew rate (output impedance = 40Ω ±30%)	1.5	3.5	V/ns
SRQ_{SE}	Single-ended output slew rate (output impedance = 60Ω ±30%)	1	2.5	V/ns
	Output slew-rate-matching ratio (pull-up to pull-down)	0.7	1.4	-

Notes:
1. Definitions:
   SR = slew rate; Q = Query Output (like in DQ, which stands for Data-in, Query-Output); SE = singleended signals.
2. Measured with output reference load.
3. The ratio of pull-up to pull-down slew rate is specified for the same temperature and voltage over the entire temperature and voltage range. For a given output, the ratio represents the maximum difference between pull-up and pull-down drivers due to process variation.
4. The output slew rate for falling and rising edges is defined and measured between V_{OL}(AC) and V_{OH}(AC).
5. Slew rates are measured under typical simultaneous switching output (SSO) conditions, with one-half of DQ signals per data byte driving HIGH and one-half of DQ signals per data byte driving LOW.

- Differential Output Slew Rate

Table 42. Differential Output Slew Rate Definition

Description	Measured		Defined by
	From	To	
Differential output slew rate for rising edge	V_{OL},diff(AC)	V_{OH},diff(AC)	[VOH,diff(AC) - VOL,diff(AC)] / Δ TRdiff
Differential output slew rate for falling edge	V_{OH},diff(AC)	V_{OL},diff(AC)	[VOH,diff(AC) - VOL,diff(AC)] / Δ TFdiff

Table 43. Differential Output Slew Rate

Symbol	Parameter	Value		Unit
		Min	Max	
SRQ_{diff}	Differential output slew rate (output impedance = 40Ω ±30%)	3	7	V/ns
SRQ_{diff}	Differential output slew rate (output impedance = 60Ω ±30%)	2	5	V/ns

Notes:
1. Definitions:
   SR = slew rate; Q = Query Output (like in DQ, which stands for Data-in, Query-Output); SE = singleended signals.
2. Measured with output reference load.
3. The output slew rate for falling and rising edges is defined and measured between V_{OL}(AC) and V_{OH}(AC).
4. Slew rates are measured under normal SSO conditions, with 1/2 of DQ signals per data byte driving logic-high and 1/2 of DQ signals per data byte driving logic-low.

- Overshoot/Undershoot Specification

Table 44. AC Overshoot/Undershoot Specification (CA0-9, CS#, CKE, CK, CK#, DQ, DQS, DQS#, DM)

Parameter	-18	-25	-3	Unit
	Max			
Maximum peak amplitude provided for overshoot area	0.35	0.35	0.35	V
Maximum peak amplitude provided for undershoot area	0.35	0.35	0.35	V
Maximum area above V_{DD}	0.15	0.2	0.24	V/ns
Maximum area below V_{SS}	0.15	0.2	0.24	V/ns

Notes:
1. For CA0-9, CK, CK#, CS#, and CKE, V_{DD} stands for V_{DDCA}. For DQ, DM, DQS, and DQS#, V_{DD} stands for V_{DDQ}.
2. For CA0-9, CK, CK#, CS#, and CKE, V_{SS} stands for V_{SSCA}. For DQ, DM, DQS, and DQS#, V_{SS} stands for V_{SSQ}.
3. Maximum peak amplitude values are referenced from actual V_{DD} and V_{SS} values.
4. Maximum area values are referenced from maximum operating V_{DD} and V_{SS} values.

Table 45. Capacitance (V_{DD1} = 1.8V, V_{DDCA}/V_{DDQ}/V_{DD2} = 1.2V, T_{OPER} = -25~85 °C)

Notes 1 – 2 apply to all parameters and conditions

Symbol	Parameter	Min.	Max.	Unit	Note
C_{CK}	Input Capacitance (CK, CK#)	1.0	2.0	pF	
C_{DCK}	Input capacitance delta (CK, CK#)	0	0.2	pF	3
C_I	Input capacitance (all other inputonly pins)	1.0	2.0	pF	4
C_{DI}	Input capacitance delta (all other inputonly pins)	-0.40	0.40	pF	5
C_{IO}	Input/output capacitance (DQ, DM, DQS, DQS#)	1.25	2.5	pF	6~7
C_{DDQS}	Input/output capacitance delta (DQS, DQS#)	0	0.25	pF	7~8
C_{DIO}	Input/output capacitance delta (DQ, DM)	-0.5	0.5	pF	7, 9
C_{ZQ}	Input/output capacitance ZQ Pin	0	2.5	pF	10

Notes:
1. This parameter applies to die devices only (does not include package capacitance).
2. This parameter is not subject to production testing. It is verified by design and characterization. The capacitance is measured according to JEP147 (procedure for measuring input capacitance using a vector network analyzer), with V_{DD1}, V_{DD2}, V_{DDQ}, V_{SS}, V_{SSCA}, and V_{SSQ} applied; all other pins are left floating.
3. Absolute value of C_{CK} - $C_{CK\#}$.
4. C_I applies to CS#, CKE, and CA[9:0].
5. $C_{DI} = C_I - 0.5 \times (C_{CK} + C_{CK\#})$.
6. DM loading matches DQ and DQS.
7. MR3 I/O configuration drive strength OP[3:0] = 0001b (34.3 ohm typical).
8. Absolute value of C_{DQS} and $C_{DQS\#}$.
9. $C_{DIO} = C_{IO} - 0.5 \times (C_{DQS} + C_{DQS\#})$ in byte-lane.
10. Maximum external load capacitance on ZQ pin: 5pF.

● Electrical Specifications – IDD Specifications and Conditions

The following definitions and conditions are used in the IDD measurement tables unless stated otherwise:

- LOW: $V_{IN} \leqq V_{IL}(DC)max$
- HIGH: $V_{IN} \geqq V_{IH}(DC)min$
- STABLE: Inputs are stable at a HIGH or LOW level
- SWITCHING: See the following three tables

Table 46. Switching for CA Input Signals

CK/CK#	Rising/ Falling	Falling/ Rising	Rising/ Falling	Falling/ Rising	Rising/ Falling	Falling/ Rising	Rising/ Falling	Falling/ Rising
Cycle	N		N+1		N+2		N+3	
CS#	HIGH		HIGH		HIGH		HIGH	
CA0	H	L	L	L	L	H	H	H
CA1	H	H	H	L	L	L	L	H
CA2	H	L	L	L	L	H	H	H
CA3	H	H	H	L	L	L	L	H
CA4	H	L	L	L	L	H	H	H
CA5	H	H	H	L	L	L	L	H
CA6	H	L	L	L	L	H	H	H
CA7	H	H	H	L	L	L	L	H
CA8	H	L	L	L	L	H	H	H
CA9	H	H	H	L	L	L	L	H

Notes:

1. CS# must always be driven HIGH.
2. For each clock cycle, 50% of the CA bus is changing between HIGH and LOW.
3. The noted pattern (N, N+1, N+2, N+3...) is used continuously during IDD measurement for IDD values that require switching on the CA bus.

Table 47. Switching for IDD4R

Clock	CKE	CS#	Cycle	Command	CA[2:0]	CA[9:3]	All DQ
Rising	H	L	N	Read_Rising	HLH	LHLHLHL	L
Falling	H	L	N	Read_Falling	LLL	LLLLLLL	L
Rising	H	H	N+1	NOP	LLL	LLLLLLL	H
Falling	H	H	N+1	NOP	HLH	LHLLHLH	L
Rising	H	L	N+2	Read_Rising	HLH	LHLLHLH	H
Falling	H	L	N+2	Read_Falling	LLL	HHHHHHH	H
Rising	H	H	N+3	NOP	LLL	HHHHHHH	H
Falling	H	H	N+3	NOP	HLH	LHLHLHL	L

Notes:

1. Data strobe (DQS) is changing between HIGH and LOW with every clock cycle.
2. The noted pattern (N, N+1...) is used continuously during IDD measurement for IDD4R.

Table 48. Switching for IDD4W

Clock	CKE	CS#	Cycle	Command	CA[2:0]	CA[9:3]	All DQ
Rising	H	L	N	Write_Rising	LLH	LHLHLHL	L
Falling	H	L	N	Write_Falling	LLL	LLLLLLL	L
Rising	H	H	N+1	NOP	LLL	LLLLLLL	H
Falling	H	H	N+1	NOP	HLH	LHLLHLH	L
Rising	H	L	N+2	Write_Rising	LLH	LHLLHLH	H
Falling	H	L	N+2	Write_Falling	LLL	HHHHHHH	H
Rising	H	H	N+3	NOP	LLL	HHHHHHH	H
Falling	H	H	N+3	NOP	HLH	LHLHLHL	L

Notes:
1. Data strobe (DQS) is changing between HIGH and LOW with every clock cycle.
2. Data masking (DM) must always be driven LOW.
3. The noted pattern (N, N+1...) is used continuously during IDD measurement for IDD4W.

Table 49. D.C. Characteristics (V_{DD1} = 1.8V, V_{DDCA} /V_{DDQ} /V_{DD2} = 1.2V, T_{OPER} = -25~85 °C)

Parameter & Test Condition	Symbol	Power Supply	-18/18R	-25/25R	-3/3R	Unit	Note
			Max.				
Operating one bank active-precharge current: t_{RC}=$t_{RC(min)}$; t_{CK}=$t_{CK(min)}$; CKE is HIGH; CS# is HIGH between valid commands; CA bus inputs are SWITCHING; data bus inputs are STABLE	$IDD0_1$	V_{DD1}	16	16	16	mA	1
	$IDD0_2$	V_{DD2}	26	21	16	mA	1
	$IDD0_{IN}$	V_{DDCA}, V_{DDQ}	7.5	7.5	7.5	mA	1,4
Idle power-down standby current: All banks idle, CKE is LOW; CS# is HIGH, t_{CK}=$t_{CK(min)}$; CA bus inputs are SWITCHING; data bus inputs are STABLE	$IDD2P_1$	V_{DD1}	0.4	0.4	0.4	mA	1
	$IDD2P_2$	V_{DD2}	1	1	1	mA	1
	$IDD2P_{IN}$	V_{DDCA}, V_{DDQ}	0.3	0.3	0.3	mA	1,4
Idle power-down standby current with clock stop: All banks idle, CKE is LOW; CS# is HIGH, CK = LOW, CK# = HIGH; CA bus inputs are STABLE; data bus inputs are STABLE	$IDD2PS_1$	V_{DD1}	0.4	0.4	0.4	mA	1
	$IDD2PS_2$	V_{DD2}	1	1	1	mA	1
	$IDD2PS_{IN}$	V_{DDCA}, V_{DDQ}	0.3	0.3	0.3	mA	1,4
Idle non power-down standby current: All banks idle, CKE is HIGH; CS# is HIGH, t_{CK}=$t_{CK(min)}$; CA bus inputs are SWITCHING; data bus inputs are STABLE	$IDD2N_1$	V_{DD1}	0.6	0.6	0.6	mA	1
	$IDD2N_2$	V_{DD2}	15	15	15	mA	1
	$IDD2N_{IN}$	V_{DDCA}, V_{DDQ}	7.5	7.5	7.5	mA	1,4
Idle non power-down standby current with clock stop: All banks idle, CKE is HIGH; CS# is HIGH, CK = LOW, CK# = HIGH; CA bus inputs are STABLE; data bus inputs are STABLE	$IDD2NS_1$	V_{DD1}	0.6	0.6	0.6	mA	1
	$IDD2NS_2$	V_{DD2}	10	8	8	mA	1
	$IDD2NS_{IN}$	V_{DDCA}, V_{DDQ}	7.5	7.5	7.5	mA	1,4
Active power-down standby current: One bank active, CKE is LOW; CS# is HIGH, t_{CK}=$t_{CK(min)}$; CA bus inputs are SWITCHING; data bus inputs are STABLE	$IDD3P_1$	V_{DD1}	1	1	1	mA	1
	$IDD3P_2$	V_{DD2}	8	8	8	mA	1
	$IDD3P_{IN}$	V_{DDCA}, V_{DDQ}	0.3	0.3	0.3	mA	1,4
Active power-down standby current with clock stop: One bank active, CKE is LOW; CS# is HIGH, CK = LOW, CK# = HIGH;CA bus inputs are STABLE; data bus inputs are STABLE	$IDD3PS_1$	V_{DD1}	1	1	1	mA	1
	$IDD3PS_2$	V_{DD2}	8	8	8	mA	1
	$IDD3PS_{IN}$	V_{DDCA}, V_{DDQ}	0.3	0.3	0.3	mA	1,4
Active non power-down standby current: One bank active, CKE is HIGH; CS# is HIGH, t_{CK}=$t_{CK(min)}$; CA bus inputs are SWITCHING; data bus inputs are STABLE	$IDD3N_1$	V_{DD1}	1.5	1.5	1.5	mA	1
	$IDD3N_2$	V_{DD2}	20	20	20	mA	1
	$IDD3N_{IN}$	V_{DDCA}, V_{DDQ}	7.5	7.5	7.5	mA	1,4
Active non power-down standby current with clock stop: One bank active, CKE is HIGH; CS# is HIGH, CK = LOW, CK# = HIGH; CA bus inputs are STABLE; data bus inputs are STABLE	$IDD3NS_1$	V_{DD1}	1.5	1.5	1.5	mA	1
	$IDD3NS_2$	V_{DD2}	15	15	15	mA	1
	$IDD3NS_{IN}$	V_{DDCA}, V_{DDQ}	7.5	7.5	7.5	mA	1,4
Operating burst read current: t_{CK}=$t_{CK(min)}$; CS# is HIGH between valid commands; One bank active; BL = 4; RL = RL(min); CA bus inputs are SWITCHING; 50% data change each burst transfer	$IDD4R_1$	V_{DD1}	2	2	2	mA	1
	$IDD4R_2$	V_{DD2}	155	140	125	mA	1
	$IDD4R_{IN}$	V_{DDCA}	6.5	6.5	6.5	mA	1

Operating burst write current: $t_{CK}=t_{CK(min)}$; CS# is HIGH between valid commands; One bank active; BL = 4; WL = WL(min); CA bus inputs are SWITCHING; 50% data change each burst transfer	$IDD4W_1$	V_{DD1}	2	2	2	mA	1
	$IDD4W_2$	V_{DD2}	150	140	130	mA	1
	$IDD4W_{IN}$	V_{DDCA}, V_{DDQ}	30	30	30	mA	1,4
All Bank Refresh Burst current: $t_{CK}=t_{CK(min)}$; CKE is HIGH between valid commands; $t_{RC}=t_{RFC(min)}$; burst refresh; CA bus inputs are SWITCHING; data bus inputs are STABLE	$IDD5_1$	V_{DD1}	38	34	30	mA	1
	$IDD5_2$	V_{DD2}	38	34	30	mA	1
	$IDD5_{IN}$	V_{DDCA}, V_{DDQ}	7.5	7.5	7.5	mA	1,4
All Bank Refresh Average current: $t_{CK}=t_{CK(min)}$; CKE is HIGH between valid commands; $t_{RC}=t_{RFC(min)}$; CA bus inputs are SWITCHING; data bus inputs are STABLE	$IDD5AB_1$	V_{DD1}	2	2	2	mA	1
	$IDD5AB_2$	V_{DD2}	16	16	16	mA	1
	$IDD5AB_{IN}$	V_{DDCA}, V_{DDQ}	7.5	7.5	7.5	mA	1,4
Self refresh current: CK = LOW, CK# = HIGH; CKE is LOW, CA bus inputs are STABLE; data bus inputs are STABLE, Maximum 1x Self-Refresh Rate	$IDD6_1$	V_{DD1}	0.6	0.6	0.6	mA	1,3, 7
	$IDD6_2$	V_{DD2}	1.5	1.5	1.5	mA	1,3, 7
	$IDD6_{IN}$	V_{DDCA}, V_{DDQ}	0.3	0.3	0.3	mA	1,3, 4,7
Deep Power Down Mode Current: CK=LOW; CK# =HIGH; CKE is LOW; CA bus inputs are STABLE; Data bus inputs are STABLE	$IDD8_1$	V_{DD1}	30	30	30	uA	1
	$IDD8_2$	V_{DD2}	30	30	30	uA	1
	$IDD8_{IN}$	V_{DDCA}, V_{DDQ}	100	100	100	uA	1,4

Notes:

1. IDD values are the maximum of the distribution of the arithmetic mean.
2. IDD current specifications are tested after the device is properly initialized.
3. The 1x self refresh rate is the rate at which the device is refreshed internally during self refresh, before going into the extended temperature range.
4. Measured currents are the sum of V_{DDQ} and V_{DDCA}.
5. Guaranteed by design with output reference load and RON = 40 ohm.
6. The IDD6 currents are measured using bank-masking only.

Parameter	PASR	Power Supply	45°C	85°C	Unit
			Max.	Max.	
Partial Array Self Refresh Current	Full array	V_{DD1}	600	700	uA
		V_{DD2}	1500	2000	
		V_{DDCA}, V_{DDQ}	300	300	
	1/2 array	V_{DD1}	550	600	uA
		V_{DD2}	1300	1500	
		V_{DDCA}, V_{DDQ}	300	300	
	1/4 array	V_{DD1}	530	550	uA
		V_{DD2}	1200	1300	
		V_{DDCA}, V_{DDQ}	300	300	

7. This is the general definition that applies to full-array self refresh.

Table 50. Electrical AC Characteristics (V_{DD1} = 1.8V, V_{DDCA} /V_{DDQ} /V_{DD2} = 1.2V, T_{OPER} = -25~85 °C)

Symbol	Parameter	tCK	-18		-25		-3		Unit
		Min.	Min.	Max.	Min.	Max.	Min.	Max.	
Clock Timing									
$t_{CK(avg)}$	Average clock period		1.875	100	2.5	100	3	100	ns
$t_{CH(avg)}$	Average HIGH pulse width		0.45	0.55	0.45	0.55	0.45	0.55	t_{CK}
$t_{CL(avg)}$	Average LOW pulse width		0.45	0.55	0.45	0.55	0.45	0.55	t_{CK}
$t_{CK(abs)}$	Absolute clock period		**Min:** $t_{CK(avg)min} + t_{JIT(per),min}$ **Max:** -						ps
$t_{CH(abs)}$, allowed	Absolute clock HIGH pulse width		0.43	0.57	0.43	0.57	0.43	0.57	t_{CK}
$t_{CL(abs)}$, allowed	Absolute clock LOW pulse width		0.43	0.57	0.43	0.57	0.43	0.57	t_{CK}
$t_{JIT(per)}$, allowed	Clock Period Jitter (with allowed jitter)		-90	90	-100	100	-110	110	ps
$t_{JIT(cc)}$, allowed	Maximum Clock Jitter between two consecutive clock cycles (with allowed jitter)		-	180	-	200	-	220	ps
$t_{JIT(duty)}$, allowed	Duty cycle Jitter (with allowed jitter)		**Min:** $\min((t_{CH(abs),min} - t_{CH(avg),min}), (t_{CL(abs),min} - t_{CL(avg),min})) * t_{CK(avg)}$ **Max:** $\max((t_{CH(abs),max} - t_{CH(avg),max}), (t_{CL(abs),max} - t_{CL(avg),max})) * t_{CK(avg)}$						ps
$t_{ERR(2per)}$, allowed	Cumulative error across 2 cycles		-132	132	-147	147	-162	162	ps
$t_{ERR(3per)}$, allowed	Cumulative error across 3 cycles		-157	157	-175	175	-192	192	ps
$t_{ERR(4per)}$, allowed	Cumulative error across 4 cycles		-175	175	-194	194	-214	214	ps
$t_{ERR(5per)}$, allowed	Cumulative error across 5 cycles		-188	188	-209	209	-230	230	ps
$t_{ERR(6per)}$, allowed	Cumulative error across 6 cycles		-200	200	-222	222	-244	244	ps
$t_{ERR(7per)}$, allowed	Cumulative error across 7 cycles		-209	209	-232	232	-256	256	ps
$t_{ERR(8per)}$, allowed	Cumulative error across 8 cycles		-217	217	-241	241	-266	266	ps
$t_{ERR(9per)}$, allowed	Cumulative error across 9 cycles		-224	224	249	249	-274	274	ps
$t_{ERR(10per)}$, allowed	Cumulative error across 10 cycles		-231	231	-257	257	-282	282	ps
$t_{ERR(11per)}$, allowed	Cumulative error across 11 cycles		-237	237	-263	263	-289	289	ps
$t_{ERR(12per)}$, allowed	Cumulative error across 12 cycles		-242	242	-269	269	-296	296	ps

$t_{ERR(nper),allowed}$	Cumulative error across n = 13, 14 . . . 49, 50 cycles		**Min:** t_{ERR}(nper), allowed, min= (1+0.68ln(n)) * t_{JIT}(per),allowed,min **Max:** t_{ERR}(nper), allowed, max= (1+0.68ln(n)) * t_{JIT}(per),allowed, max						ps
ZQ Calibration Parameters									
t_{ZQINIT}	Initialization Calibration Time		1	-	1	-	1	-	µs
t_{ZQCL}	Long Calibration Time	6	360	-	360	-	360	-	ns
t_{ZQCS}	Short Calibration Time	6	90	-	90	-	90	-	ns
$t_{ZQRESET}$	Calibration Reset Time	3	50	-	50	-	50	-	ns
Read Parameters									
t_{DQSCK}	DQS output access time from CK/CK#		2.5	5.5	2.5	5.5	2.5	5.5	ns
$t_{DQSCKDS}$[4]	DQSCK Delta Short		-	0.33	-	0.45	-	0.54	ns
$t_{DQSCKDM}$[5]	DQSCK Delta Medium		-	0.68	-	0.9	-	1.05	ns
$t_{DQSCKDL}$[6]	DQSCK Delta Long		-	0.92	-	1.2	-	1.4	ns
t_{DQSQ}	DQS - DQ skew		-	0.2	-	0.24	-	0.28	ns
t_{QHS}	Data hold skew factor		-	0.23	-	0.28	-	0.34	ns
t_{QSH}	DQS Output High Pulse Width		**Min:** tCH(abs) - 0.05						t_{CK}
t_{QSL}	DQS Output Low Pulse Width		**Min:** tCL(abs) - 0.05						t_{CK}
t_{QHP}	Data Half Period		**Min:** min(tQSH, tQSL)						t_{CK}
t_{QH}	DQ / DQS output hold time from DQS		**Min:** tQHP - tQHS						ps
t_{RPRE}[7]	Read preamble		0.9	-	0.9	-	0.9	-	t_{CK}
t_{RPST}[8]	Read postamble		**Min:** tCL(abs) - 0.05						t_{CK}
$t_{LZ(DQS)}$	DQS low-Z from clock		**Min:** tDQSCK(MIN) - 300						ps
$t_{LZ(DQ)}$	DQ low-Z from clock		**Min:** tDQSCK(MIN) - (1.4 * tQHS(MAX))						ps
$t_{HZ(DQS)}$	DQS high-Z from clock		**Max:** tDQSCK(MAX) - 100						ps
$t_{HZ(DQ)}$	DQ high-Z from clock		**Max:** tDQSCK(MAX) + (1.4 * tDQSQ(MAX))						ps
Write Parameters									
t_{DH}	DQ and DM input hold time (Vref based)		0.21	-	0.27	-	0.35	-	ns
t_{DS}	DQ and DM input setup time (Vref based)		0.21	-	0.27	-	0.35	-	ns
t_{DIPW}	DQ and DM input pulse width		0.35	-	0.35	-	0.35	-	t_{CK}
t_{DQSS}	Write command to 1st DQS latching transition		0.75	1.25	0.75	1.25	0.75	1.25	t_{CK}
t_{DQSH}	DQS input high-level width		0.4	-	0.4	-	0.4	-	t_{CK}
t_{DQSL}	DQS input low-level width		0.4	-	0.4	-	0.4	-	t_{CK}
t_{DSS}	DQS falling edge to CK setup time		0.2	-	0.2	-	0.2	-	t_{CK}
t_{DSH}	DQS falling edge hold time from CK		0.2	-	0.2	-	0.2	-	t_{CK}
t_{WPST}	Write postamble		0.4	-	0.4	-	0.4		t_{CK}

t_{WPRE}	Write preamble		0.35	-	0.35	-	0.35	-	t_{CK}
CKE Input Parameters									
t_{CKE}	CKE min. pulse width (high and low pulse width)	3	3	-	3	-	3	-	t_{CK}
t_{ISCKE}[9]	CKE input setup time		0.25	-	0.25	-	0.25	-	t_{CK}
t_{IHCKE}[10]	CKE input hold time		0.25	-	0.25	-	0.25	-	t_{CK}
Command Address Input Parameters									
t_{IS}[3, 11]	Address and control input setup time (V_{REF} based)		0.22	-	0.29	-	0.37	-	ns
t_{IH}[3, 11]	Address and control input hold time (V_{REF} based)		0.22	-	0.29	-	0.37	-	ns
t_{IPW}	Address and control input pulse width		0.4	-	0.4	-	0.4	-	t_{CK}
Mode Register Parameters									
t_{MRW}	MODE REGISTER Write command period	5	5	-	5	-	5	-	t_{CK}
t_{MRR}	Mode Register Read command period	2	2	-	2	-	2	-	t_{CK}
LPDDR2 SDRAM Core Parameters									
RL	Read Latency	3	8	-	6	-	5	-	t_{CK}
WL	Write Latency	1	4	-	3	-	2	-	t_{CK}
t_{RC}[17]	ACTIVE to ACTIVE command period	**Min:** t_{RAS} + t_{RPab} (with all-bank Precharge) **Min:** t_{RAS} + t_{RPpb} (with per-bank Precharge)							ns
t_{CKESR}	CKE min. pulse width during Self-Refresh (low pulse width during Self-Refresh)	3	15	-	15	-	15	-	ns
t_{XSR}	Self refresh exit to next valid command delay	2	**Min:** t_{RFC} + 10						ns
t_{XP}	Exit power down to next valid command delay	2	7.5	-	7.5	-	7.5	-	ns
t_{CCD}	CAS to CAS delay	2	2	-	2	-	2	-	t_{CK}
t_{RTP}	Internal Read to Precharge command delay	2	7.5	-	7.5	-	7.5	-	ns
t_{RCD}	RAS to CAS Delay	3	18	-	18	-	18	-	ns
t_{RPpb}	Row Precharge Time (single bank)	3	18	-	18	-	18	-	ns
t_{RPab}	Row Precharge Time (4-bank)	3	18	-	18	-	18	-	ns
t_{RAS}	Row Active Time	3	42	70K	42	70K	42	70K	ns
t_{WR}	Write Recovery Time	3	15	-	15	-	15	-	ns
t_{WTR}	Internal Write to Read Command Delay	2	7.5	-	7.5	-	7.5	-	ns
t_{RRD}	Active bank A to Active bank B	2	10	-	10	-	10	-	ns
t_{FAW}	Four Bank Activate Window	8	50	-	50	-	50	-	ns
t_{DPD}	Minimum Deep Power Down Time		500	-	500	-	500	-	µs
t_{REFI}	Average time between REFRESH commands		7.8	-	7.8	-	7.8	-	µs
t_{RFC}	Refresh Cycle time		90	-	90	-	90	-	ns
t_{REFBW}	Burst REFRESH window = 4 × 8 × tRFC		2.88	-	2.88	-	2.88	-	µs
Boot Parameters (10 MHz - 55 MHz)									
t_{CKb}	Clock Cycle Time		18	100	18	100	18	100	ns
t_{ISCKEb}	CKE Input Setup Time		2.5	-	2.5	-	2.5	-	ns
t_{IHCKEb}	CKE Input Hold Time		2.5	-	2.5	-	2.5	-	ns

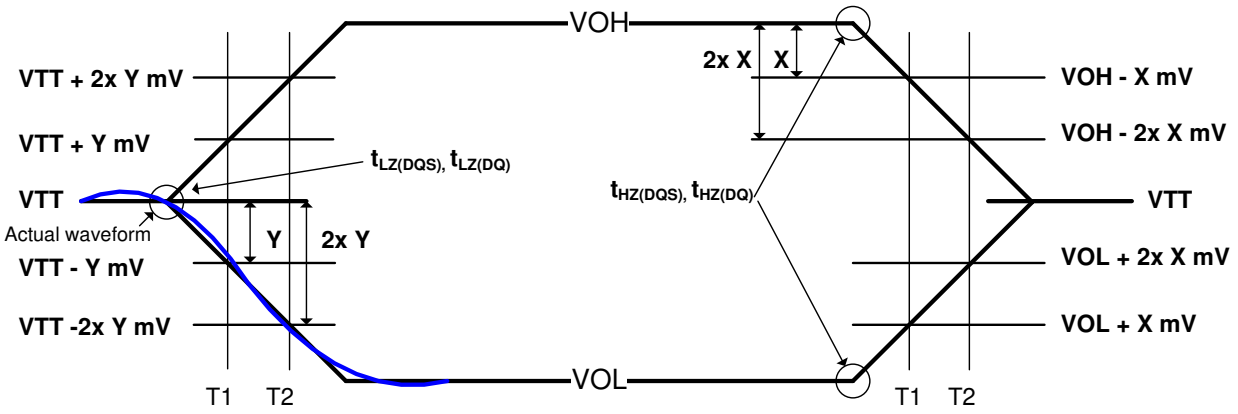
t_{ISb}	Address & Control Input Setup Time		1.15	-	1.15	-	1.15	-	ns
t_{IHb}	Address & Control Input Hold Time		1.15	-	1.15	-	1.15	-	ns
t_{DQSCKb}	DQS Output Data Access Time from CK/CK#		2	10	2	10	2	10	ns
t_{DQSQb}	Data Strobe Edge to Ouput Data Edge tDQSQb		-	1.2	-	1.2	-	1.2	ns
t_{QHSb}	Data Hold Skew Factor		-	1.2	-	1.2	-	1.2	ns
Temperature De-Rating[16]									
t_{DQSCK}	t_{DQSCK} derating		-	5.62	-	6	-	6	ns
t_{RCD}	Core Timings Temperature De-Rating		**Min:** t_{RCD} + 1.875						ns
t_{RC}			**Min:** t_{RC} + 1.875						ns
t_{RAS}			**Min:** t_{RAS} + 1.875						ns
t_{RP}			**Min:** t_{RP} + 1.875						ns
t_{RRD}			**Min:** t_{RRD} + 1.875						ns

Notes:

1. Frequency values are for reference only. Clock cycle time (tCK) is used to determine device capabilities.
2. All AC timings assume an input slew rate of 1 V/ns.
3. READ, WRITE, and input setup and hold values are referenced to VREF.
4. tDQSCKDS is the absolute value of the difference between any two tDQSCK measurements (in a byte lane) within a contiguous sequence of bursts in a 160ns rolling window. tDQSCKDS is not tested and is guaranteed by design. Temperature drift in the system is <10 ◦C/s. Values do not include clock jitter.
5. tDQSCKDM is the absolute value of the difference between any two tDQSCK measurements (in a byte lane) within a 1.6us rolling window. tDQSCKDM is not tested and is guaranteed by design. Temperature drift in the system is <10 ◦C/s. Values do not include clock jitter.
6. tDQSCKDL is the absolute value of the difference between any two tDQSCK measurements (in a byte lane) within a 32ms rolling window. tDQSCKDL is not tested and is guaranteed by design. Temperature drift in the system is <10 ◦C/s. Values do not include clock jitter.

For LOW-to-HIGH and HIGH-to-LOW transitions, the timing reference is at the point when the signal crosses the transition threshold (VTT). tHZ and tLZ transitions occur in the same access time (with respect to clock) as valid data transitions. These parameters are not referenced to a specific voltage level but to the time when the device output is no longer driving (for tRPST, tHZ(DQS) and tHZ(DQ)), or begins driving (for tRPRE, tLZ(DQS), tLZ(DQ)). The figure below shows a method to calculate the point when the device is no longer driving tHZ(DQS) and tHZ(DQ) or begins driving tLZ(DQS) and tLZ(DQ) by measuring the signal at two different voltages. The actual voltage measurement points are not critical as long as the calculation is consistent. The parameters tLZ(DQS), tLZ(DQ), tHZ(DQS), and tHZ(DQ) are defined as single-ended. The timing parameters tRPRE and tRPST are determined from the differential signal DQS/DQS#.

Figure 6. Output Transition Timing



7. Measured from the point when DQS/DQS# begins driving the signal, to the point when DQS/DQS# begins driving the first rising strobe edge.
8. Measured from the last falling strobe edge of DQS/DQS# to the point when DQS/DQS# finishes driving the signal.
9. CKE input setup time is measured from CKE reaching a HIGH/LOW voltage level to CK/CK# crossing.
10. CKE input hold time is measured from CK/CK# crossing to CKE reaching a HIGH/LOW voltage level.
11. Input setup/hold time for signal (CA[9:0], CS#).
12. To ensure device operation before the device is configured, a number of AC boot timing parameters are defined in this table. The letter b is appended to the boot parameter symbols (for example, tCK during boot is tCKb).
13. Mobile LPDDR2 devices set some mode register default values upon receiving a RESET (MRW) command, as specified in Mode Register Definition.
14. The output skew parameters are measured with default output impedance settings using the reference load.
15. The minimum tCK column applies only when tCK is greater than 6ns.
16. Timing derating applies for operation at 85°C to 105°C when the requirement to derate is indicated by mode register 4 op-code (see the MR4 Device Temperature (MA[7:0] = 04h) table).
17. DRAM devices should be evenly addressed when being accessed. Disproportionate accesses to a particular row address may result in reduction of the product lifetime.
18. Clock Specification

    The jitter specified is a random jitter meeting a Gaussian distribution. Input clocks violating the min/max values may result in device malfunction.

Definitions:

- $t_{CK}(avg)$

  $t_{CK}(avg)$ is calculated as the average clock period across any consecutive 200 cycle window.

$$t_{CK}(avg) = \left[\sum_{j=1}^{N} t_{CK_j}\right] / N \quad \text{where N=200}$$

- $t_{CH}(avg)$ and $t_{CL}(avg)$

  $t_{CH}(avg)$ is defined as the average HIGH pulse width, as calculated across any consecutive 200 HIGH pulses.

$$t_{CH}(avg) = \left[\sum_{j=1}^{N} t_{CH_j}\right] / \left(N \times t_{CK}(avg)\right) \quad \text{where N=200}$$

- t_{CL}(avg) is defined as the average LOW pulse width, as calculated across any consecutive 200 LOW pulses.

$$t_{CL}(avg) = \left[\sum_{j=1}^{N} t_{CL_j}\right] / \left(N \times t_{CK}(avg)\right) \quad \text{where N=200}$$

- t_{JIT}(per)
  t_{JIT}(per) is the single period jitter defined as the largest deviation of any single tCK from t_{CK}(avg).
  t_{JIT}(per) = Min/max of {t_{CKi}- t_{CK}(avg) where i=1 to 200}
  t_{JIT}(per), act is the actual clock jitter for a given system.
  t_{JIT}(per), allowed is the specified allowed clock period jitter.
  t_{JIT}(per), is not subject to production test.

- t_{JIT}(cc)
  t_{JIT}(cc) is defined as the absolute difference in clock period between two consecutive clock cycles.
  t_{JIT}(cc) = Max of |{tCKi +1 - tCKi}.
  t_{JIT}(cc) defines the cycle to cycle jitter.
  t_{JIT}(cc) is not subject to production test.

- t_{JIT}(duty)
  t_{JIT} (duty) is defined with absolute and average specification of t_{CH} / t_{CL}.

- t_{ERR}(2per), t_{ERR} (3per), t_{ERR} (4per), t_{ERR} (5per), t_{ERR} (6-10per) and t_{ERR} (11-50per)
  t_{ERR} is defined as the cumulative error across multiple consecutive cycles from t_{CK}(avg).

$$t_{ERR}(\text{nper}) = \left[\sum_{j=1}^{i+N-1} t_{CK_j}\right] - \left(N \times t_{CK}(avg)\right) \quad \text{where} \begin{cases} n=2 & \text{for } t_{ERR}(2per) \\ n=3 & \text{for } t_{ERR}(3per) \\ n=4 & \text{for } t_{ERR}(4per) \\ n=5 & \text{for } t_{ERR}(5per) \\ 6 \le n \le 10 & \text{for } t_{ERR}(6-10per) \\ 11 \le n \le 50 & \text{for } t_{ERR}(11-50per) \end{cases}$$

Definition for tCK(abs), tCH(abs) and tCL(abs)
These parameters are specified per their average values, however it is understood that the following relationship between the average timing and the absolute instantaneous timing holds at all times.

Table 51. Definition for tCK(abs), tCH(abs) and tCL(abs)

Parameter	Symbol	Min.	Unit
Absolute clock period	t_{CK} (abs)	t_{CK}(avg),min + t_{JIT}(per),min	ps
Absolute clock HIGH pulse width	t_{CH} (abs)	t_{CH}(avg),min + t_{JIT}(duty),min / t_{CK}(avg)min	ps
Absolute clock LOW pulse width	t_{CL} (abs)	t_{CL}(avg),min + t_{JIT}(duty),min / t_{CK}(avg)min	ps

Notes:

1. tCK(avg),min is expressed is ps for this table.
2. tJIT(duty),min is a negative value.

19. CA and CS# Setup, Hold, and Derating

For all input signals (CA and CS#), the total required setup time (tIS) and hold time (tIH) is calculated by adding the data sheet tIS (base) and tIH (base) values to the ΔtIS and ΔtIH derating values, respectively.
Example: tIS (total setup time) = tIS(base) + ΔtIS. (See the series of tables following this section.)

Table 52. CA and CS# Setup and Hold Base Values

Unit [ps]	LPDDR2						Reference
	1066	933	800	667	533	466	
t_{IS} (base)	0	30	70	150	240	300	$V_{IH}/V_{IL}(AC) = V_{REF}(DC) \pm 220mV$
t_{IH} (base)	90	120	160	240	330	390	$V_{IH}/V_{IL}(DC) = V_{REF}(DC) \pm 130mV$

Unit [ps]	LPDDR2				Reference
	400	333	255	200	
t_{IS} (base)	300	440	600	850	$V_{IH}/V_{IL}(AC) = V_{REF}(DC) \pm 300mV$
t_{IH} (base)	400	540	700	950	$V_{IH}/V_{IL}(DC) = V_{REF}(DC) \pm 200mV$

Notes: AC/DC referenced for 1 V/ns CA and CS# slew rate, and 2 V/ns differential CK/CK# slew rate.

Table 53. Derating Values for AC/DC-Based tIS/tIH (AC220)

		CK, CK# Differential Slew Rate															
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
		△tIS	△tIH	△tIS	△tIH	△tIS	△tIH	△tIS	△tIH	△tIS	△tIH	△tIS	△tIH	△tIS	△tIH	△tIS	△tIH
CA, CS# slew rate V/ns	2.0	110	65	110	65	110	65	-	-	-	-	-	-	-	-	-	-
	1.5	74	43	73	43	73	43	89	59	-	-	-	-	-	-	-	-
	1.0	0	0	0	0	0	0	16	16	32	32	-	-	-	-	-	-
	0.9	-	-	-3	-5	-3	-5	13	11	29	27	45	43	-	-	-	-
	0.8	-	-	-	-	-8	-13	8	3	24	19	40	35	56	55	-	-
	0.7	-	-	-	-	-	-	2	-6	18	10	34	26	50	46	66	78
	0.6	-	-	-	-	-	-	-	-	10	-3	26	13	42	33	58	65
	0.5	-	-	-	-	-	-	-	-	-	-	4	-4	20	16	36	48
	0.4	-	-	-	-	-	-	-	-	-	-	-	-	-7	2	17	34

Table 54. Derating Values for AC/DC-Based tIS/tIH (AC300)

		CK, CK# Differential Slew Rate															
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
		△tIS	△tIH	△tIS	△tIH	△tIS	△tIH	△tIS	△tIH	△tIS	△tIH	△tIS	△tIH	△tIS	△tIH	△tIS	△tIH
CA, CS# slew rate V/ns	2.0	150	100	150	100	150	100	-	-	-	-	-	-	-	-	-	-
	1.5	100	67	100	67	100	67	116	83	-	-	-	-	-	-	-	-
	1.0	0	0	0	0	0	0	16	16	32	32	-	-	-	-	-	-
	0.9	-	-	-4	-8	-4	-8	12	8	28	24	44	40	-	-	-	-
	0.8	-	-	-	-	-12	-20	4	-4	20	12	36	28	52	48	-	-
	0.7	-	-	-	-	-	-	-3	-18	13	-2	29	14	45	34	61	66
	0.6	-	-	-	-	-	-	-	-	2	-21	18	-5	34	15	50	47
	0.5	-	-	-	-	-	-	-	-	-	-	-12	-32	4	-12	20	20
	0.4	-	-	-	-	-	-	-	-	-	-	-	-	-35	-40	-11	-8

20. Data Setup, Hold, and Slew Rate Derating

For all input signals (DQ, DM) calculate the total required setup time (tDS) and hold time (tDH) by adding the data sheet tDS(base) and tDH(base) values to the ΔtDS and ΔtDH derating values, respectively.
Example: tDS = tDS(base) + ΔtDS.

Table 55. Data Setup and Hold Base Values

Unit [ps]	LPDDR2						Reference
	1066	900	800	667	533	466	
t_{DS} (base)	-10	15	50	130	210	230	$V_{IH}/V_{IL}(AC) = V_{REF}(DC) \pm 220mV$
t_{DH} (base)	80	105	140	220	300	320	$V_{IH}/V_{IL}(DC) = V_{REF}(DC) \pm 130mV$

Unit [ps]	LPDDR2				Reference
	400	333	255	200	
t_{DS} (base)	180	300	450	700	$V_{IH}/V_{IL}(AC) = V_{REF}(DC) \pm 300mV$
t_{DH} (base)	280	400	550	800	$V_{IH}/V_{IL}(DC) = V_{REF}(DC) \pm 200mV$

Notes: AC/DC referenced for 1 V/ns DQ, DM slew rate, and 2 V/ns differential DQS/DQS# slew rate.

Table 56. Derating Values for AC/DC-Based tDS/tDH (AC220)

		DQS, DQS# Differential Slew Rate															
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
		△tDS	△tDH	△tDS	△tDH	△tDS	△tDH	△tDS	△tDH	△tDS	△tDH	△tDS	△tDH	△tDS	△tDH	△tDS	△tDH
DQ, DM slew rate V/ns	2.0	110	65	110	65	110	65	-	-	-	-	-	-	-	-	-	-
	1.5	74	43	73	43	73	43	89	59	-	-	-	-	-	-	-	-
	1.0	0	0	0	0	0	0	16	16	32	32	-	-	-	-	-	-
	0.9	-	-	-3	-5	-3	-5	13	11	29	27	45	43	-	-	-	-
	0.8	-	-	-	-	-8	-13	8	3	24	19	40	35	56	55	-	-
	0.7	-	-	-	-	-	-	2	-6	18	10	34	26	50	46	66	78
	0.6	-	-	-	-	-	-	-	-	10	-3	26	13	42	33	58	65
	0.5	-	-	-	-	-	-	-	-	-	-	4	-4	20	16	36	48
	0.4	-	-	-	-	-	-	-	-	-	-	-	-	-7	2	17	34

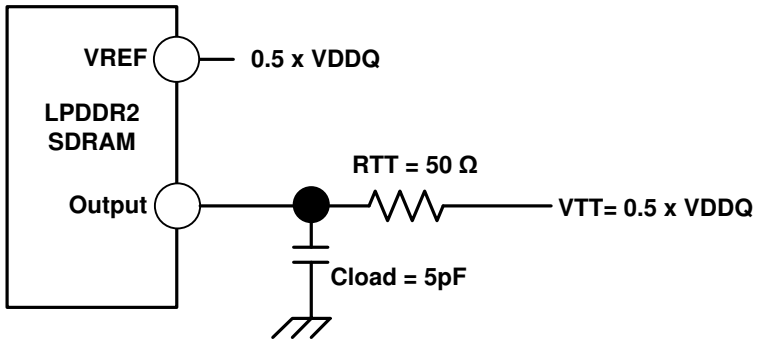
Table 57. Derating Values for AC/DC-Based tDS/tDH (AC300)

		CK, CK# Differential Slew Rate															
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
		△tDS	△tDH	△tDS	△tDH	△tDS	△tDH	△tDS	△tDH	△tDS	△tDH	△tDS	△tDH	△tDS	△tDH	△tDS	△tDH
DQ, DM slew rate V/ns	2.0	150	100	150	100	150	100	-	-	-	-	-	-	-	-	-	-
	1.5	100	67	100	67	100	67	116	83	-	-	-	-	-	-	-	-
	1.0	0	0	0	0	0	0	16	16	32	32	-	-	-	-	-	-
	0.9	-	-	-4	-8	-4	-8	12	8	28	24	44	40	-	-	-	-
	0.8	-	-	-	-	-12	-20	4	-4	20	12	36	28	52	48	-	-
	0.7	-	-	-	-	-	-	-3	-18	13	-2	29	14	45	34	61	66
	0.6	-	-	-	-	-	-	-	-	2	-21	18	5	34	15	50	47
	0.5	-	-	-	-	-	-	-	-	-	-	-12	-32	4	-12	20	20
	0.4	-	-	-	-	-	-	-	-	-	-	-	-	-35	-40	-11	-8

21. HSUL_12 Driver Output Timing Reference Load

The below figure represents the timing reference load used in defining the relevant timing parameters of the part.
It is not intended to be either a precise representation of the typical system environment or a depiction of the actual load presented by a production tester.

Figure 7. HSUL_12 Driver Output Reference Load for Timing and Slew Rate



22. RON_{PU} and RON_{PD} Resistor Definition

$$RONPU = \frac{(VDDQ - Vout)}{ABS\ (Iout)}$$

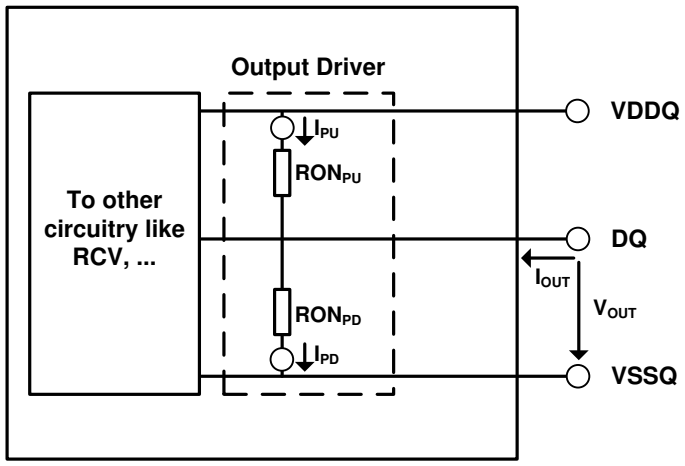
NOTE: This is under the condition that RON_{PD} is turned off

$$RONPD = \frac{(Vout)}{ABS\ (Iout)}$$

NOTE: This is under the condition that RON_{PU} is turned off

Figure 8. Output Driver: Definition of Voltages and Currents

Chip in Drive Mode



23. Output Driver Temperature and Voltage Sensitivity

If temperature and/or voltage change after calibration, the tolerance limits widen according to the Tables shown below.

Table 58. Output Driver Sensitivity Definition

Resistor	Vout	Min	Max	Unit	Note
RON_{PD}	0.5 x V_{DDQ}	85 - (dRONdT x |ΔT|) - (dRONdV x |ΔV|)	115 + (dRONdT x |ΔT|) + (dRONdV x |ΔV|)	%	a,b
RON_{PU}					

NOTE:

a. ΔT = T – T (@ calibration), ΔV = V – V (@ calibration)

b. dRONdT and dRONdV are not subject to production test but are verified by design and characterization.

Table 59. Output Driver Temperature and Voltage Sensitivity

Symbol	Parameter	Min	Max	Unit
dRONdT	RON Temperature Sensitivity	0.00	0.75	%/°C
dRONdV	RON Voltage Sensitivity	0.00	0.20	%/mV

24. RON_{PU} and RON_{PD} Characteristics without ZQ Calibration

Output driver impedance RON is defined by design and characterization as default setting.

Table 60. Output Driver DC Electrical Characteristics without ZQ Calibration

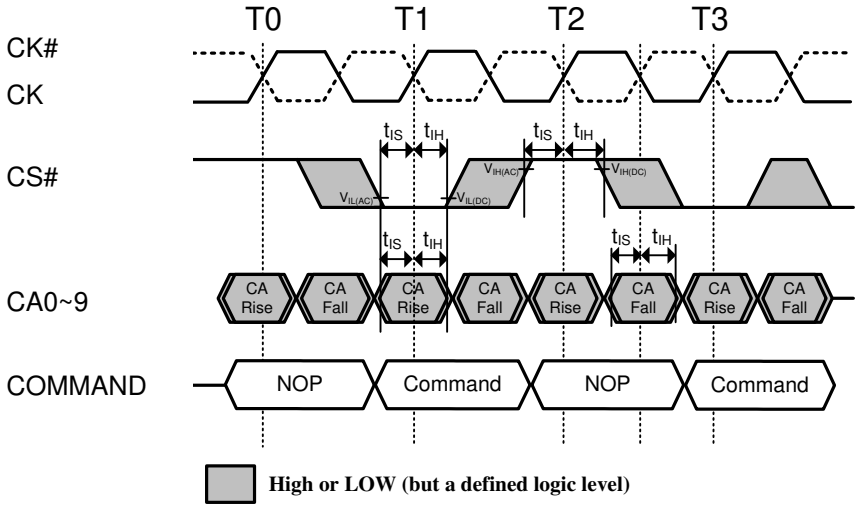
RON_{NOM}	Resistor	Vout	Min	Nom	Max	Unit	Note
34.3Ω	RON34PD	0.5 x V_{DDQ}	24	34.3	44.6	Ω	a
	RON34PU	0.5 x V_{DDQ}	24	34.3	44.6	Ω	a
40.0Ω	RON40PD	0.5 x V_{DDQ}	28	40	52	Ω	a
	RON40PU	0.5 x V_{DDQ}	28	40	52	Ω	a
48.0Ω	RON48PD	0.5 x V_{DDQ}	33.6	48	62.4	Ω	a
	RON48PU	0.5 x V_{DDQ}	33.6	48	62.4	Ω	a
60.0Ω	RON60PD	0.5 x V_{DDQ}	42	60	78	Ω	a
	RON60PU	0.5 x V_{DDQ}	42	60	78	Ω	a
80.0Ω	RON80PD	0.5 x V_{DDQ}	56	80	104	Ω	a
	RON80PU	0.5 x V_{DDQ}	56	80	104	Ω	a
120.0Ω (optional)	RON120PD	0.5 x V_{DDQ}	84	120	156	Ω	a
	RON120PU	0.5 x V_{DDQ}	84	120	156	Ω	a

NOTE:

a. Across entire operating temperature range, without calibration.

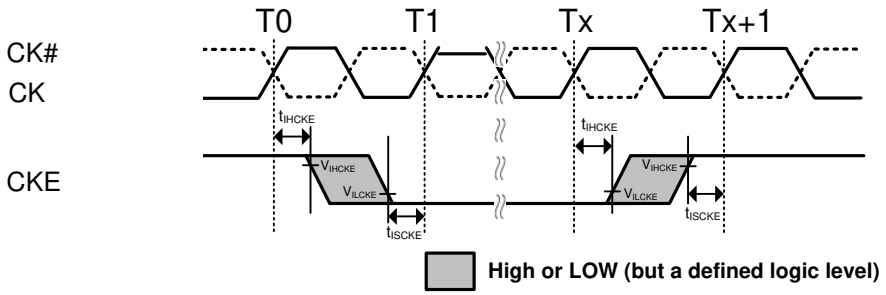
Timing Waveforms

Figure 9. Command Input Setup and Hold Timing



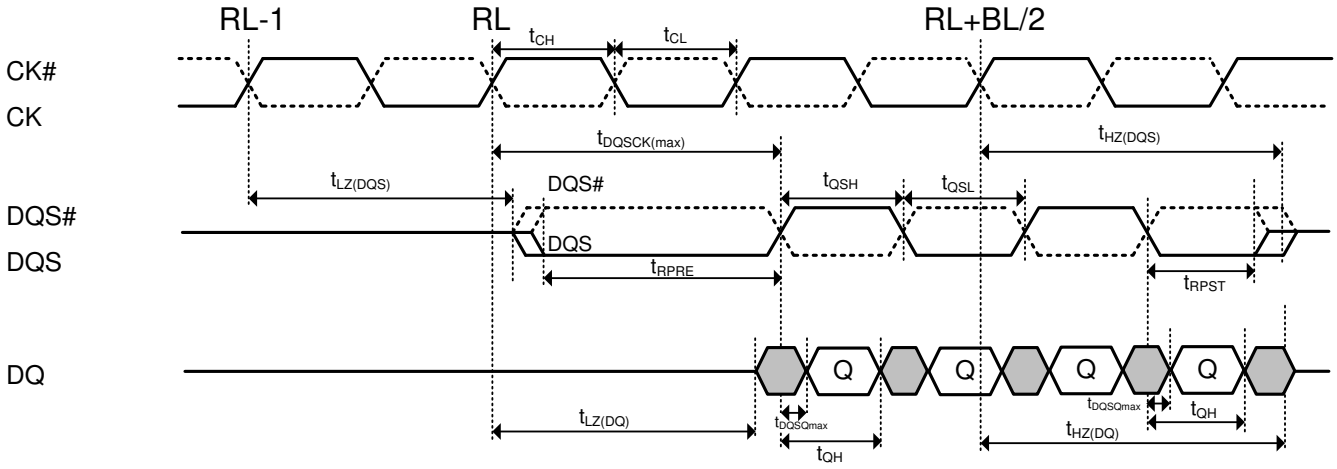
NOTES:
Setup and hold conditions also apply to the CKE pin. See section related to power down for timing diagrams related to the CKE pin.

Figure 10. CKE Input Setup and Hold Timing



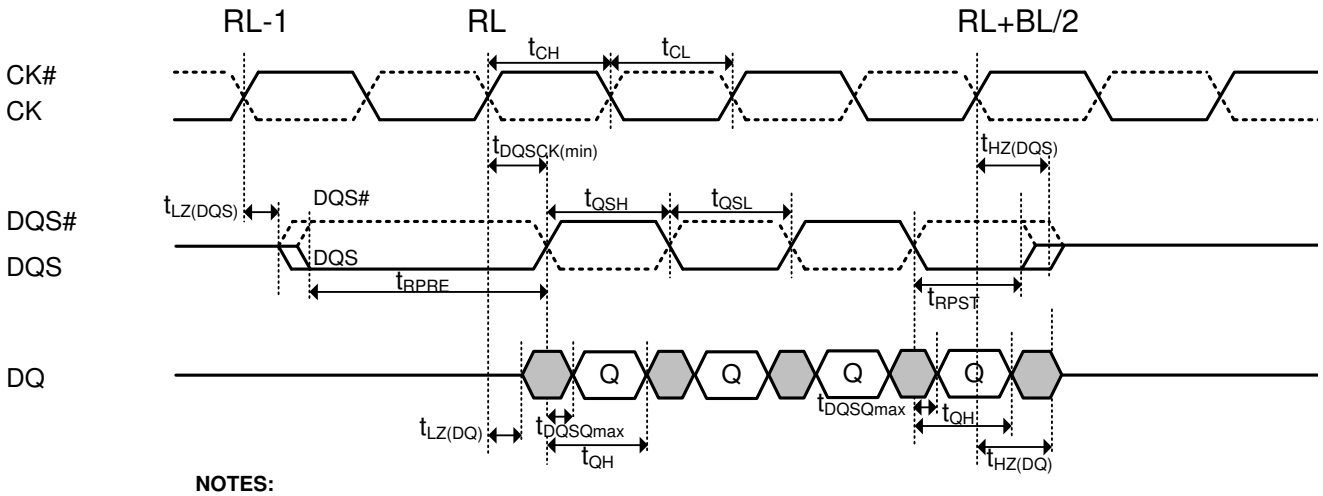
NOTES:
1. After CKE is registered LOW, CKE signal level shall be maintained below VILCKE for tCKE specification (LOW pulse width).
2. After CKE is registered HIGH, CKE signal level shall be maintained above VIHCKE for tCKE specification (HIGH pulse width).

Figure 11. Data output (read) timing (tDQSCKmax)



NOTES:
1. tDQSCK may span multiple clock periods.
2. An effective Burst Length of 4 is shown.

Figure 12. Data output (read) timing (tDQSCKmin)



NOTES:
1. An effective Burst Length of 4 is shown.

Figure 13. Burst read (RL = 5, BL = 4, tDQSCK > tCK)

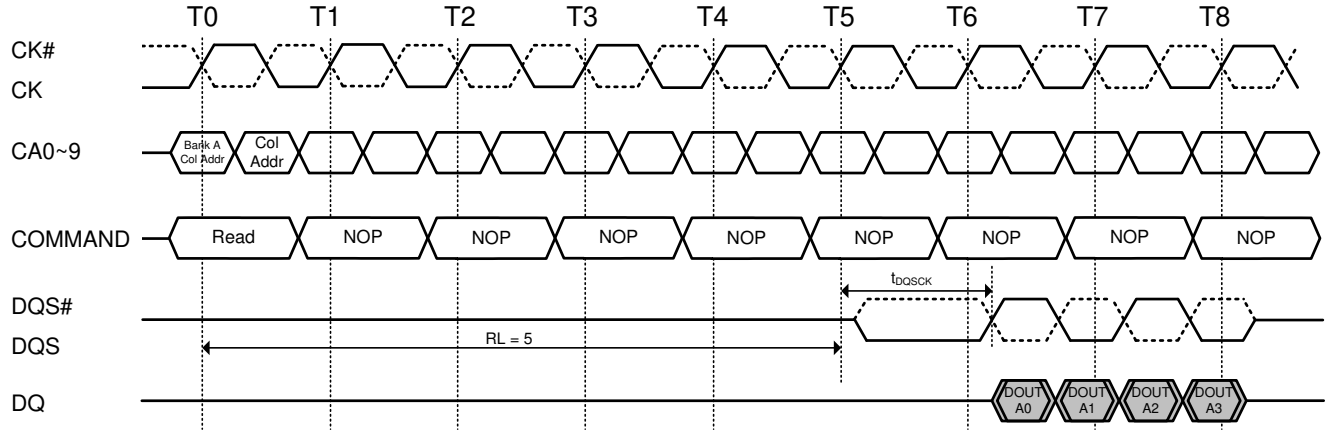


Figure 14. Burst read (RL = 3, BL = 8, tDQSCK < tCK)

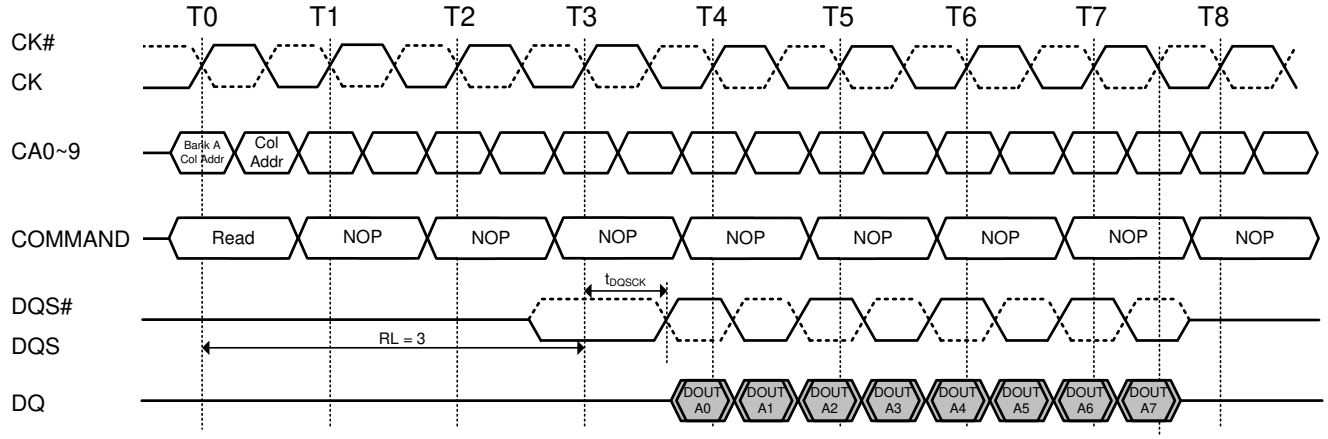
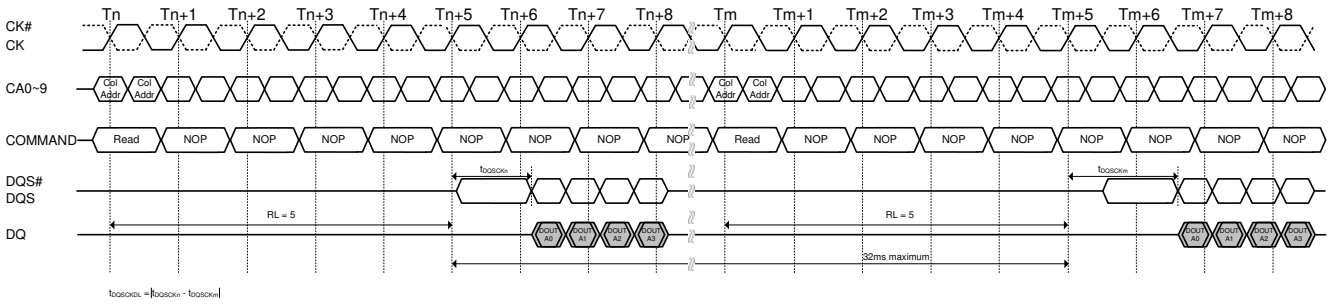
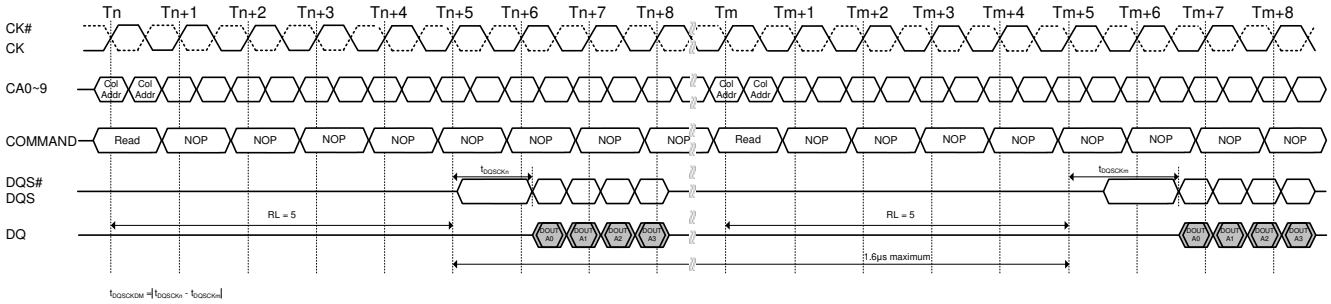


Figure 15. tDQSCKDL timing



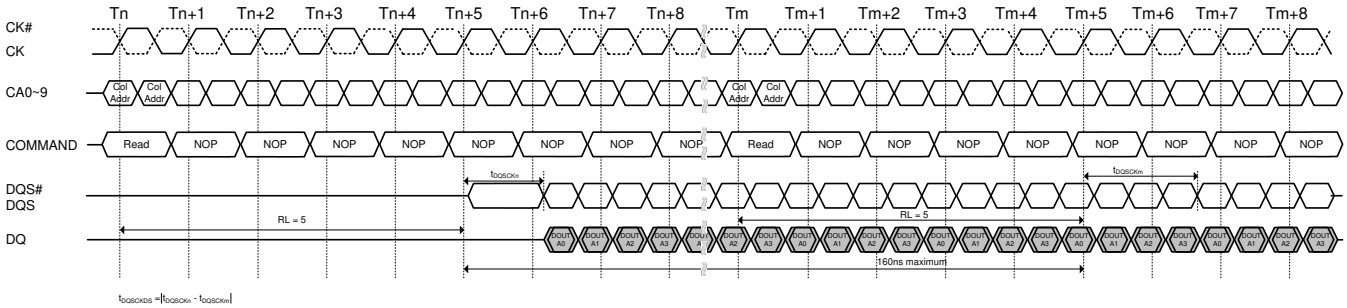
NOTES:
1. tDQSCKDLmax is defined as the maximum of ABS(tDQSCKn - tDQSCKm) for any {tDQSCKn, tDQSCKm} pair within any 32ms rolling window.

Figure 16. tDQSCKDM timing



NOTES:
1. tDQSCKDMmax is defined as the maximum of ABS(tDQSCKn - tDQSCKm) for any {tDQSCKn,tDQSCKm} pair within any 1.6µs rolling window.

Figure 17. tDQSCKDS timing



NOTES:
1. tDQSCKDSmax is defined as the maximum of ABS(tDQSCKn - tDQSCKm) for any {tDQSCKn, tDQSCKm} pair for reads within a consecutive burst within any 160ns rolling window.

Figure 18. Burst read followed by burst write (RL = 3, WL = 1, BL = 4)

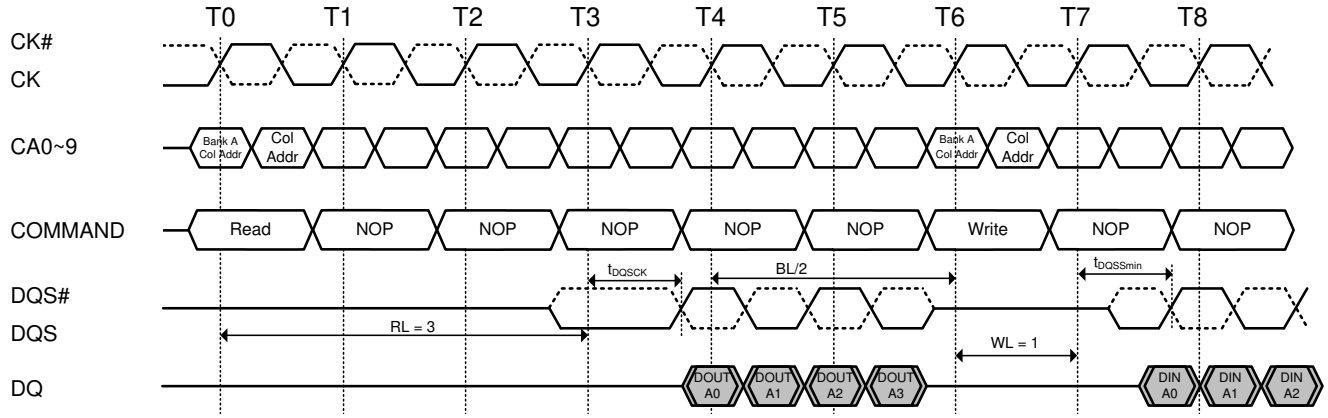


Figure 19. Seamless burst read (RL = 3, BL = 4, tCCD = 2)

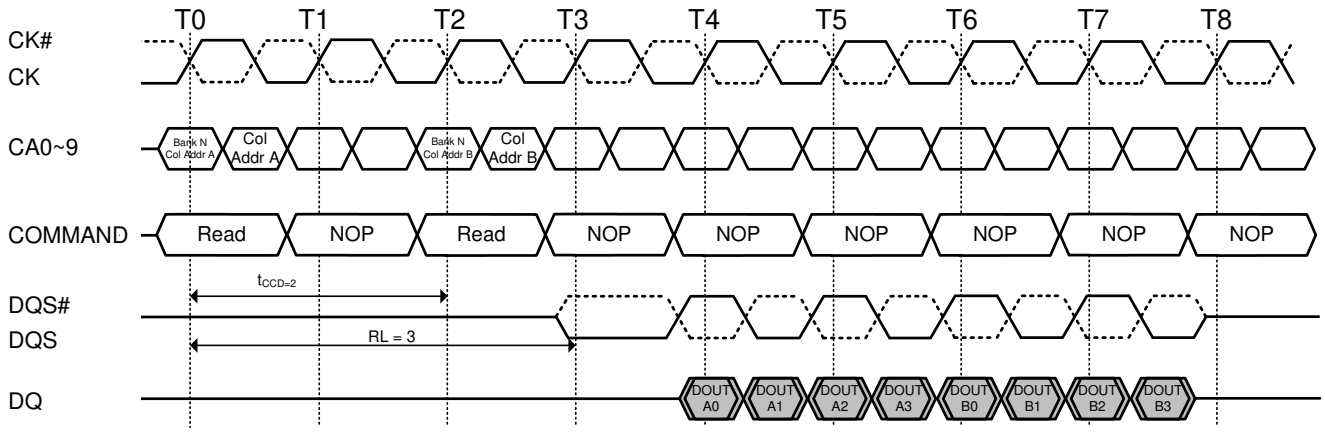
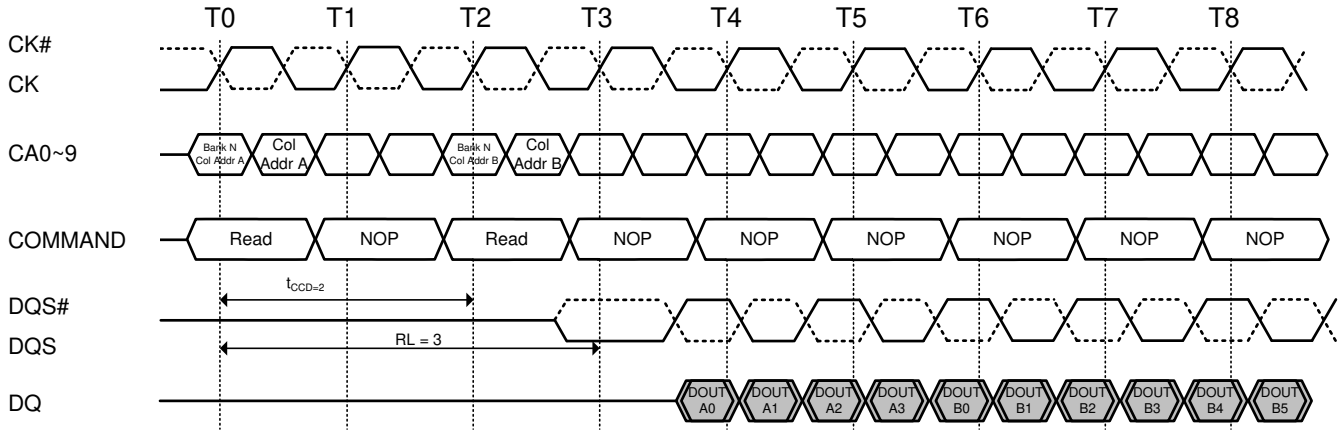


Figure 20. Read burst interrupt example (RL = 3, BL = 8, tCCD = 2)



NOTES:
1. For LPDDR2-S4 devices, read burst interrupt function is only allowed on burst of 8 and burst of 16.
2. For LPDDR2-S4 devices, read burst interrupt may only occur on even clock cycles after the previous read commands, provided that tCCD is met.
3. Reads can only be interrupted by other reads or the BST command.
4. Read burst interruption is allowed to any bank inside DRAM.
5. Read burst with Auto-Precharge is not allowed to be interrupted.
6. The effective burst length of the first read equals two times the number of clock cycles between the first read and the interrupting read.

Figure 21. Burst write (WL = 1, BL = 4)

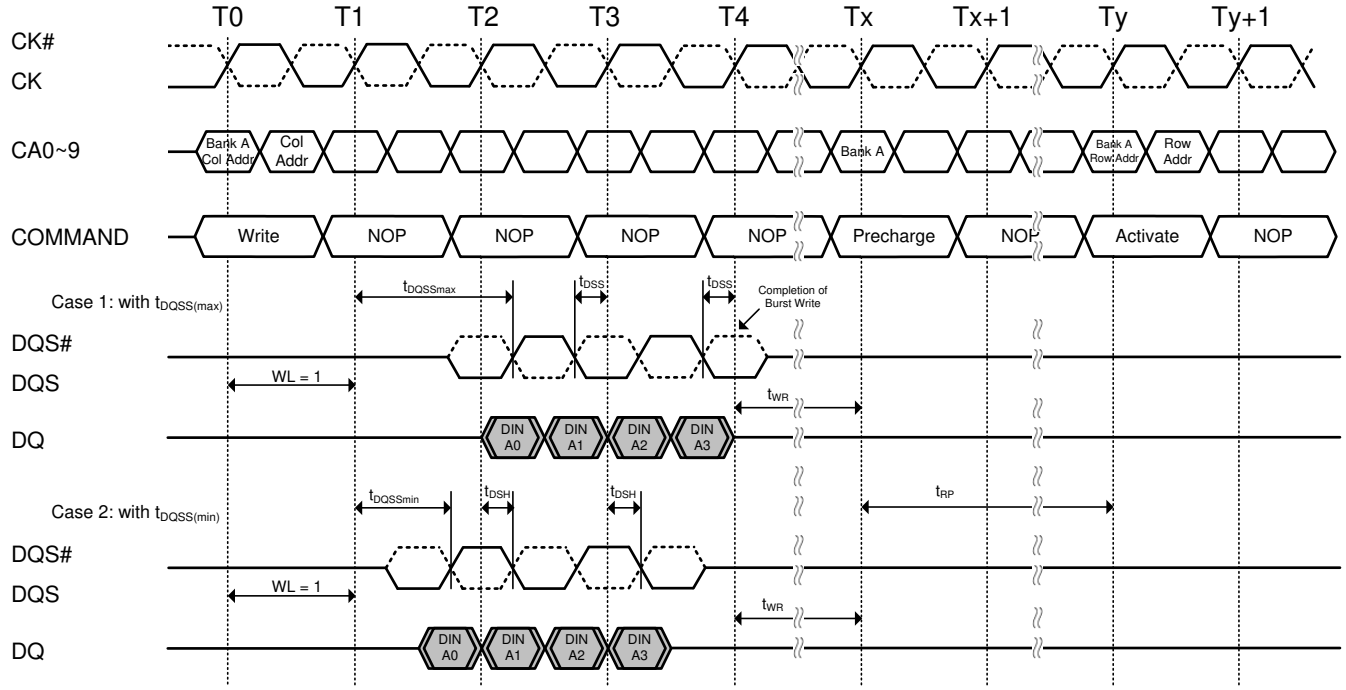
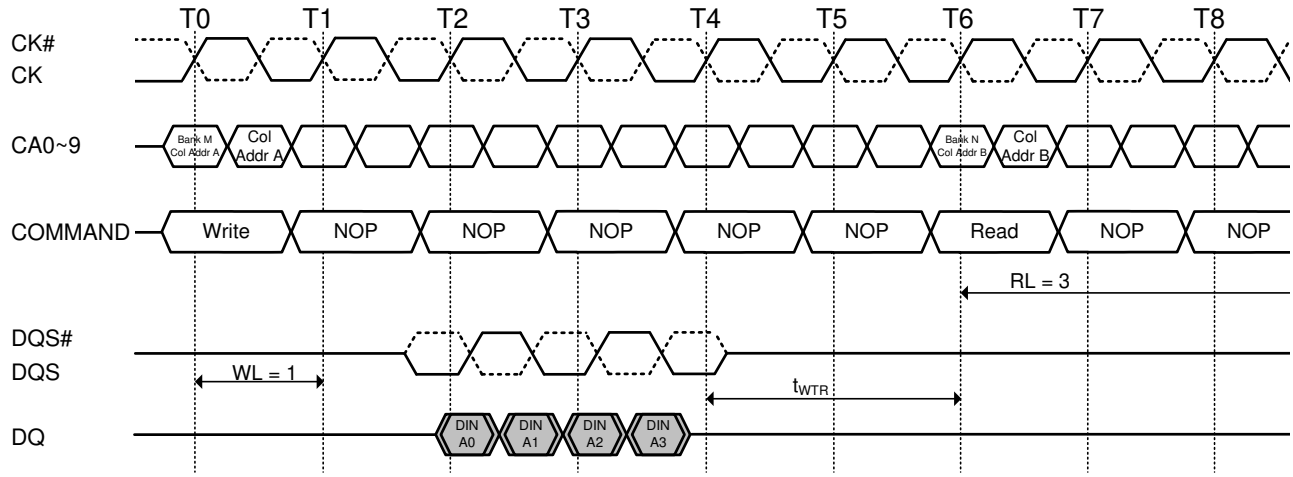


Figure 22. Burst write followed by burst read (RL=3, WL = 1, BL = 4)



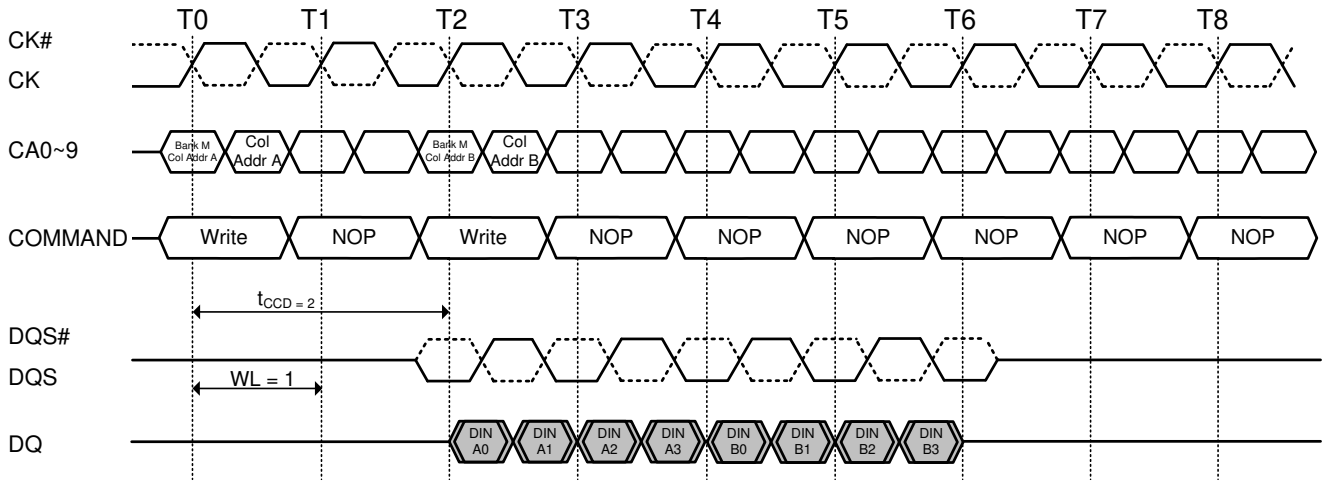
NOTES:

1. The minimum number of clock cycles from the burst write command to the burst read command for any bank is [WL + 1 + BL/2 + RU(tWTR/tCK)].

2. tWTR starts at the rising edge of the clock after the last valid input datum.

3. If a write burst is truncated with a Burst Terminate (BST) command, the effective burst length of the truncated write burst should be used as BL to calculate the minimum write to read delay.

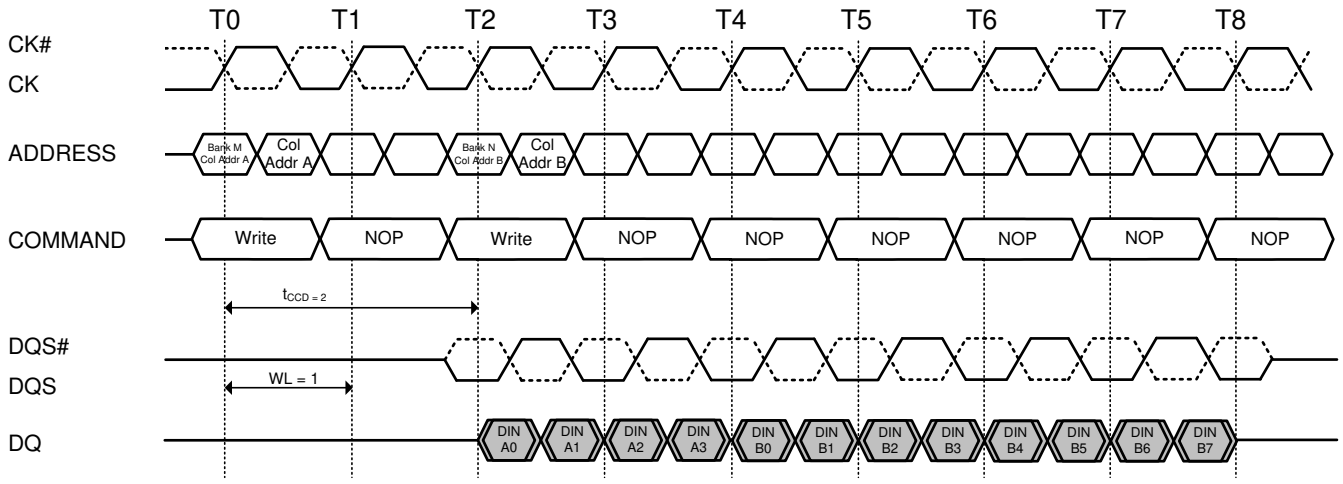
Figure 23. Seamless burst write (WL = 1, BL = 4, tCCD = 2)



NOTES:

1. The seamless burst write operation is supported by enabling a write command every other clock for BL = 4 operation, every four clocks for BL = 8 operation, or every eight clocks for BL=16 operation. This operation is allowed regardless of same or different banks as long as the banks are activated.

Figure 24. Write burst interrupt timing (WL = 1, BL = 8, tCCD = 2)



NOTES:

1. For LPDDR2-S4 devices, write burst interrupt function is only allowed on burst of 8 and burst of 16.

2. For LPDDR2-S4 devices, write burst interrupt may only occur on even clock cycles after the previous write commands, provided that tCCD(min) is met.

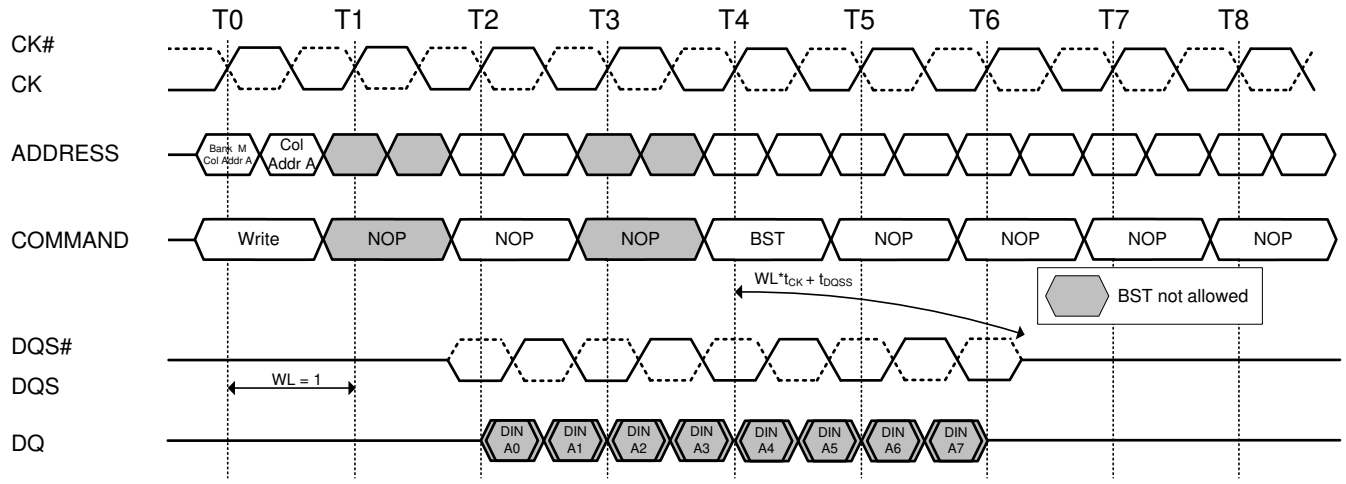
3. Writes can only be interrupted by other writes or the BST command.

4. Write burst interruption is allowed to any bank inside DRAM.

5. Write burst with Auto-Precharge is not allowed to be interrupted.

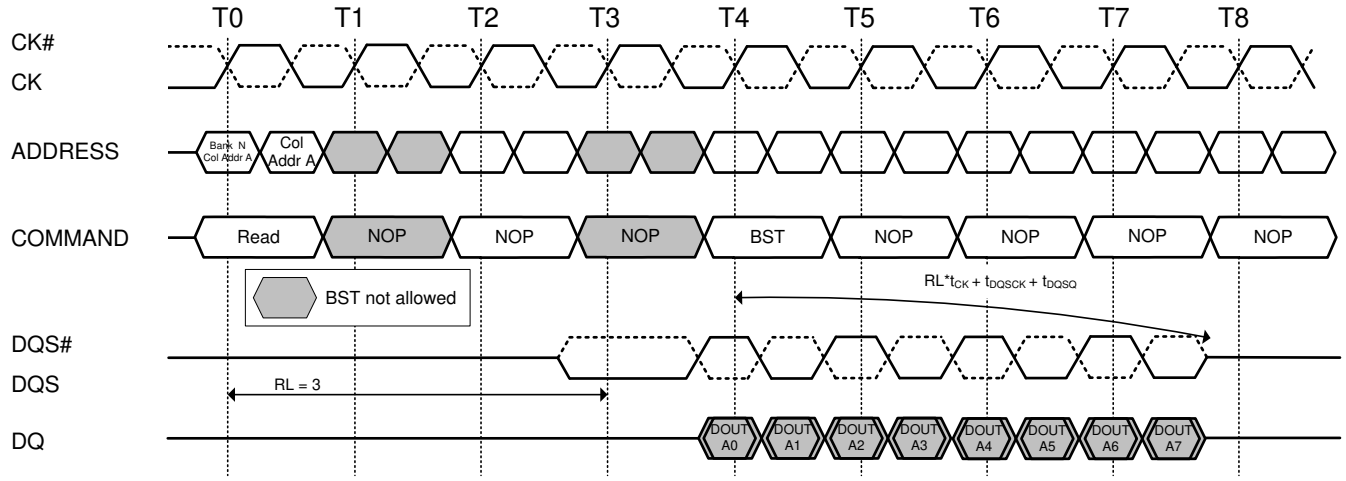
6. The effective burst length of the first write equals two times the number of clock cycles between the first write and the interrupting write.

Figure 25. Burst Write truncated by BST (WL = 1, BL = 16)



NOTES:
1. The BST command truncates an ongoing write burst WL * tCK + tDQSS after the rising edge of the clock where the Burst Terminate command is issued.
2. For LPDDR2-S4 devices, BST can only be issued an even number of clock cycles after the Write command.
3. Additional BST commands are not allowed after T4 and may not be issued until after the next Read or Write command.

Figure 26. Burst Read truncated by BST (RL=3, BL = 16)



NOTES:
1. The BST command truncates an ongoing read burst RL * tCK + tDQSCK + tDQSQ after the rising edge of the clock where the Burst Terminate command is issued.
2. For LPDDR2-S4 devices, BST can only be issued an even number of clock cycles after the Read command.
3. Additional BST commands are not allowed after T4 and may not be issued until after the next Read or Write command.

Figure 27. Write Data Mask

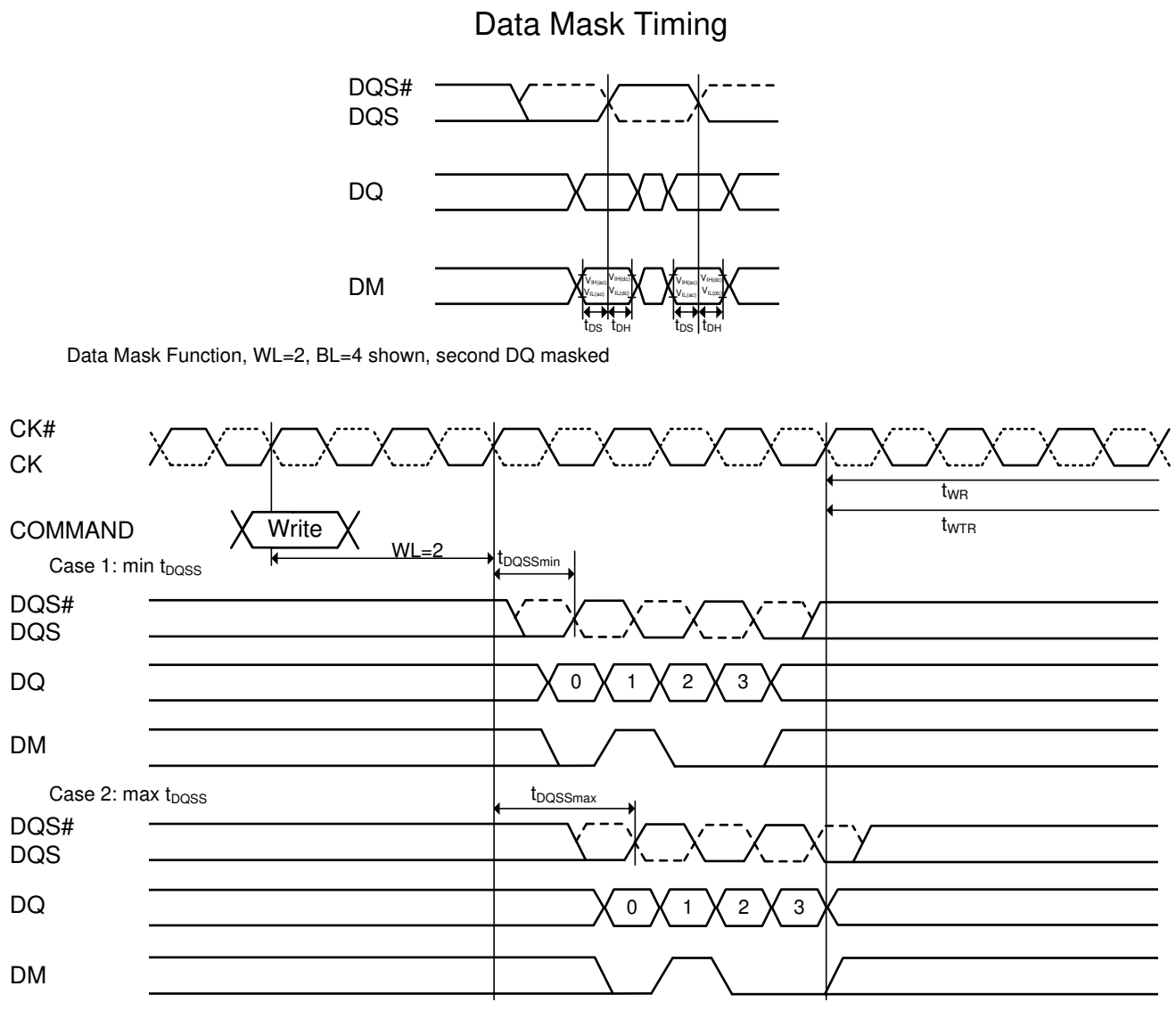


Figure 28. Burst read followed by precharge (RL = 3, BL = 8, RU(tRTP(min)/tCK) = 2)

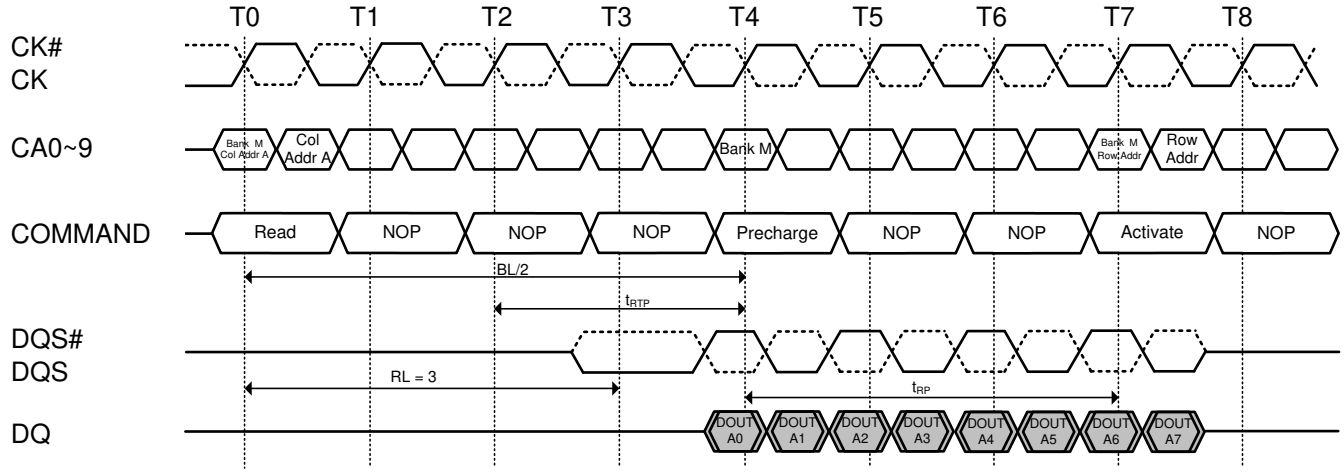


Figure 29. Burst read followed by precharge (RL = 3, BL = 4, RU(tRTP(min)/tCK) = 3)

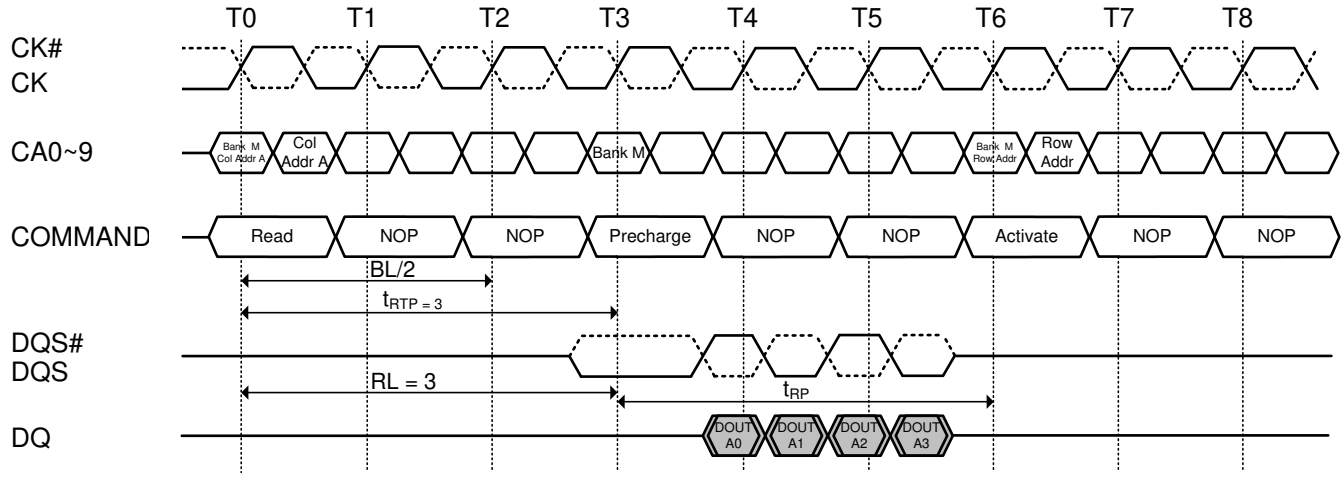


Figure 30. Burst write operation followed by precharge (WL = 1, BL = 4)

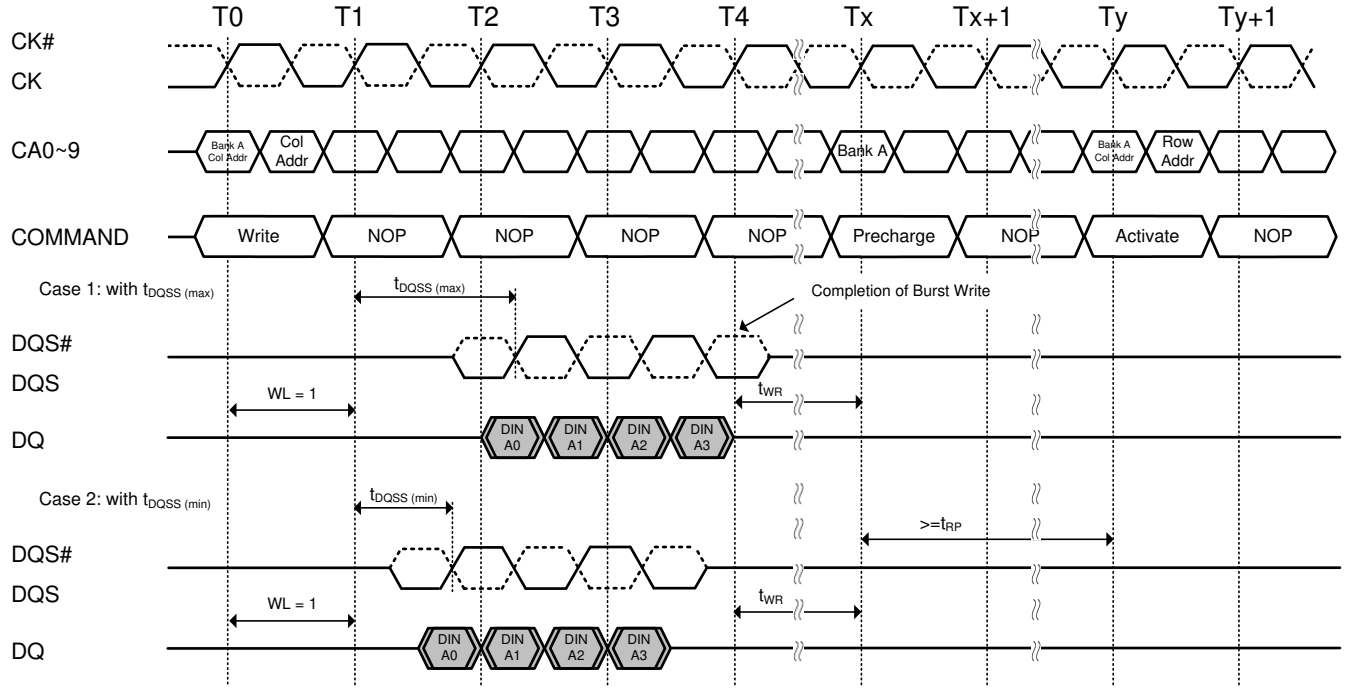


Figure 31. Burst read with auto-precharge (RL = 3, BL = 4, RU(tRTP(min)/tCK) = 2)

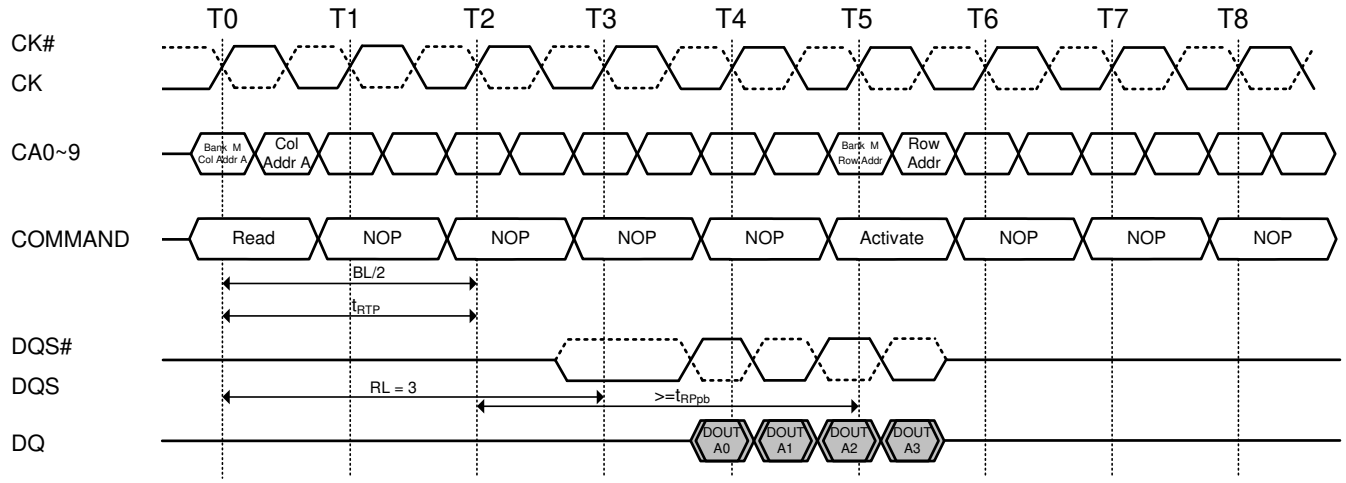


Figure 32. Burst write with auto-precharge (WL = 1, BL = 4)

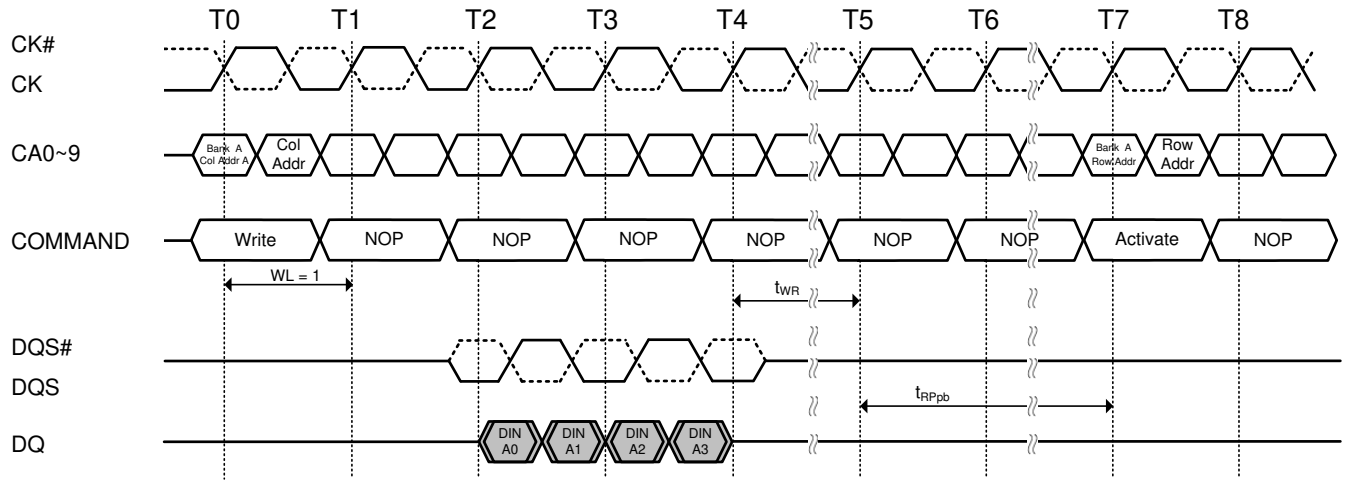


Figure 33. All Bank Refresh Operation

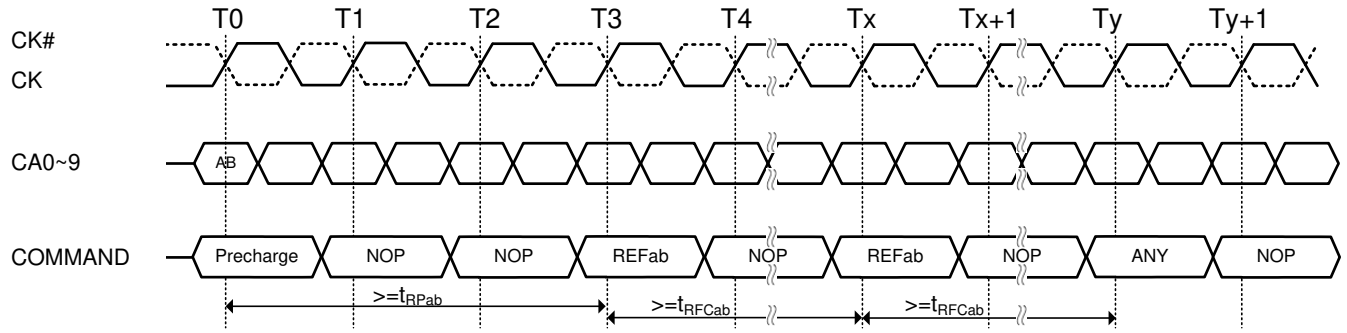
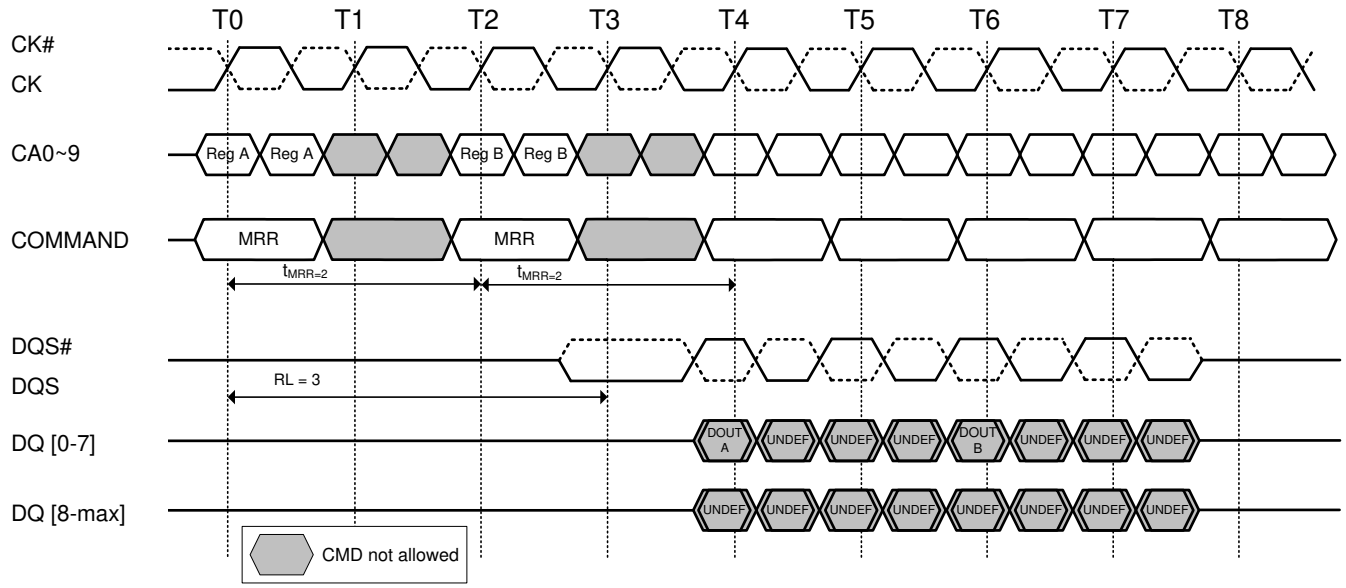
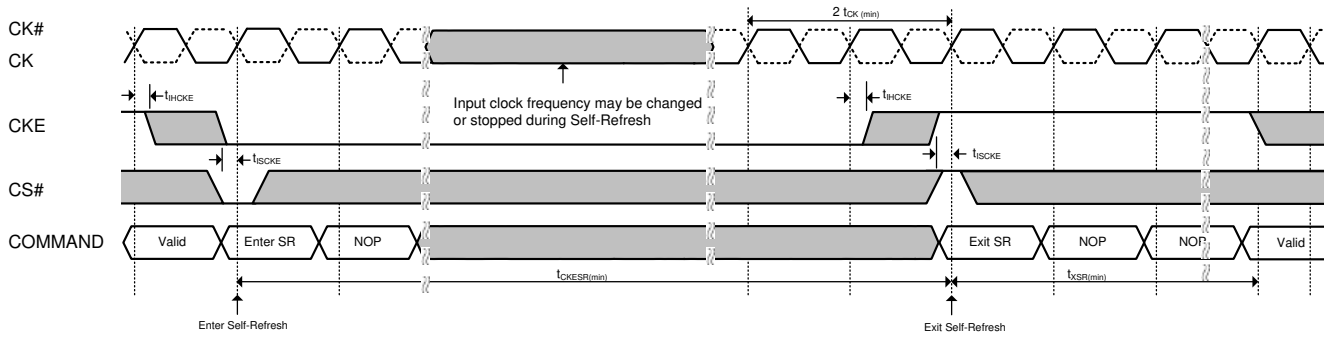


Figure 34. Mode Register Read timing (RL = 3, tMRR = 2)



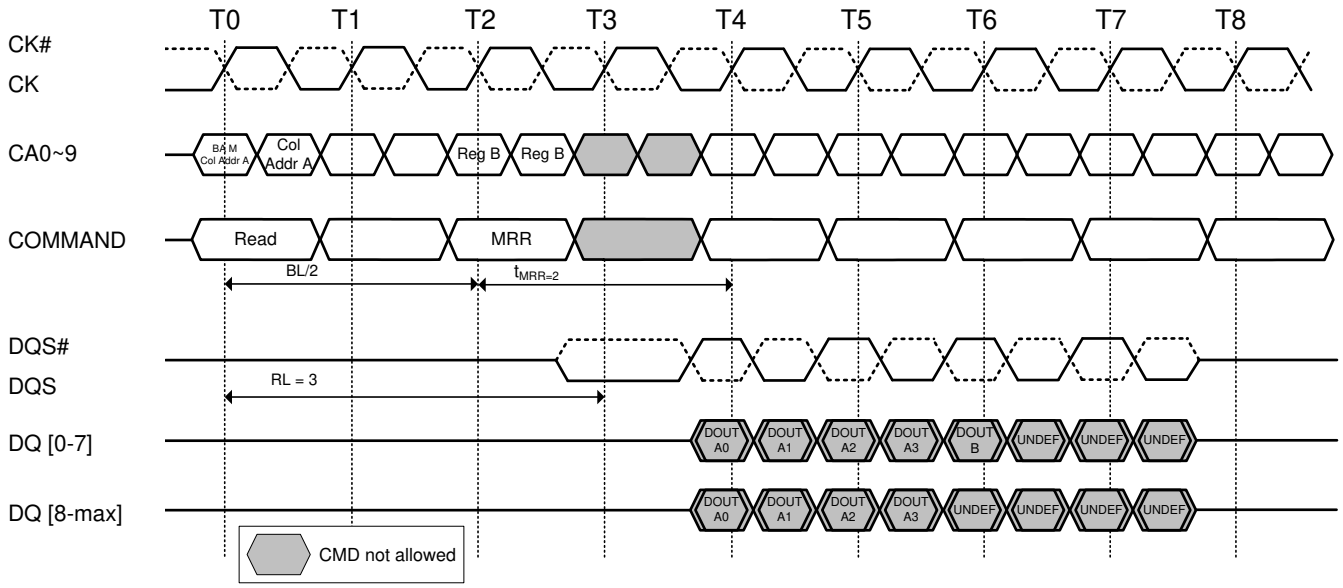
NOTES:
1. Mode Register Read has a burst length of four.
2. Mode Register Read operation shall not be interrupted.
3. Mode Register data is valid only on DQ[0-7] on the first beat. Subsequent beats contain valid, but undefined data. DQ[8-max] contain valid, but undefined data for the duration of the MRR burst.
4. The Mode Register Command period is tMRR. No command (other than Nop) is allowed during this period.
5. Mode Register Reads to DQ Calibration registers MR32 and MR40 are described in the section on DQ Calibration.
6. Minimum Mode Register Read to write latency is RL + RU(tDQSCKmax/tCK) + 4/2 + 1 - WL clock cycles.
7. Minimum Mode Register Read to Mode Register Write latency is RL + RU(tDQSCKmax/tCK) + 4/2 + 1 clock cycles.

Figure 35. Self-Refresh Operation



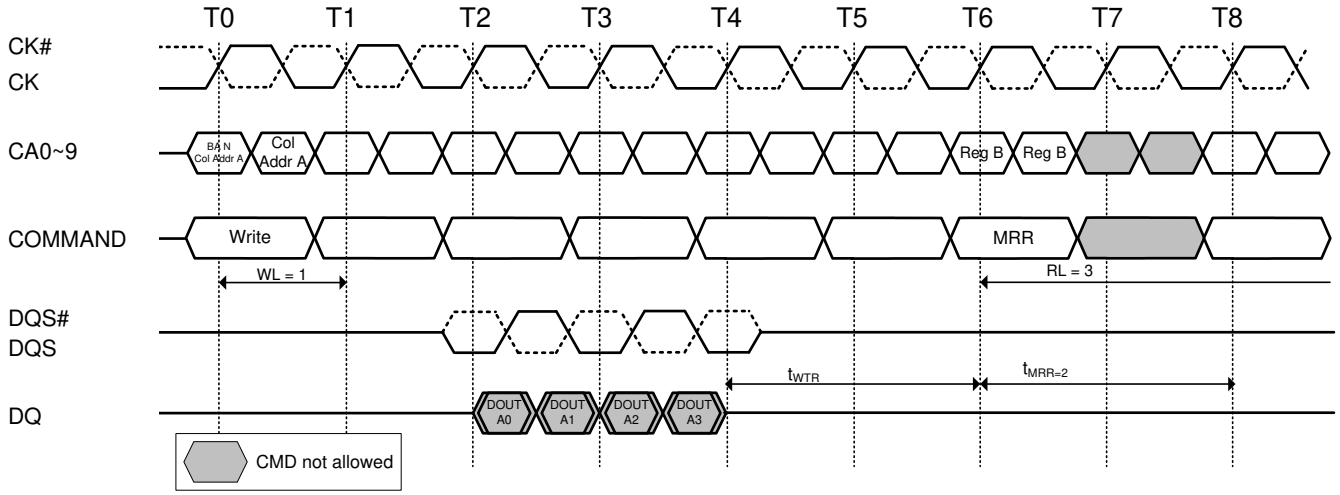
NOTES:
1. Input clock frequency may be changed or stopped during self-refresh, provided that upon exiting self-refresh, a minimum of 2 clocks of stable clock are provided and the clock frequency is between the minimum and maximum frequency for the particular speed grade.
2. Device must be in the "All banks idle" state prior to entering Self Refresh mode.
3. tXSR begins at the rising edge of the clock after CKE is driven HIGH.
4. A valid command may be issued only after tXSR is satisfied. NOPs shall be issued during tXSR.

Figure 36. Read to MRR timing (RL = 3, tMRR = 2)



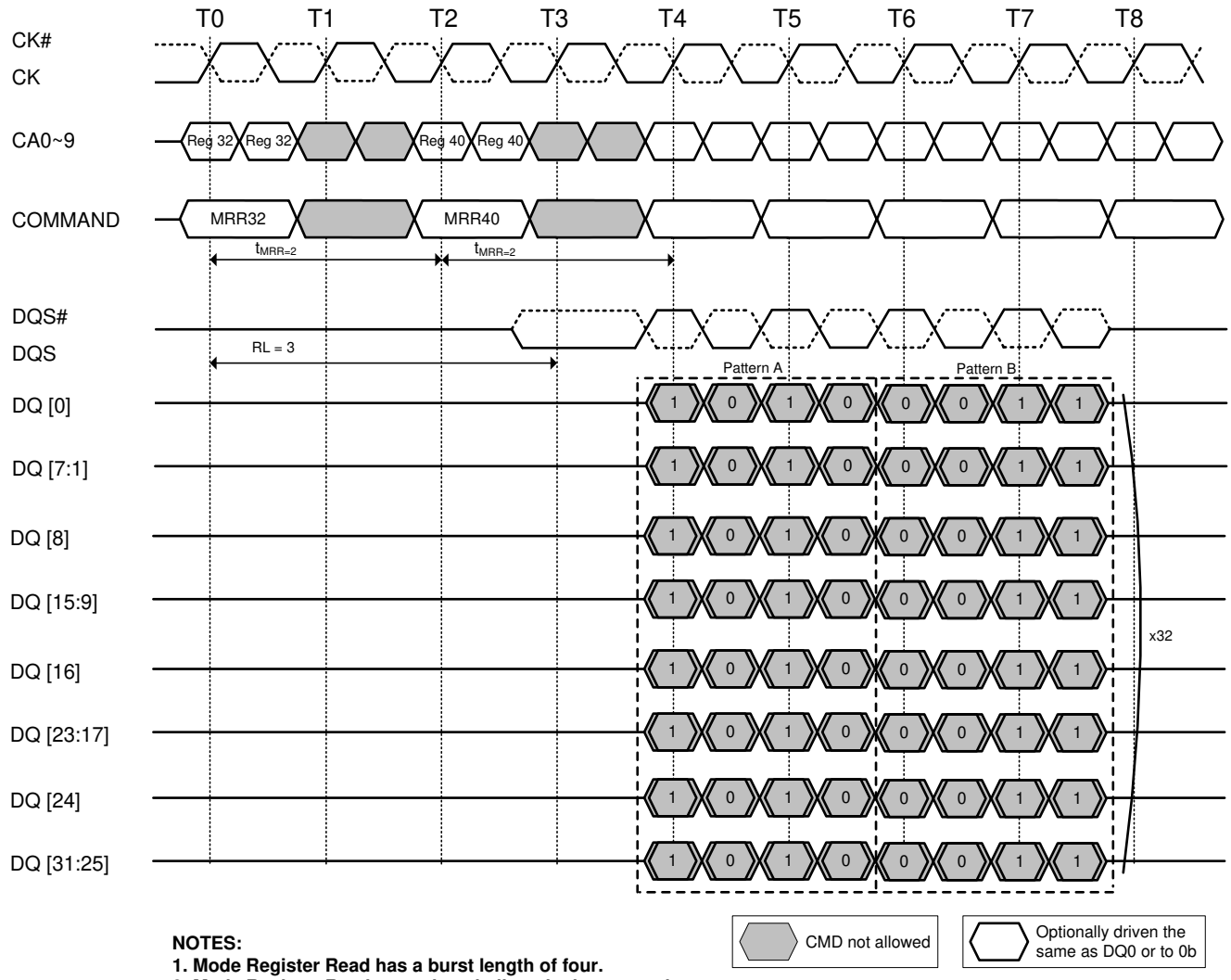
NOTES:
1. The minimum number of clocks from the burst read command to the Mode Register Read command is BL/2.
2. The Mode Register Read Command period is tMRR. No command (other than Nop) is allowed during this period.

Figure 37. Burst Write Followed by MRR (RL = 3, WL = 1, BL = 4)



NOTES:
1. The minimum number of clock cycles from the burst write command to the Mode Register Read command is [WL + 1 + BL/2 + RU(tWTR/tCK)].
2. The Mode Register Read Command period is tMRR. No command (other than Nop) is allowed during this period.

Figure 38. MR32 and MR40 DQ Calibration timing (RL = 3, tMRR = 2)



NOTES:

1. Mode Register Read has a burst length of four.

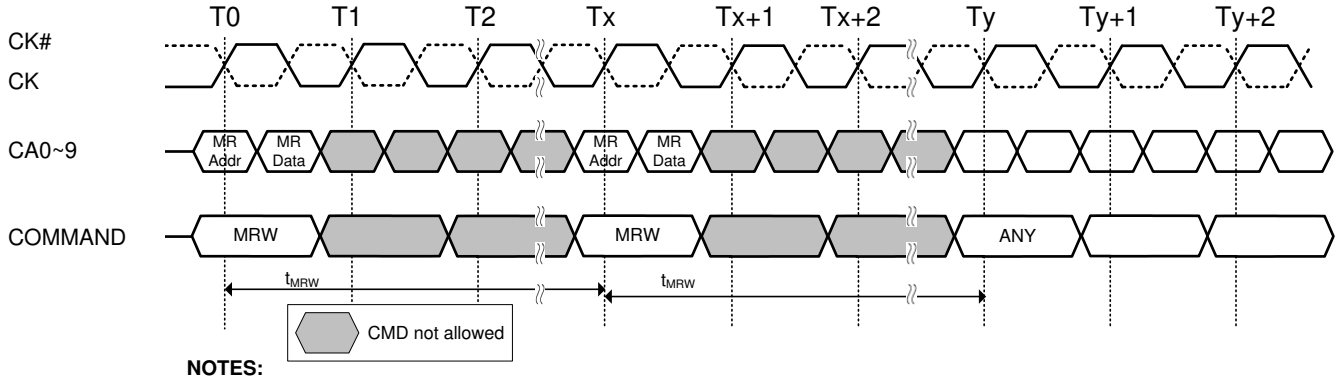
2. Mode Register Read operation shall not be interrupted.

3. Mode Register Reads to MR32 and MR40 drive valid data on DQ[0] during the entire burst. For x32 devices, DQ[8], DQ[16], and DQ[24] shall drive the same information as DQ[0] during the burst.

4. For x32 devices, DQ[7:1], DQ[15:9], DQ[23:17], and DQ[31:25] may optionally drive the same information as DQ[0] or they may drive 0b during the burst.

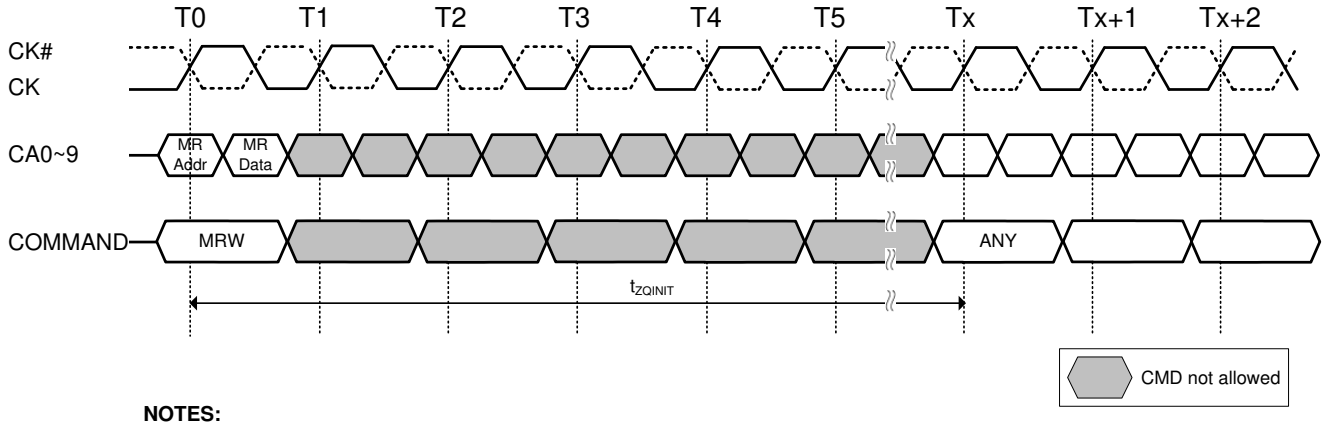
5. The Mode Register Command period is tMRR. No command (other than Nop) is allowed during this period

Figure 39. Mode Register Write timing (RL = 3, tMRW = 5)



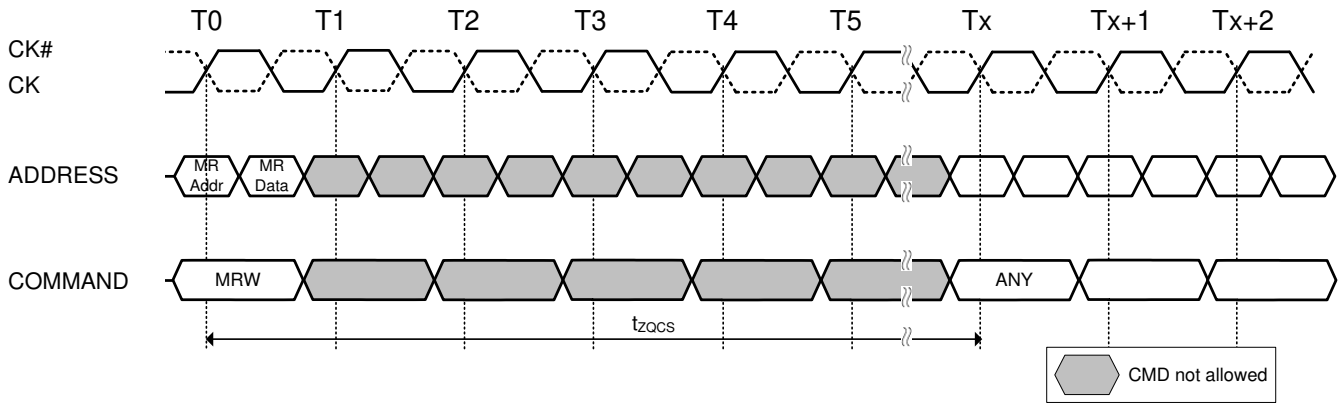
NOTES:
1. The Mode Register Write Command period is tMRW. No command (other than Nop) is allowed during this period.
2. At time Ty, the device is in the idle state.

Figure 40. ZQ Calibration Initialization timing



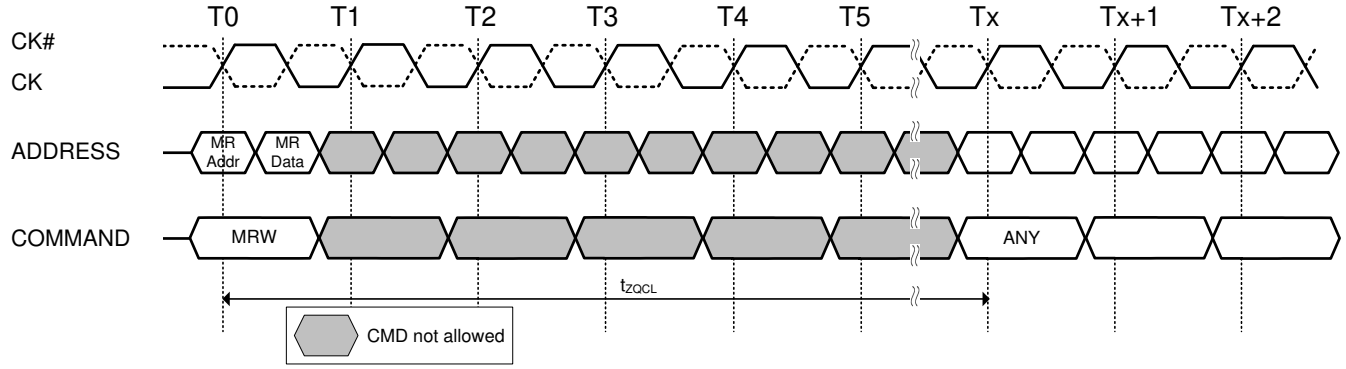
NOTES:
1. The ZQ Calibration Initialization period is tZQINIT. No command (other than Nop) is allowed during this period.
2. CKE must be continuously registered HIGH during the calibration period.
3. All devices connected to the DQ bus should be high impedance during the calibration process.

Figure 41. ZQ Calibration short timing



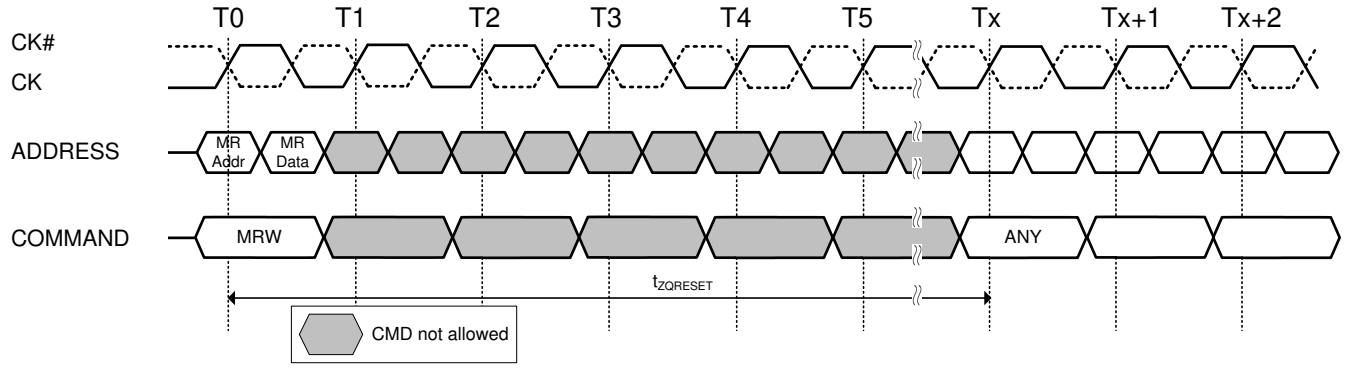
NOTES:
1. The ZQ Calibration Short period is tZQCS. No command (other than Nop) is allowed during this period.
2. CKE must be continuously registered HIGH during the calibration period.
3. All devices connected to the DQ bus should be high impedance during the calibration process.

Figure 42. ZQ Calibration Long timing



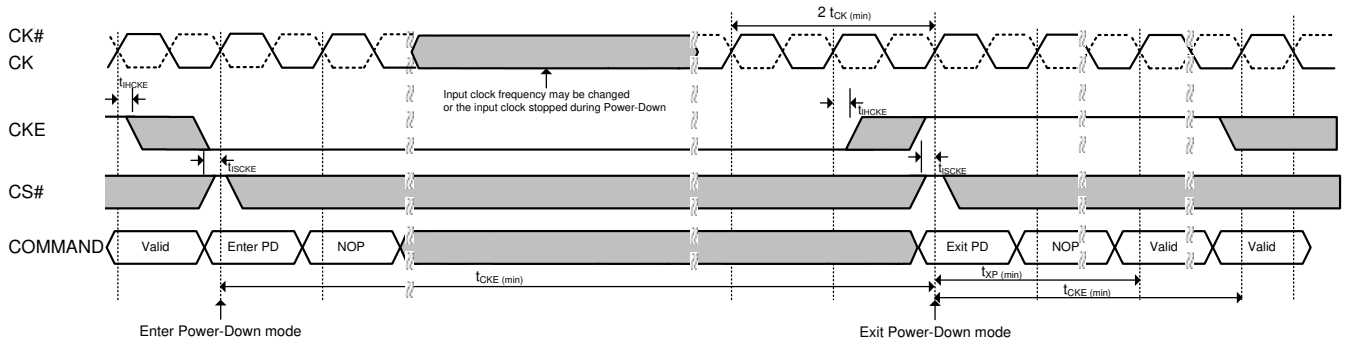
NOTES:
1. The ZQ Calibration Long period is tZQCL. No command (other than Nop) is allowed during this period.
2. CKE must be continuously registered HIGH during the calibration period.
3. All devices connected to the DQ bus should be high impedance during the calibration process.

Figure 43. ZQ Calibration Reset timing



NOTES:
1. The ZQ Calibration Reset period is tZQRESET. No command (other than Nop) is allowed during this period.
2. CKE must be continuously registered HIGH during the calibration period.
3. All devices connected to the DQ bus should be high impedance during the calibration process.

Figure 44. Basic power down entry and exit timing diagram



NOTES:
1. Input clock frequency may be changed or the input clock stopped during power-down, provided that upon exiting power-down, the clock is stable and within specified limits for a minimum of 2 clock cycles prior to power-down exit and the clock frequency is between the minimum and maximum frequency for the particular speed grade.

Figure 45. Example of CKE intensive environment

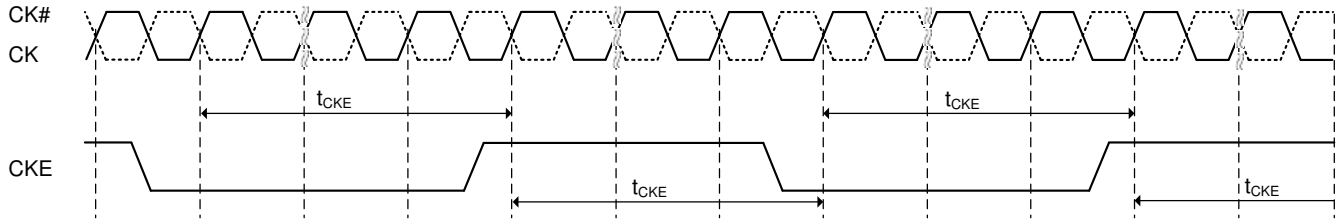
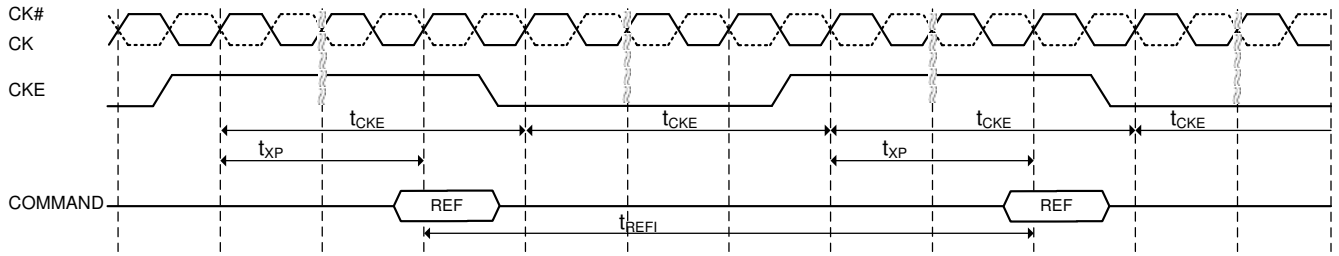
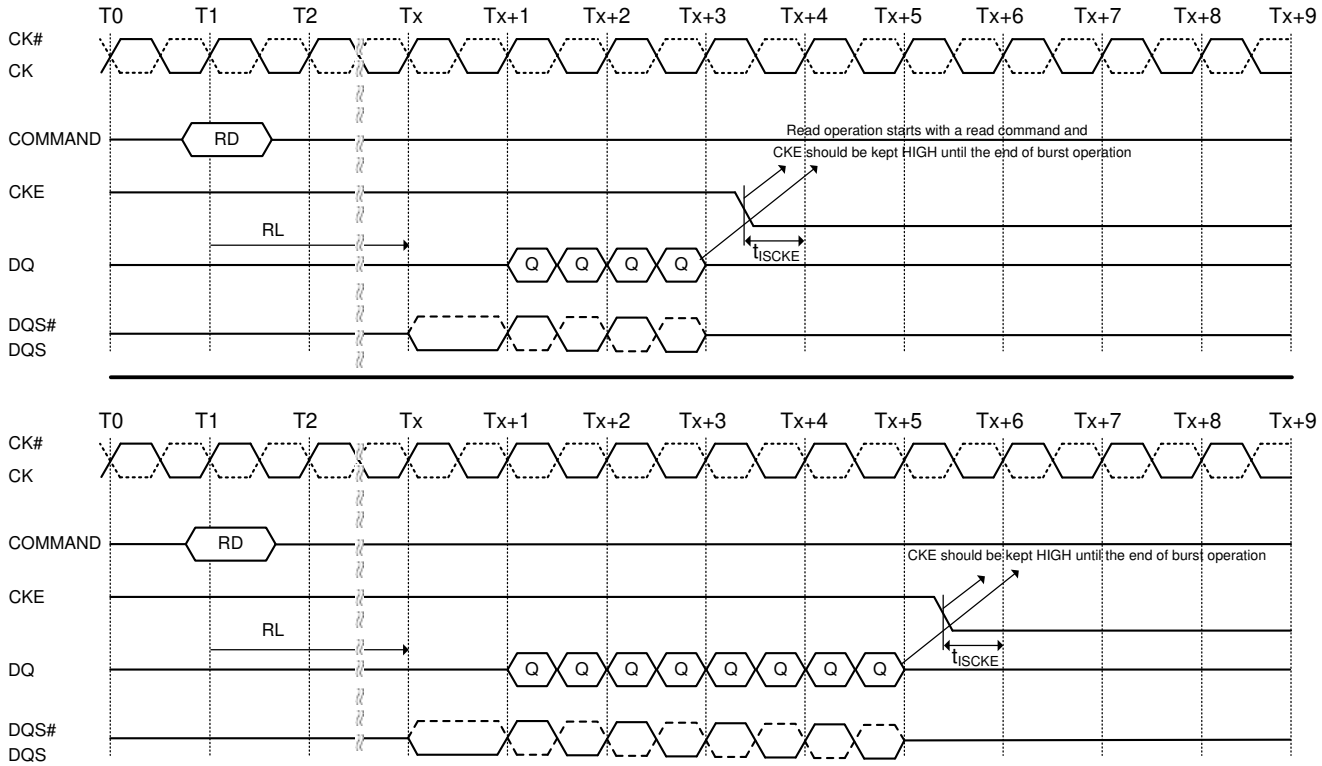


Figure 46. REF to REF timing with CKE intensive environment



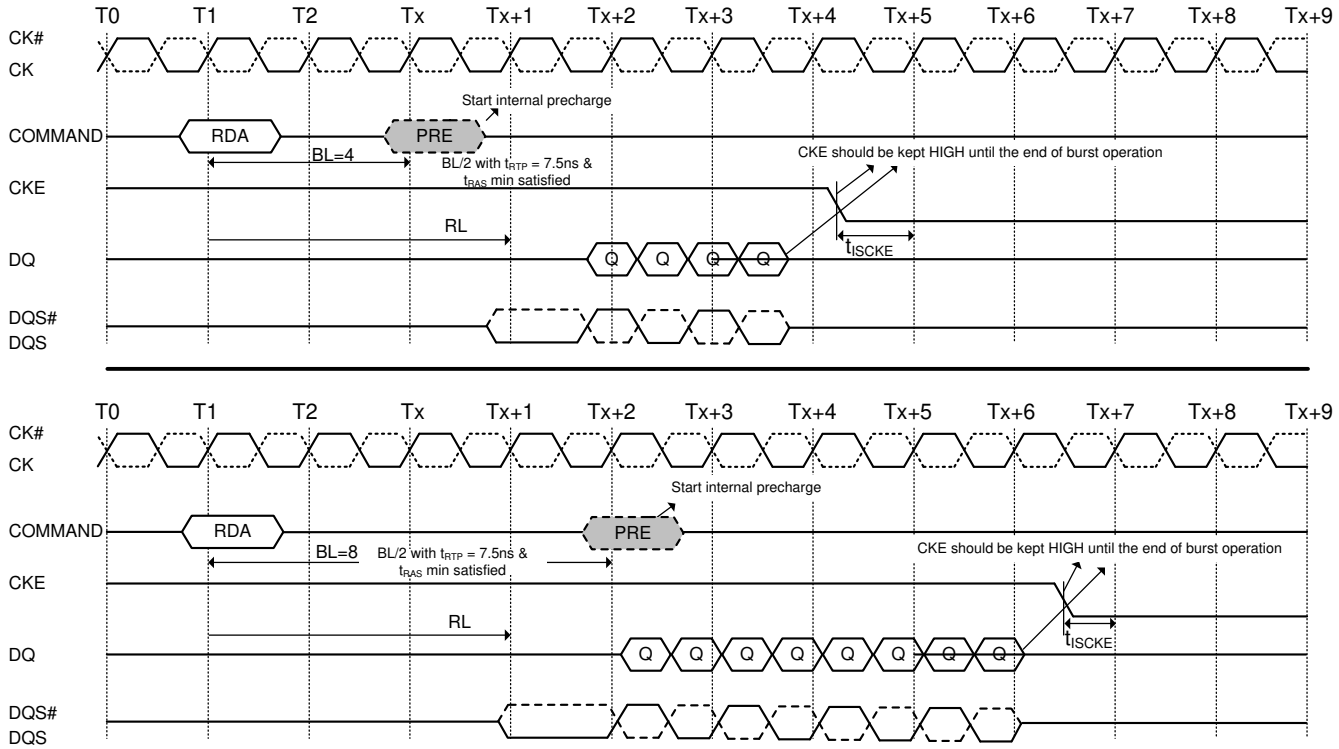
NOTE: The pattern shown above can repeat over a long period of time. With this pattern, DRAM guarantees all AC and DC timing & voltage specifications and DLL operation with temperature and voltage drift

Figure 47. Read to power-down entry



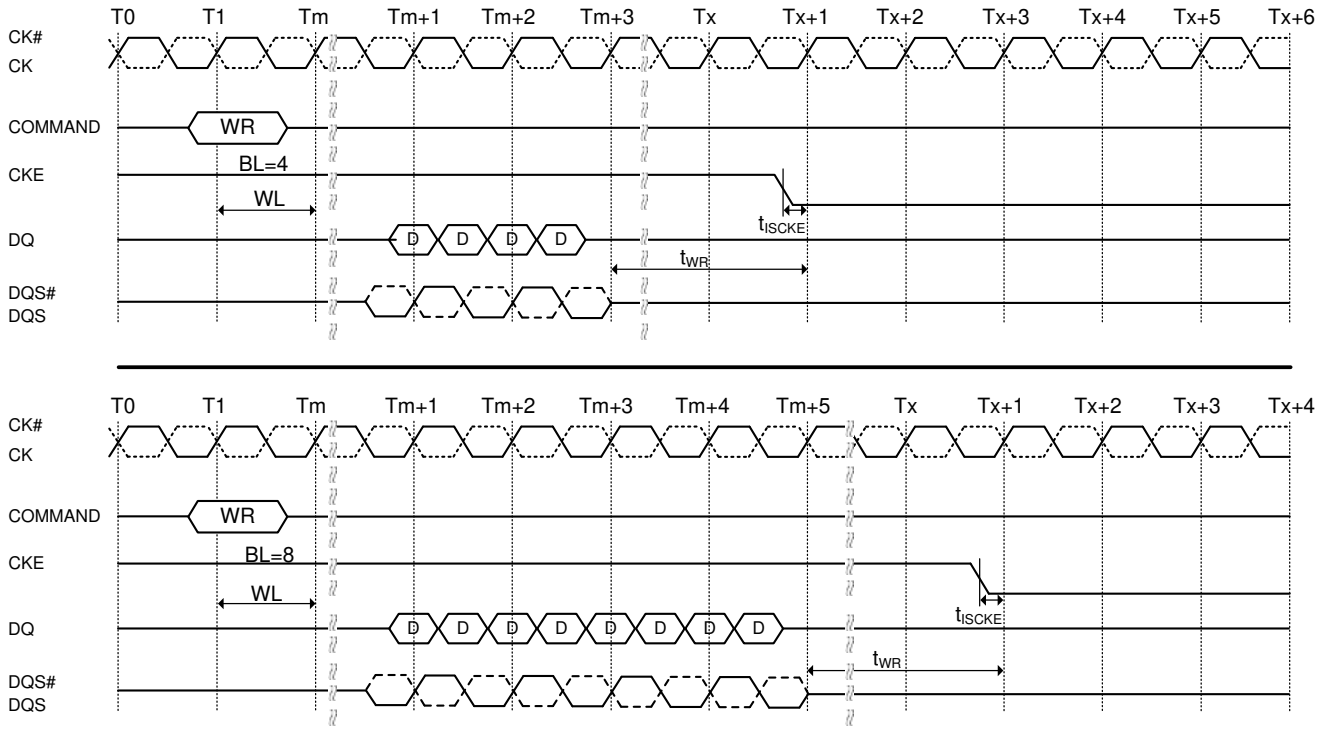
NOTES:
1. CKE may be registered LOW RL + RU(tDQSCK(MAX)/tCK) + BL/2 + 1 clock cycles after the clock on which the Read command is registered.

Figure 48. Read with autoprecharge to power-down entry



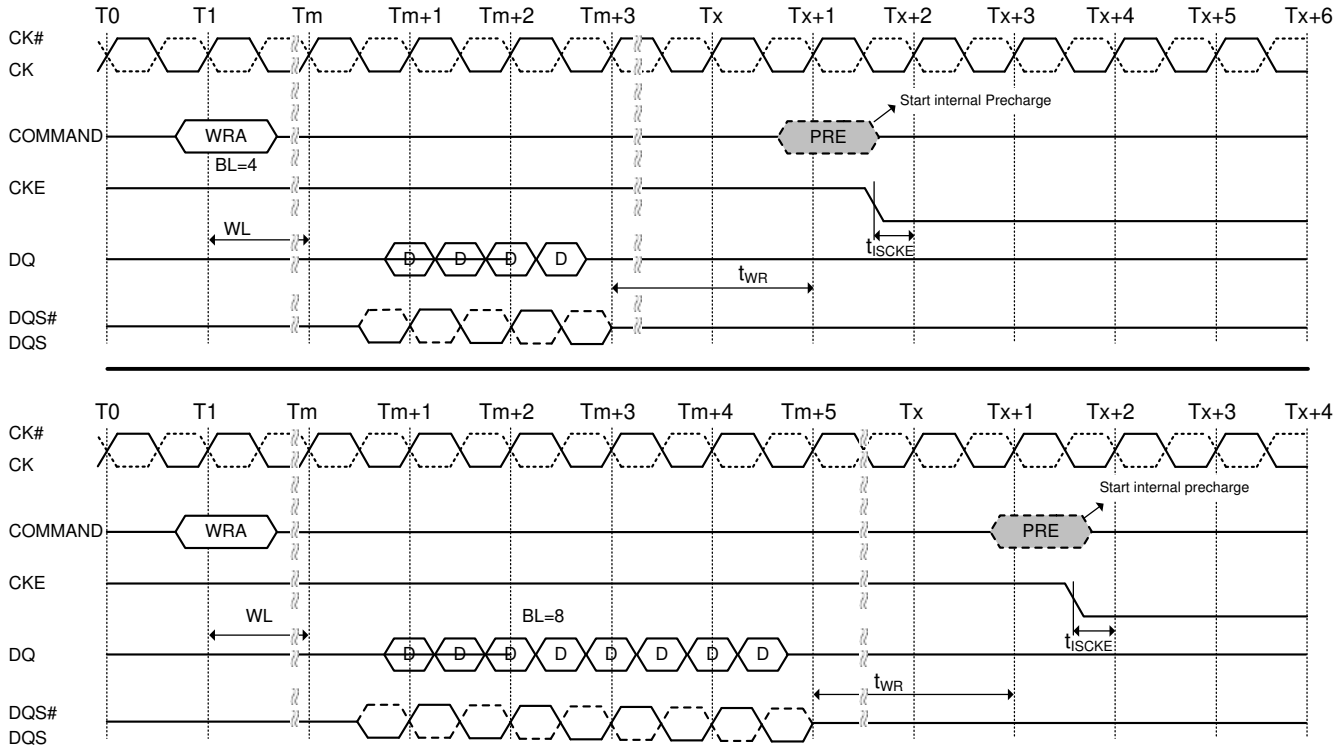
NOTES:
1. CKE may be registered LOW RL + RU(tDQSCK(MAX)/tCK)+ BL/2 + 1 clock cycles after the clock on which the Read command is registered.

Figure 49. Write to power-down entry



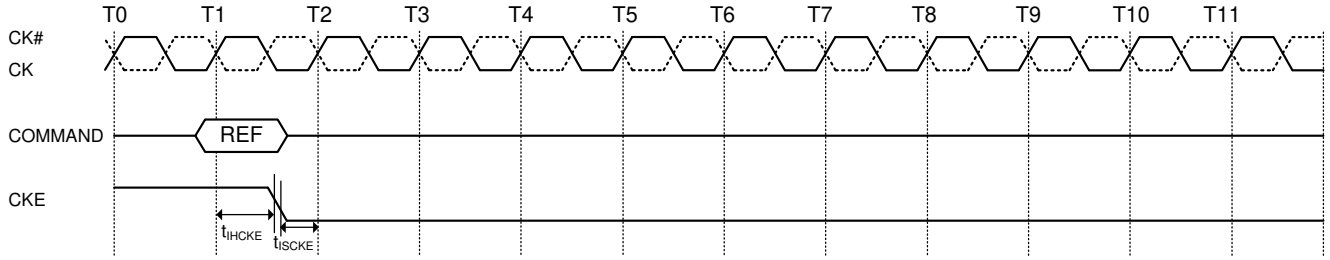
NOTES:
1. CKE may be registered LOW WL + 1 + BL/2 + RU(tWR/tCK) clock cycles after the clock on which the Write command is registered.

Figure 50. Write with autoprecharge to power-down entry



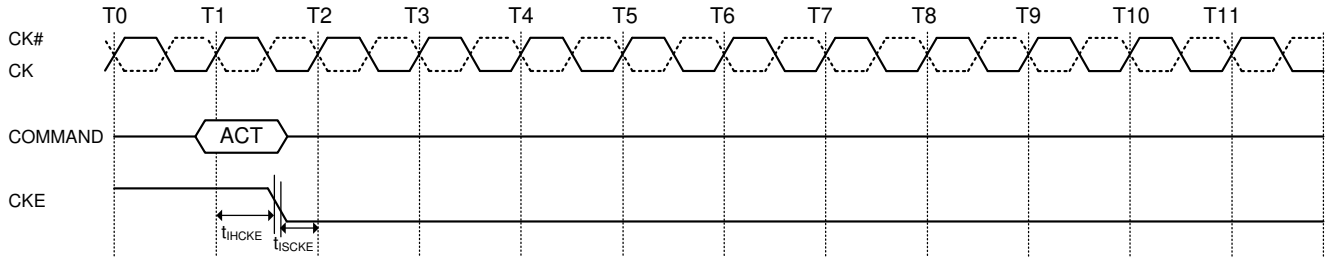
NOTES:
1. CKE may be registered LOW RL + RU(tDQSCK(MAX)/tCK)+ BL/2 + 1 clock cycles after the clock on which the Read command is registered.

Figure 51. Refresh command to power-down entry



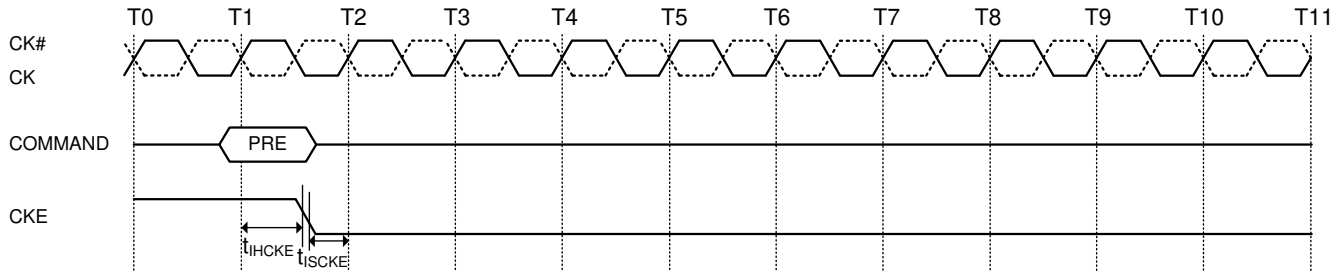
NOTES:
1. CKE may go LOW tIHCKE after the clock on which the Activate command is registered.

Figure 52. Activate command to power-down entry



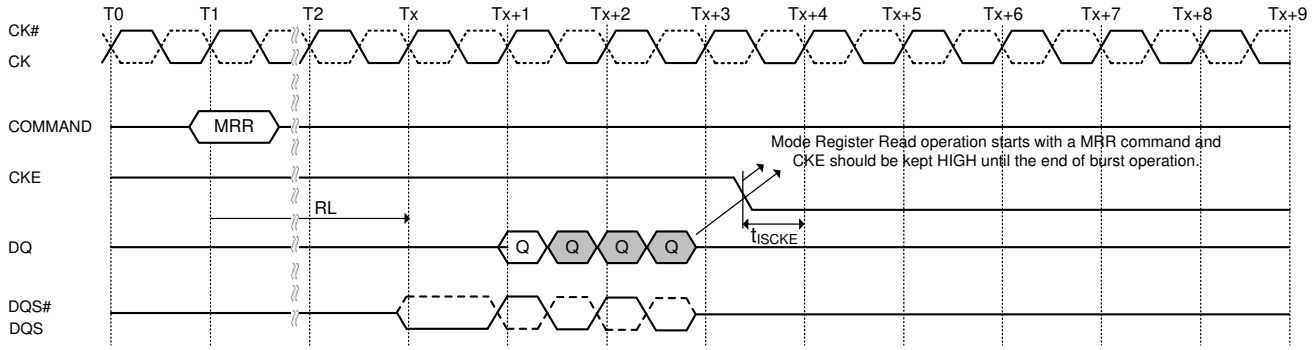
NOTES:
1. CKE may go LOW tIHCKE after the clock on which the Activate command is registered.

Figure 53. Preactive Precharge-all command to power-down entry



NOTES:
1. CKE may go LOW tIHCKE after the clock on which the Preactive/Precharge/Precharge-All command is registered.

Figure 54. Mode Register Read to power-down entry



NOTES:
1. CKE may be registered LOW RL + RU(tDQSCK(MAX)/tCK) + 4/2 + 1 clock cycles after the clock on which the Mode Register Read command is registered.

Figure 55. MRW command to power-down entry

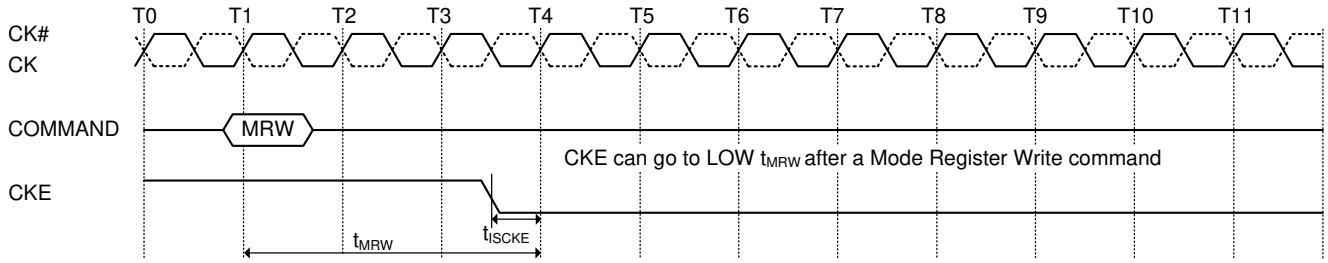
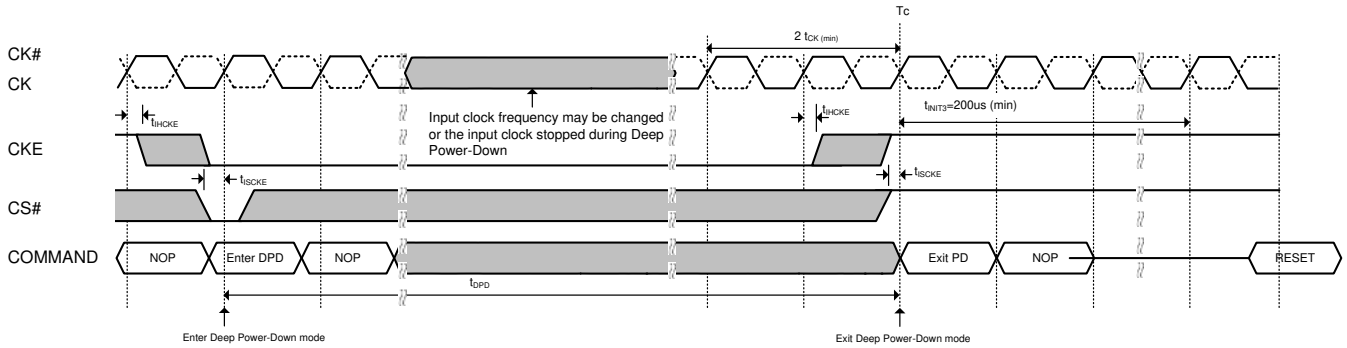
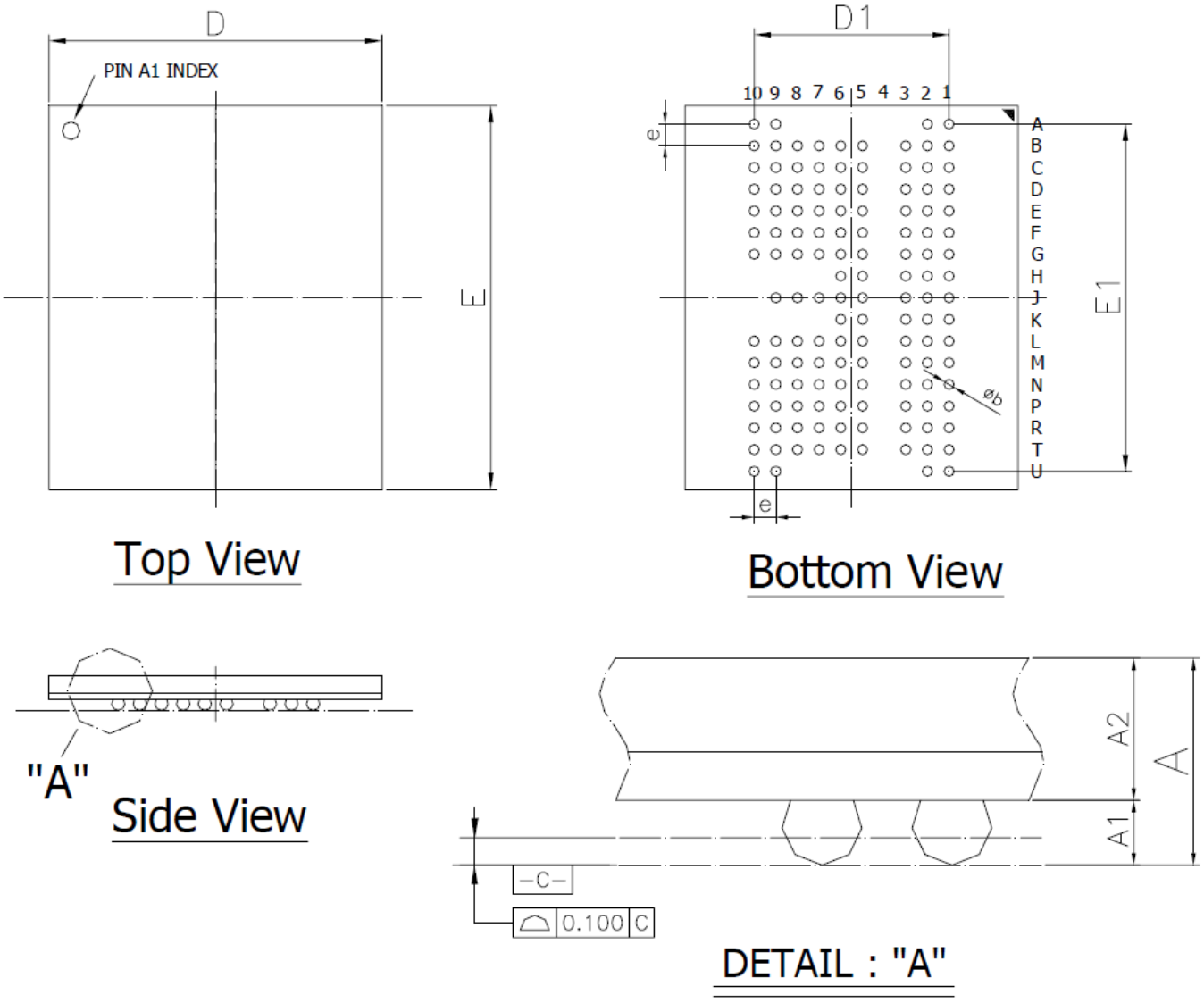


Figure 56. Deep power down entry and exit timing diagram



NOTES:
1. Initialization sequence may start at any time after Tc.
2. tINIT3, and Tc refer to timings in the LPDDR2 initialization sequence. For more detail, see "Power-up, Initialization, and Power-Off".
3. Input clock frequency may be changed or the input clock stopped during deep power-down, provided that upon exiting deep power-down, the clock is stable and within specified limits for a minimum of 2 clock cycles prior to deep power-down exit and the clock frequency is between the minimum and maximum frequency for the particular speed grade.

Figure 57. 134-Ball FBGA Package 10 x 11.5 x 1.0mm(max) Outline Drawing Information



Symbol	Dimension in inch			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	--	--	0.040	--	--	1.02
A1	0.010	0.012	0.014	0.25	0.30	0.35
A2	0.023	--	0.026	0.585	--	0.67
D	0.390	0.394	0.398	9.90	10.00	10.10
E	0.449	0.453	0.457	11.40	11.50	11.60
D1	--	0.230	--	--	5.85	--
E1	--	0.409	--	--	10.40	--
e	--	0.026	--	--	0.65	--
b	0.012	0.014	0.016	0.30	0.35	0.40