

MBM27C1001P-17/-20/-25

CMOS 1M-BIT OTPROM

CMOS 1,048,576-BIT UV ONE TIME ELECTRICALLY PROGRAMMABLE READ ONLY MEMORY

The Fujitsu MBM27C1001P is a high speed 1,048,576 bits CMOS one time electrically programmable read only memory (OTPROM). It is especially well suited for application where rapid turn-around and/or bit pattern experimentation, and low-power consumption are important.

The MBM27C1001P is fabricated using CMOS double polysilicon gate technology with single transistor stacked gate cells and housed in standard 32-pin plastic DIP package and 32-pin plastic SOP package, 32-pin plastic bend-type(Gull-Wing) TSOP package and 32-pin plastic J-Lead LCC package.

It is organized as 131,072 words by 8 bits for use in microprocessor applications. Single +5V operation greatly facilitates its use in systems.

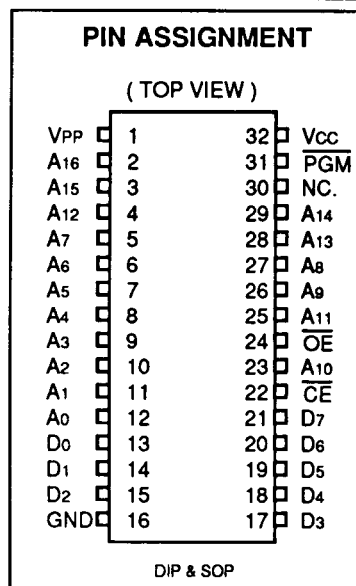
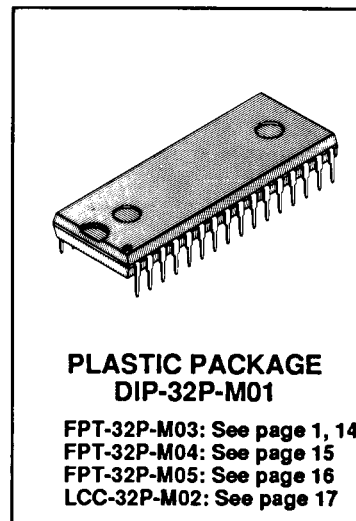
The MBM27C1001P has the same functions including write operations as MBM27C1001(EPROM) except for erase.

- Single 5V($\pm 10\%$) power supply with low current drain:
 - Active operation = 30mA(Max.) for 200ns/250ns
40mA(Max.) for 170ns
 - Standby operation = 0.1mA(Max.)
- 131,072 words x 8 bits organization with on-chip decoding
- Single-byte or Four-byte programming capability with Quick Programming Algorithm
- Static operation (no clocks required)
- Fast access time:
 - 170ns max. (MBM27C1001P-17)
 - 200ns max. (MBM27C1001P-20)
 - 250ns max. (MBM27C1001P-25)
- Three-state output for wired-OR capability
- Programming voltage: +12.5V
- Standard 32-pin plastic DIP (Suffix: P)
- Standard 32-pin plastic SOP (Suffix: PF)
- Standard 32-pin plastic bend-type(Gull-Wing) TSOP (Suffix: PFT)
- Standard 32-pin plastic J-Lead LCC (Suffix: PD)

ABSOLUTE MAXIMUM RATINGS (see NOTE)

Rating	Symbol	Value	Unit
Temperature under Bias	TBIAS	-25 to +85	°C
Storage Temperature Range	TSTG	-45 to +125	°C
All Inputs/Outputs Voltage with respect to GND	V _{IN} , V _{OUT}	-0.6 to V _{CC} + 0.3	V
Voltage on A ₉ with respect to GND	V _{A9}	-0.6 to +13.5	V
Programming Voltage with respect to GND	V _{PP}	-0.6 to +14.0	V
Supply Voltage with respect to GND	V _{CC}	-0.6 to +7.0	V

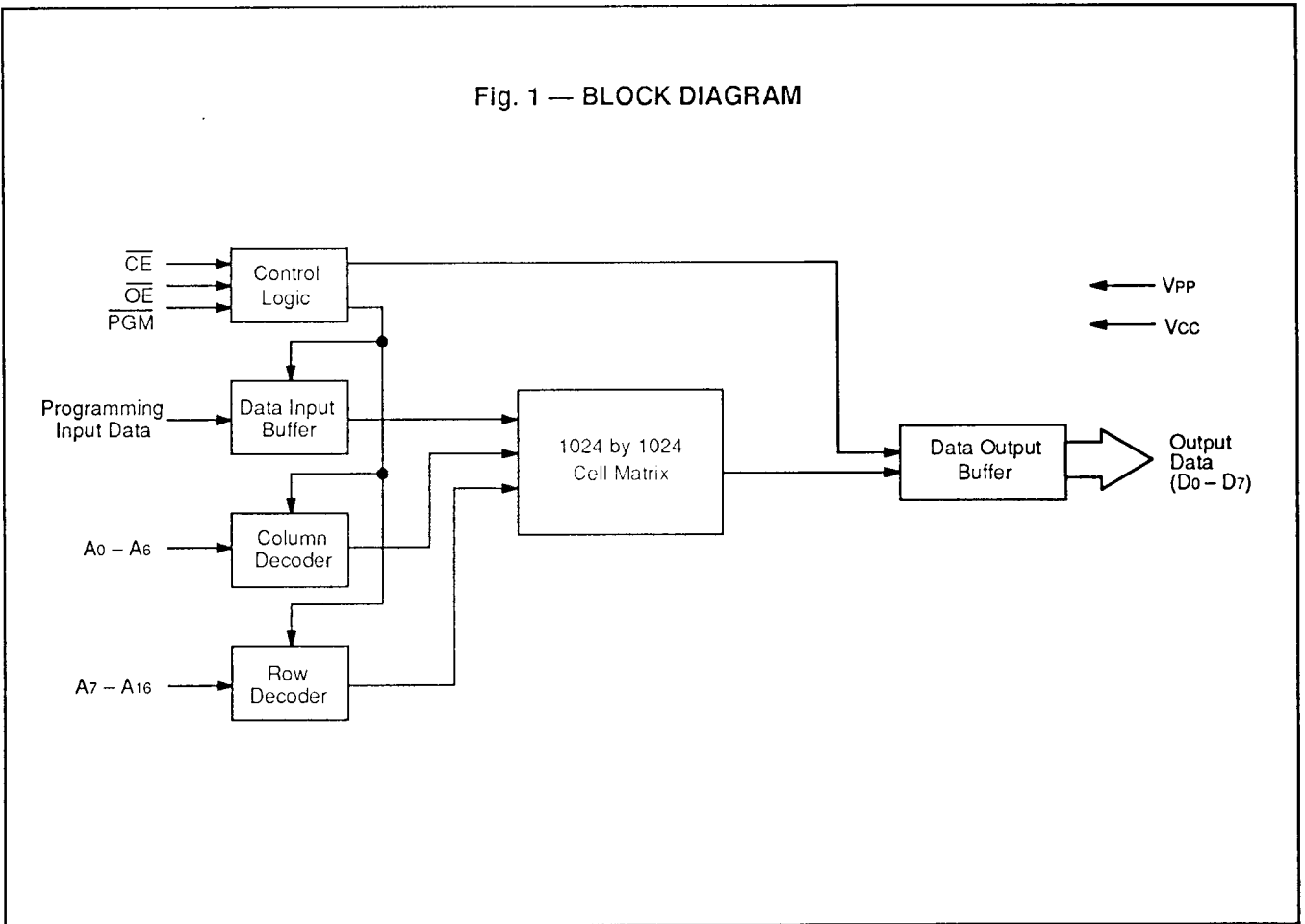
NOTE: Permanent device damage may occur if the above Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

MBM27C1001P-17
 MBM27C1001P-20
 MBM27C1001P-25

Fig. 1 — BLOCK DIAGRAM



CAPACITANCE ($T_A = 25^\circ\text{C}$, $f = 1\text{MHz}$)

Parameter	Symbol	Values			Unit
		Min	Typ	Max	
Input Capacitance ($V_{IN}=0V$)	C_{IN}		8	12	pF
Output Capacitance ($V_{OUT}=0V$)	C_{OUT}		8	12	pF

PIN DESCRIPTION

Symbol	Pin No.	Function
V _{PP}	1	+12.5V programming voltage
$\overline{\text{OE}}$	24	Output enable. When $\overline{\text{OE}}$ and $\overline{\text{CE}}$ are active Low and the $\overline{\text{PGM}}$ strobe is active High; all output lines(D ₀ –D ₇) are enabled.
A ₀ –A ₁₆	2–12, 23 25–29	Address lines
D ₀ –D ₇	13–15, 17–21	Three-state output data line
GND	16	Circuit ground
$\overline{\text{CE}}$	22	When active Low, the device is enabled for data read.
NC.	30	No connection
$\overline{\text{PGM}}$	31	When active Low, programming data from the input buffer is written into a specified address of memory.
V _{cc}	32	+5V power supply

FUNCTIONS AND PIN CONNECTIONS

1. Read Mode

Mode \ Symbol	A ₀ –A ₁₆	D ₀ –D ₇	$\overline{\text{OE}}$	$\overline{\text{CE}}$	$\overline{\text{PGM}}$	V _{cc}	V _{PP}	GND
	Read	A _{IN}	D _{OUT}	V _{IL}	V _{IL}	V _{IH}	+5V	+5V
Standby	X	Hi-Z	X	V _{IH}	X	+5V	+5V	GND
Output Disable	A _{IN}	Hi-Z	V _{IH}	V _{IL}	X	+5V	+5V	GND
			X	V _{IL}	V _{IL}			

Legend: X=Don't care

FUNCTIONS AND PIN CONNECTIONS(Cont'd)

2. Single-Byte Programming Mode

Mode \ Symbol	A ₀ -A ₁₆	D ₀ -D ₇	$\overline{\text{OE}}$	$\overline{\text{CE}}$	$\overline{\text{PGM}}$	V _{CC}	V _{PP}	GND
Program	A _{IN}	D _{IN}	V _{IH}	V _{IL}	V _{IL}	+6V	+12.5V	GND
Verify	A _{IN}	D _{OUT}	V _{IL}	V _{IL}	V _{IH}	+6V	+12.5V	GND
Program Inhibit	A _{IN}	Hi-Z	V _{IH}	V _{IL}	V _{IH}	+6V	+12.5V	GND

3. Four-Byte Programming Mode

Mode \ Symbol	A ₀ , A ₁	A ₂ to A ₁₆	D ₀ -D ₇	$\overline{\text{OE}}$	$\overline{\text{CE}}$	$\overline{\text{PGM}}$	V _{CC}	V _{PP}	GND
Program	A _{IN}	A _{IN}	D _{IN}	V _{IH}	V _{IH}	V _{IH}	+6V	+12.5V	GND
Program	X	A _{IN}	Hi-Z	V _{IL}	V _{IH}	V _{IL}	+6V	+12.5V	GND
Verify	A _{IN}	A _{IN}	D _{OUT}	V _{IL}	V _{IL}	V _{IH}	+6V	+12.5V	GND
Program Inhibit	A _{IN}	A _{IN}	Hi-Z	V _{IL}	V _{IH}	V _{IH}	+6V	+12.5V	GND

Legend: X=Don't care

RECOMMENDED OPERATING CONDITIONS

(Referenced to GND)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V _{CC}	4.5	5.0	5.5	V
Supply Voltage *1	V _{PP}	V _{CC} -0.6	V _{CC}	V _{CC} +0.6	V
Operating Temperature	T _A	0		70	°C

*1 : V_{PP} supply voltage is applied posterior to or coincident with V_{CC} supply voltage and cut off prior to or coincident with V_{CC} supply voltage.

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Conditions	Values			Unit
			Min	Typ	Max	
Input Leakage Current	$ I_{LI} $	$V_{IN} = V_{CC} = 5.5V$			10	μA
Output Leakage Current	$ I_{LO} $	$V_{OUT} = V_{CC} = 5.5V$			10	μA
Vcc Standby Current	ISB1	$\overline{CE} = V_{IH}$			1.0	mA
Vcc Standby Current	ISB2	$\overline{CE} = V_{CC} \pm 0.3V$		1.0	100	μA
Vcc Active Current	200ns/250ns	Icc1			30	mA
	170ns				40	mA
Vcc Operation Current	200ns/250ns	Icc2	Cycle = min., IOUT = 0mA		30	mA
	170ns				40	mA
VPP Supply Current	IPP	$V_{PP} = V_{CC} \pm 0.6V$		1.0	100	μA
Input High Level	V_{IH}		2.0		$V_{CC} + 0.3$	V
Input Low Level	V_{IL}		-0.1		0.8	V
Output High Level	V_{OH1}	$I_{OH} = -400\mu A$	2.4			V
Output High Level	V_{OH2}	$I_{OH} = -100\mu A$	$V_{CC} - 0.7$			V
Output Low Level	V_{OL}	$I_{OL} = 2.1mA$			0.45	V

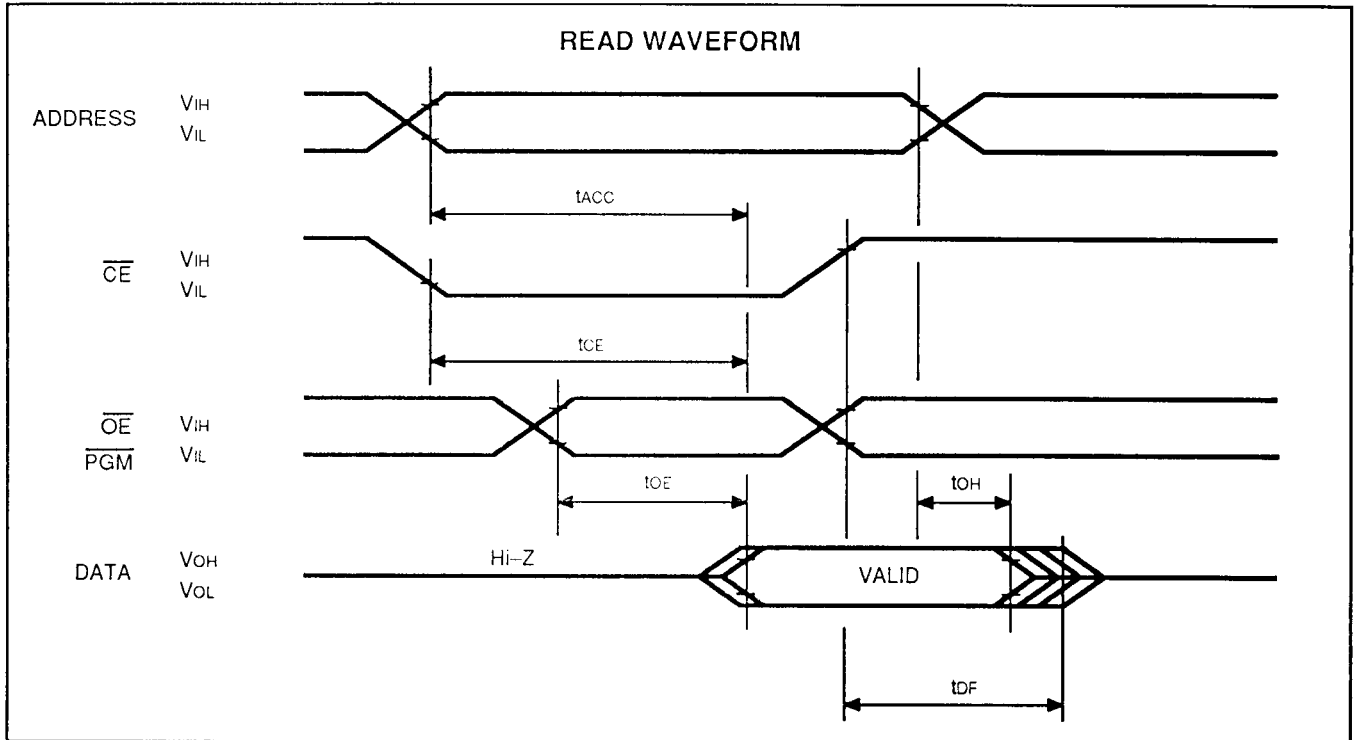
AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter	Conditions	Symbol	MBM27C1001P-17 Values		MBM27C1001P-20 Values		MBM27C1001P-25 Values		Unit
			Min	Max	Min	Max	Min	Max	
Address Access Time	$\overline{CE} = \overline{OE} = V_{IL}$ $\overline{PGM} = V_{IH}$	tACC		170		200		250	ns
\overline{CE} to Output Delay Time	$\overline{OE} = V_{IL}$ $\overline{PGM} = V_{IH}$	tCE		170		200		250	ns
\overline{PGM} , \overline{OE} to Output Delay Time	$\overline{CE} = V_{IL}$	tOE		70		70		100	ns
\overline{PGM} , \overline{OE} to Output Float Delay	$\overline{OE} = \overline{CE} = V_{IL}$ $\overline{PGM} = V_{IH}$	tDF	0	60	0	60	0	60	ns
Address to Output Hold Time	$\overline{CE} = \overline{OE} = V_{IL}$ $\overline{PGM} = V_{IH}$	tOH	0		0		0		ns

AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)



PROGRAMMING INFORMATION

PROGRAMMING

Single-Byte Programming. When +12.5V(±0.3) volts is applied to Vpp, +6(±0.25) volts is applied to Vcc, \overline{CE} and $\overline{PGM}=V_{IH}$ and $\overline{OE}=V_{IH}$, the programming mode is initiated. Next, the proper address is input and the data pattern is applied to the input buffer (Figure 1). When both address and data are stable, a 0.5–millisecond negative pulse is applied to the \overline{PGM} pin. Upon verification of written data an over pulse (three times the initial pulse width times the number of pulses used to accomplish a write) should be applied to complete the programming of one byte. Refer to the PROGRAMMING FLOW-CHART that follows for step–by–step programming procedures.

Four-Byte Programming. When Compared to the Single-byte programming, the four-byte programming method reduces the pro-

gramming time by about 75% one quarter. Voltages applied to Vpp and Vcc are the same as those for Single-byte programming; however, some logic levels differ (refer to "Four Byte Programming" in the truth table). In conjunction with \overline{OE} pin, address pins A0 and A1 are used to latch four bytes of data. When both address and data are stable, a 0.5–millisecond negative pulse is applied to the \overline{PGM} pin. Upon verification of written data an over pulse (three times the initial pulse width times the number of pulses used to accomplish a write) should be applied to complete the programming of four bytes. Refer to the PROGRAMMING FLOWCHART for step–by–step programming procedures.

CAUTION

The width of one programming pulse must not exceed 40–millisecond; thus, a continuous TTL low–level voltage should not be applied to the \overline{PGM} pin. Also, a 0.1–microfarad capacitor must be connected

between VPP and ground to prevent excessive voltage transients. Neglecting either of these precautions may cause device failure.

ELECTRONIC SIGNATURE/PROGRAMMING ALGORITHM

When MBM27C1001P is shipped from the factory, all memory cells (1,048,576 bits) are set to the high state (logic 1). During the programming procedure, affected bit cells are set to the Low(logic 0) state.

The MBM27C1001P is programmed with a fast programming algorithm designed by Fujitsu Quick programming. Manufacturer and device codes are electronically stored in each device; these codes can

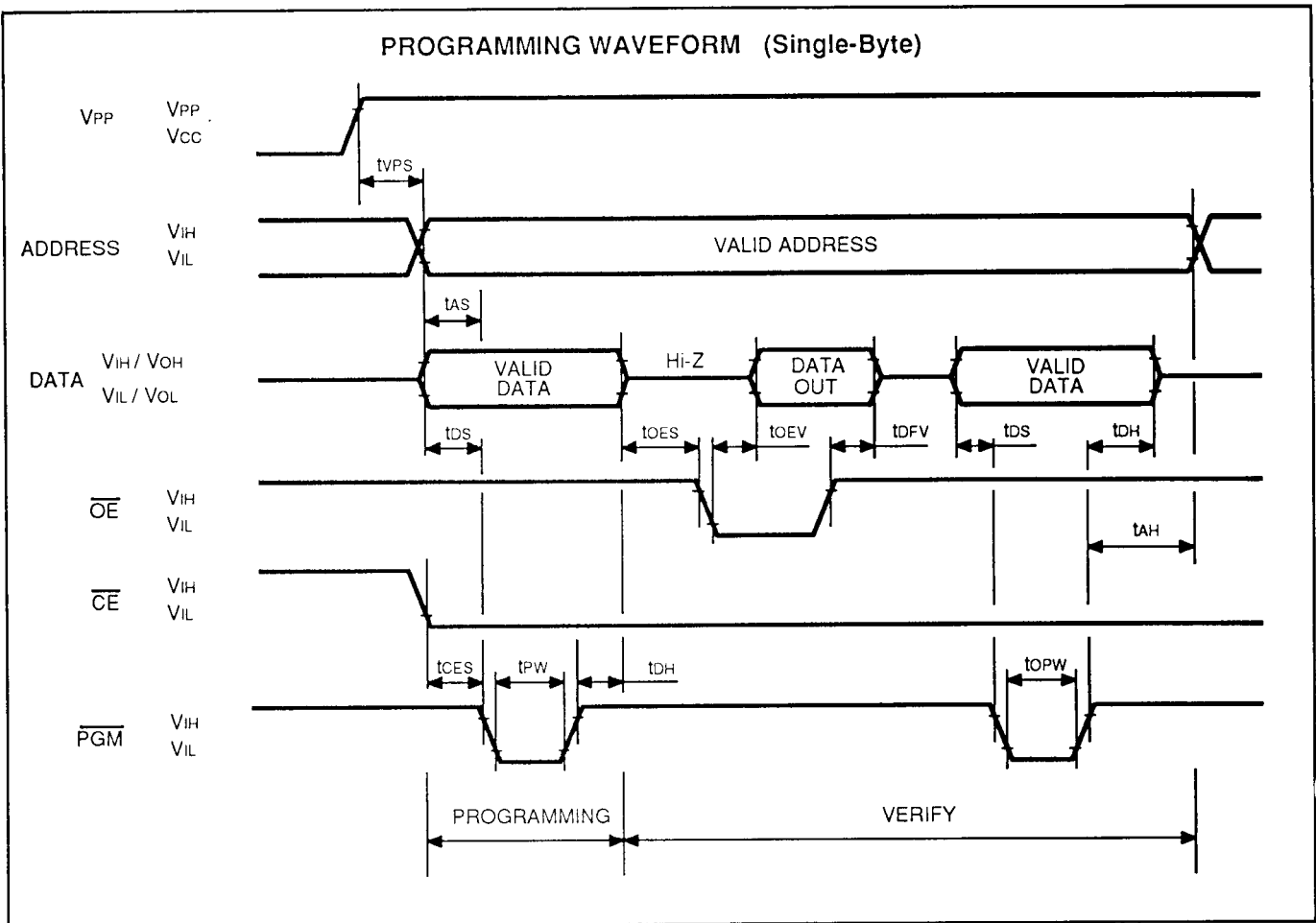
be read at the output port (D0 to D7) for the purpose of matching the device with the Quick programming algorithm. The Electronic Signature Code List is shown in the table preceding the ELECTRICAL CHARACTERISTICS.

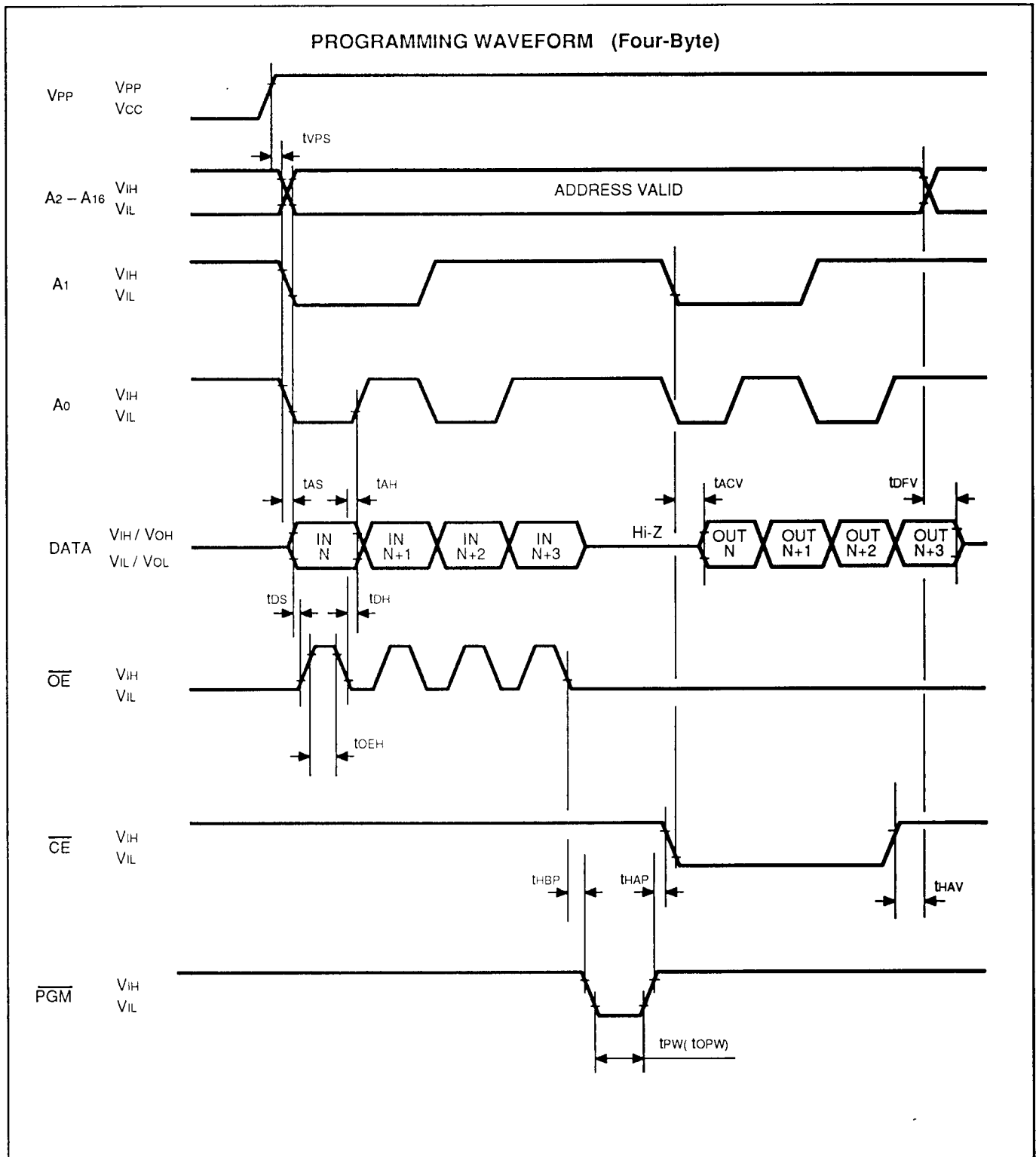
ELECTRONIC SIGNATURE CODE LIST

Definition	Vcc	VPP	A0 to A6	A7 to A16	\overline{OE}	\overline{CE}	\overline{PGM}	D0	D1	D2	D3	D4	D5	D6	D7	HEX
Manufacture	Vcc	Vcc	#0000	Don't Care	V _{IL}	V _{IL}	V _{IH}	0	0	1	0	0	0	0	0	#04
Device	Vcc	Vcc	#0001	Don't Care	V _{IL}	V _{IL}	V _{IH}	1	0	1	0	0	1	1	1	#E5

NOTE: A9=12V±0.5V

MBM27C1001P-17
MBM27C1001P-20
MBM27C1001P-25





PROGRAMMING INFORMATION (Cont'd)

DC CHARACTERISTICS

($T_A = 25\text{ }^\circ\text{C} \pm 5\text{ }^\circ\text{C}$, $V_{CC} = 6\text{V} \pm 0.25\text{V}$, $V_{PP} = 12.5\text{V} \pm 0.3\text{V}$)^{*1}
^{*2}

Parameter	Symbol	Conditions	Values			Unit
			Min	Typ	Max	
Input Leakage Current	$ I_{Li} $	$V_{iN} = 6.25\text{V}/0\text{V}$			10	μA
VPP Supply Current (Single-Byte)	I_{PP1}	$\overline{CE} = V_{iL}, \overline{OE} = V_{iH}, \overline{PGM} = V_{iL}$			30	mA
VPP Supply Current (Four-Byte)	I_{PP2}	$\overline{CE} = V_{iH}, \overline{OE} = V_{iL}, \overline{PGM} = V_{iL}$			100	mA
VPP Supply Current	I_{PP3}	$\overline{PGM} = V_{iH}$			5	mA
VCC Supply Current	I_{CC}				30	mA
Input Low Level	V_{iL}		-0.1		0.6	V
Input High Level	V_{iH}		2.4		$V_{CC} + 0.3$	V
Output Low Level	V_{oL}	$I_{oL} = 2.1\text{mA}$			0.45	V
Output High Level	V_{oH}	$I_{oH} = -400\mu\text{A}$	2.4			V

NOTE : *1 VCC must be applied either coincidentally or before VPP and removed either coincidentally or after VPP.

*2 VPP must not be 13.5volts or more including overshoot. Permanent device damage may occur if the device is taken out or put into socket remaining VPP=12.5volts.

AC CHARACTERISTICS

1. Single-Byte Programming Mode

Parameter	Symbol	Values			Unit
		Min	Typ	Max	
Address Setup Time	tAS	2			μs
Data Setup Time	tDS	2			μs
\overline{CE} Setup Time	tCES	2			μs
Programming Pulse Width	tpw	0.475	0.5	0.525	ms
Over Programming Pulse Width (Note)	topw	1.4		39.4	ms
Over Programming Pulse Number	N	1		25	times
Data Hold Time	tDH	2			μs
\overline{OE} Setup time	toES	2			μs
\overline{OE} to Output Valid	toEV			500	ns
\overline{OE} to Output Float	tDFV			150	ns
Address Hold Time	tAH	0			μs
VPP Setup Time	tvPS	2			μs

Note: $t_{OPW} = 1.5 \times N \text{ms} \pm 5\%$

AC CHARACTERISTICS(Cont'd)

2. Four-Byte Programming Mode

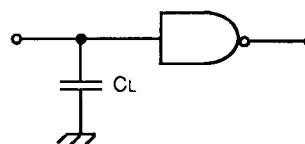
Parameter	Symbol	Values			Unit
		Min	Typ	Max	
Address Setup Time	tAS	2			μs
Address Hold Time	tAH	2			μs
Data Setup Time	tDS	2			μs
Data Hold Time	tDH	2			μs
\overline{OE} High Hold Time	tOEHigh	2			μs
Hold Time Before Programming	tHBP	2			μs
Programming Pulse Width	tPW	0.475	0.5	0.525	ms
Over Programming Pulse Width (Note)	tOPW	1.4		39.4	ms
Over Programming Pulse Number	N	1		25	times
Hold Time After Program	tHAP	2			μs
Address Access Time at Verify	tACV			500	ns
\overline{OE} to Output Float	tDFV			150	ns
Hold Time After Verify	tHAV	0			μs
VPP Setup Time	tVPS	2			μs

Note: tOPW=1.5 x Nms±5%

AC TEST CONDITIONS

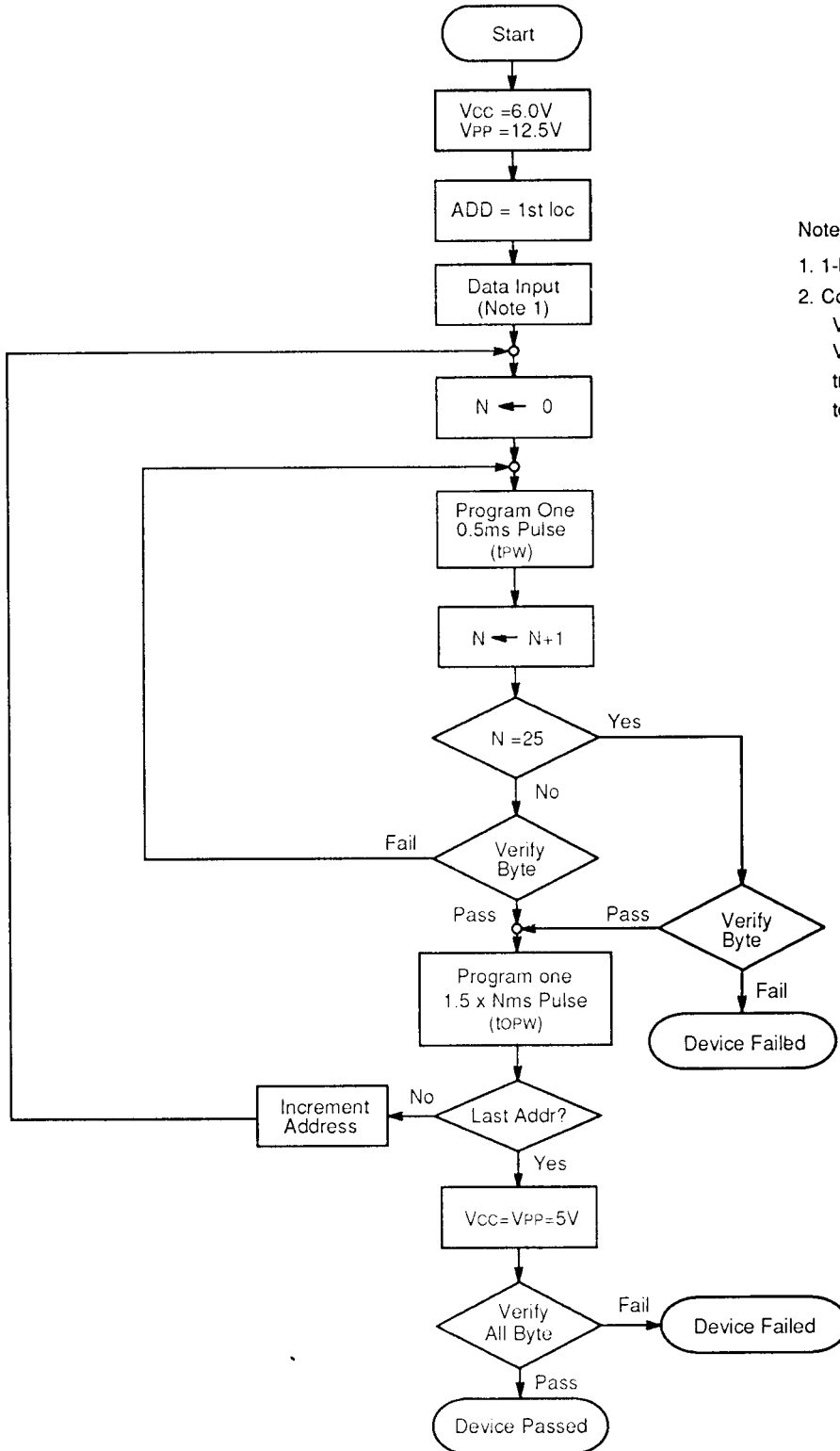
Fig. 2 — AC TEST CONDITIONS

Input pulse levels: 0.45V to 2.4V (Programming: 0.3V to 2.8V)
 Input Rise/Fall Times: $\leq 20ns$
 Input Reference Levels: 0.8V to 2.0V (Programming: 0.6V to 2.4V)
 Output Reference Levels: 0.8V to 2.0V
 Output Load: 1 TTL gate and $C_L = 100pF$



PROGRAMMING INFORMATION

QUICK PROGRAMMING FLOWCHART



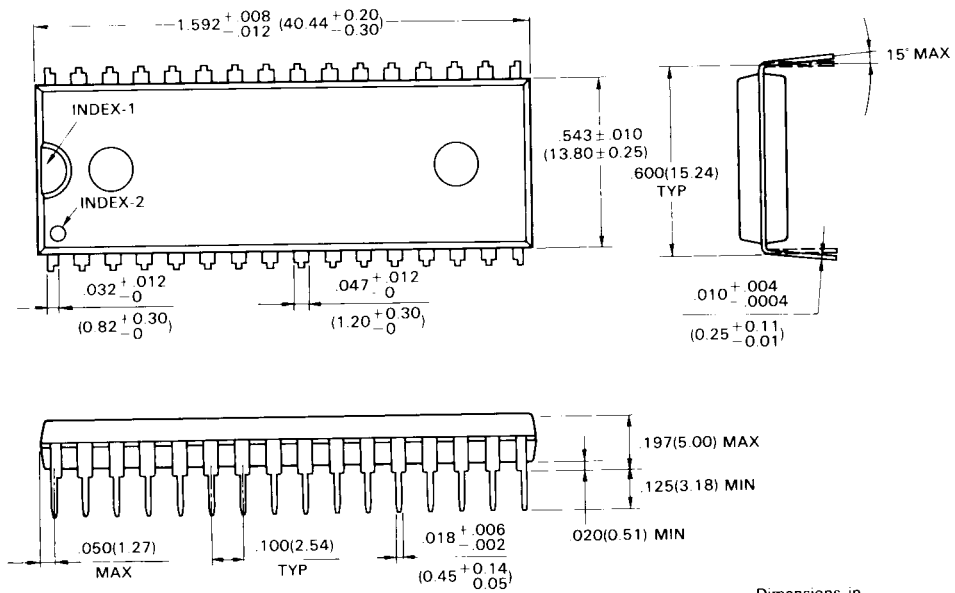
Note 1 :

1. 1-byte or 4-byte:
2. Conditions:
 $V_{cc} = 6V(\pm 0.25)V$
 $V_{pp} = 12.5V(\pm 0.3)V$
 $t_{pw} = 0.5ms \pm 25\mu s$
 $t_{OPW} = 1.5 \times Nms(\pm 5\%)$

PACKAGE DIMENSIONS (Cont'd)

(Suffix: P)

32-LEAD PLASTIC DUAL IN-LINE PACKAGE
 (CASE No.: DIP-32P-M01)



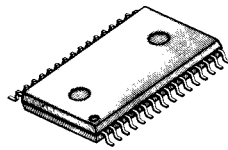
© 1988 FUJITSU LIMITED D32007S-1C

Dimensions in
 inches (millimeters)

MBM27C1001P-17
 MBM27C1001P-20
 MBM27C1001P-25

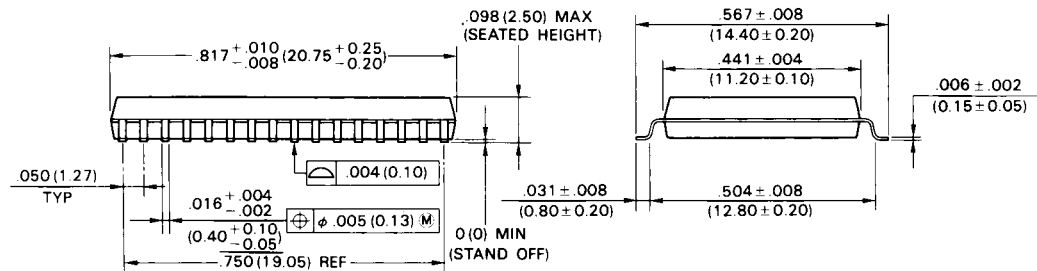
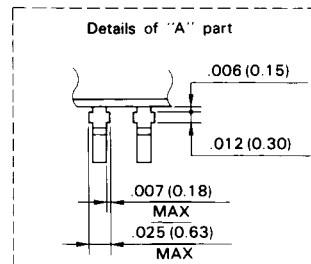
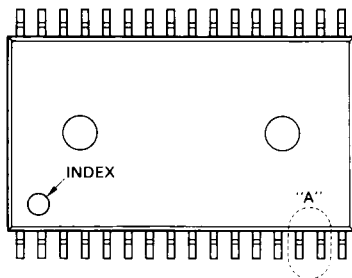
PACKAGE DIMENSIONS (Cont'd)

(Suffix: PF)



FPT-32P-M03

32-LEAD PLASTIC FLAT PACKAGE (CASE No.: FPT-32P-M03)

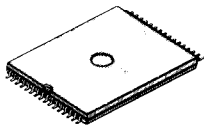


© 1990 FUJITSU LIMITED F32008S-3C

Dimensions in
 inches (millimeters)

PACKAGE DIMENSIONS (Cont'd)

(Suffix: PFTN)



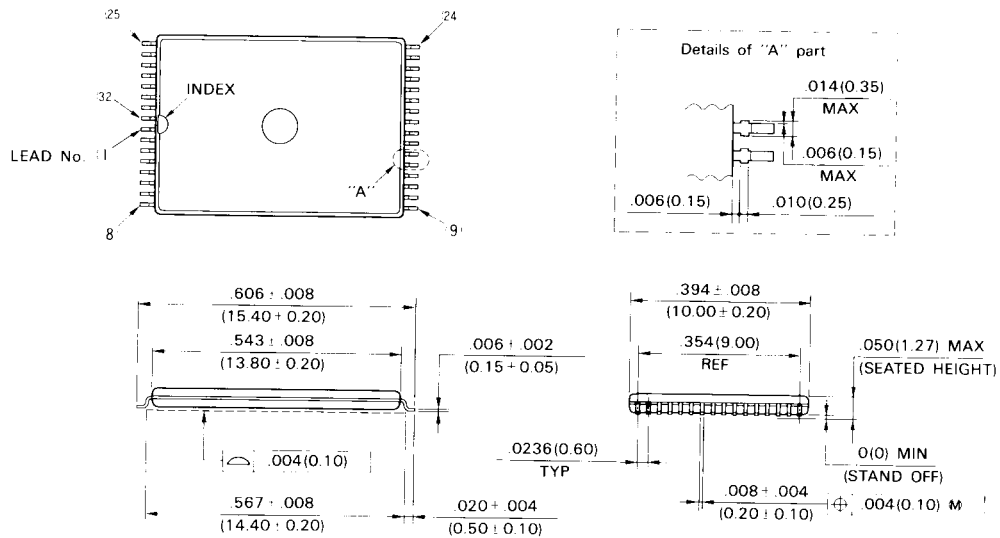
**PLASTIC PACKAGE
FPT-32P-M04**

**PIN ASSIGNMENT
(Normal Bend)**

(Top View)

A11		25		24		\overline{OE}
A9		26		23		A10
A8		27		22		\overline{CE}
A13		28		21		D7
A14		29		20		D6
NC.		30		19		D5
PGM		31		18		D4
VCC		32		17		D3
VPP		1		16		GND
A16		2		15		D2
A15		3		14		D1
A12		4		13		D0
A7		5		12		A0
A6		6		11		A1
A5		7		10		A2
A4		8		9		A3

32-LEAD PLASTIC FLAT PACKAGE (CASE No.: FPT-32P-M04)



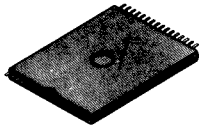
© 1990 FUJITSU LIMITED F32005S-3C

Dimensions in
inches (millimeters)

MBM27C1001P-17
 MBM27C1001P-20
 MBM27C1001P-25

PACKAGE DIMENSIONS (Cont'd)

(Suffix: PFTR)



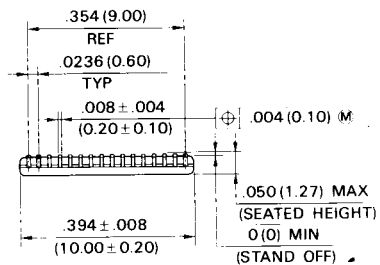
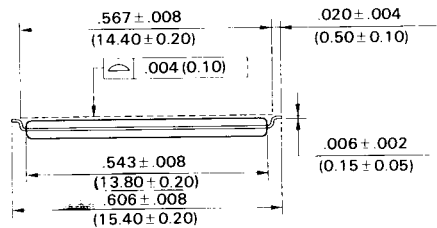
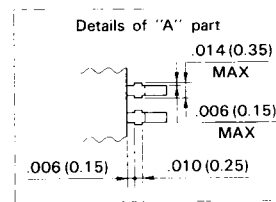
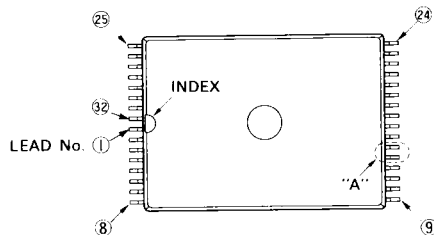
**PLASTIC PACKAGE
FPT-32P-M05**

**PIN ASSIGNMENT
(Reversed Bend)**

(Bottom View)

A4	□	8		9	□	A3
A5	□	7		10	□	A2
A6	□	6		11	□	A1
A7	□	5		12	□	A0
A12	□	4		13	□	D0
A15	□	3		14	□	D1
A16	□	2		15	□	D2
VPP	□	1	○	16	□	GND
VCC	□	32		17	□	D3
PGM	□	31		18	□	D4
NC.	□	30		19	□	D5
A14	□	29		20	□	D6
A13	□	28		21	□	D7
A8	□	27		22	□	CE
A9	□	26		23	□	A10
A11	□	25		24	□	OE

32-LEAD PLASTIC FLAT PACKAGE (CASE No.: FPT-32P-M05)

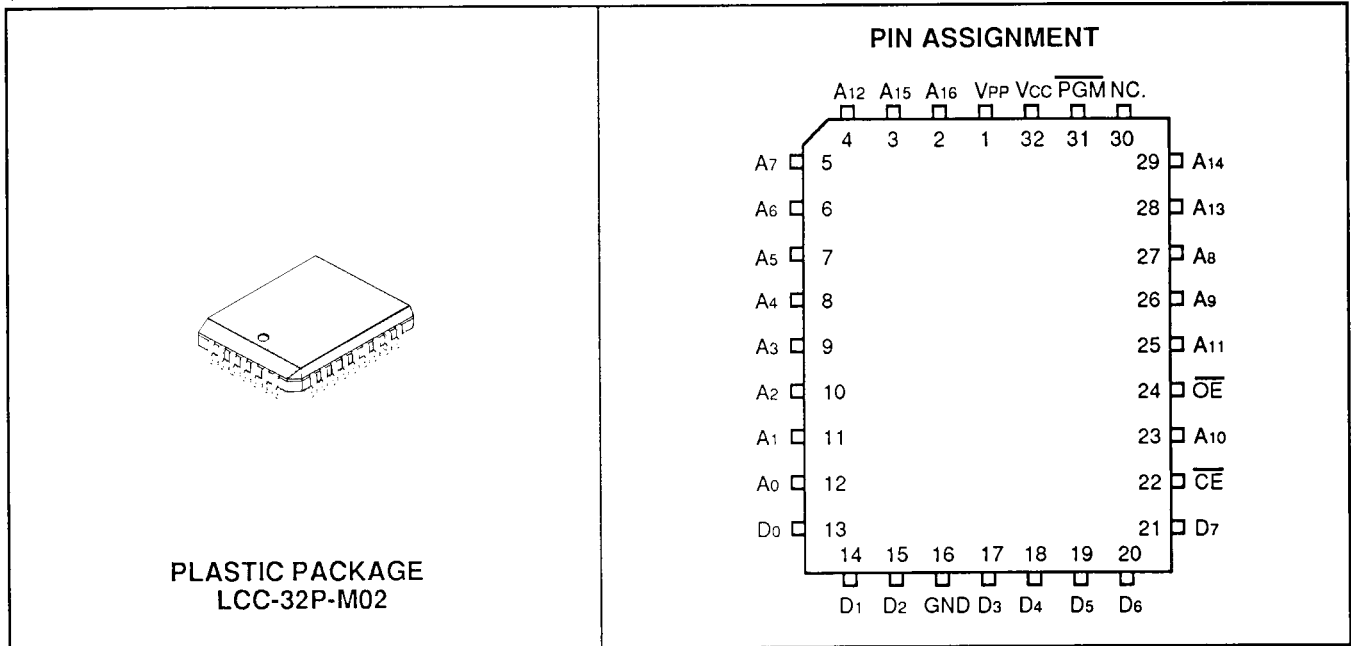


© 1990 FUJITSU LIMITED F32006S-3C

Dimensions in
inches (millimeters)

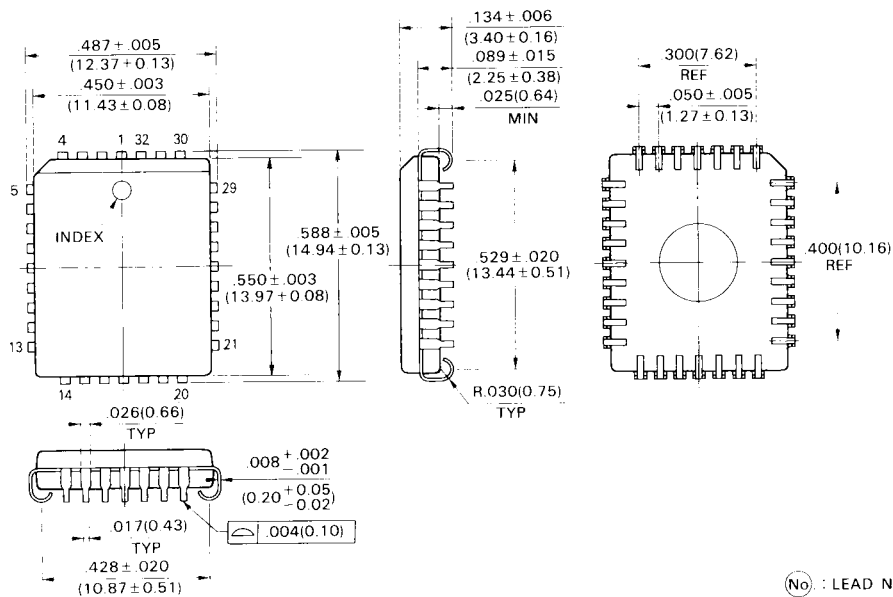
PACKAGE DIMENSIONS

(Suffix: PD)



PLASTIC PACKAGE
 LCC-32P-M02

32-LEAD PLASTIC LEADED CHIP CARRIER (CASE No.: LCC-32P-M02)



(No.) : LEAD No.

Dimensions in
 inches (millimeters)