MB87033B
SCSI Protocol Controller (SPC) with On-Chip Drivers/Receivers

Edition 1.0
September 1989

GENERAL DESCRIPTION

The MB87033B SCSI Protocol Controller (SPC) is a CMOS LSI circuit specifically designed to control a Small Computer Systems Interface (SCSI). The MB87033B establishes the Fujitsu SPC family of protocol controllers by providing software enhancements and other functional features that will meet all facets of the SCSI specification (ANSI X 3.131-1986).

To achieve optimum performance and interface flexibility, the MB87033B provides an 8-byte First-In First-Out (FIFO) data buffer register and a 28-bit transfer byte counter which allows burst transfers of up to 256 megabytes. To improve programming requirements, "Attention Detect" and "Arbitration Fail" interrupts are provided and on-chip driver/receiver circuits simplify interface connections. Data transfers can be executed in either the asynchronous or synchronous mode with a maximum offset of 8 bytes.

SCSI Compatibility

- Supports all mandatory commands, many optional commands, and some extended commands of SCSI specification (ANSI X 3.131, 1986)
- Software compatible with MB8703X and MB8935X SPCs
- Serves as either INITIATOR or TARGET

Data Bus

- Independent buses for CPU and DMA controller

Transfer Modes

- Asynchronous
- Synchronous mode transfers with programmable offset of up to eight bytes (8 Byte FIFO)

Data Transfer Speed

- Up to a maximum of 5 megabytes/sec

Selectable Operating Modes

- DMA transfer
- Program transfer
- Manual transfer
- Diagnostic

Interface

- On-chip, single-ended Drivers/Receivers
- Guaranteed to sink 48mA regardless of the number of outputs simultaneously asserted.

Enhancements

- On-chip parity generation
- Attention condition detect interrupt
- Arbitration fail interrupt

Clock Requirements

- 10 MHz clock

Technology/Power Requirements

- Silicon-gate CMOS
- Single +5 V power supply

Available Packaging

- 84-pin plastic leadless chip carrier
- 80-pin plastic flat package

ABSOLUTE MAXIMUM RATINGS[1]

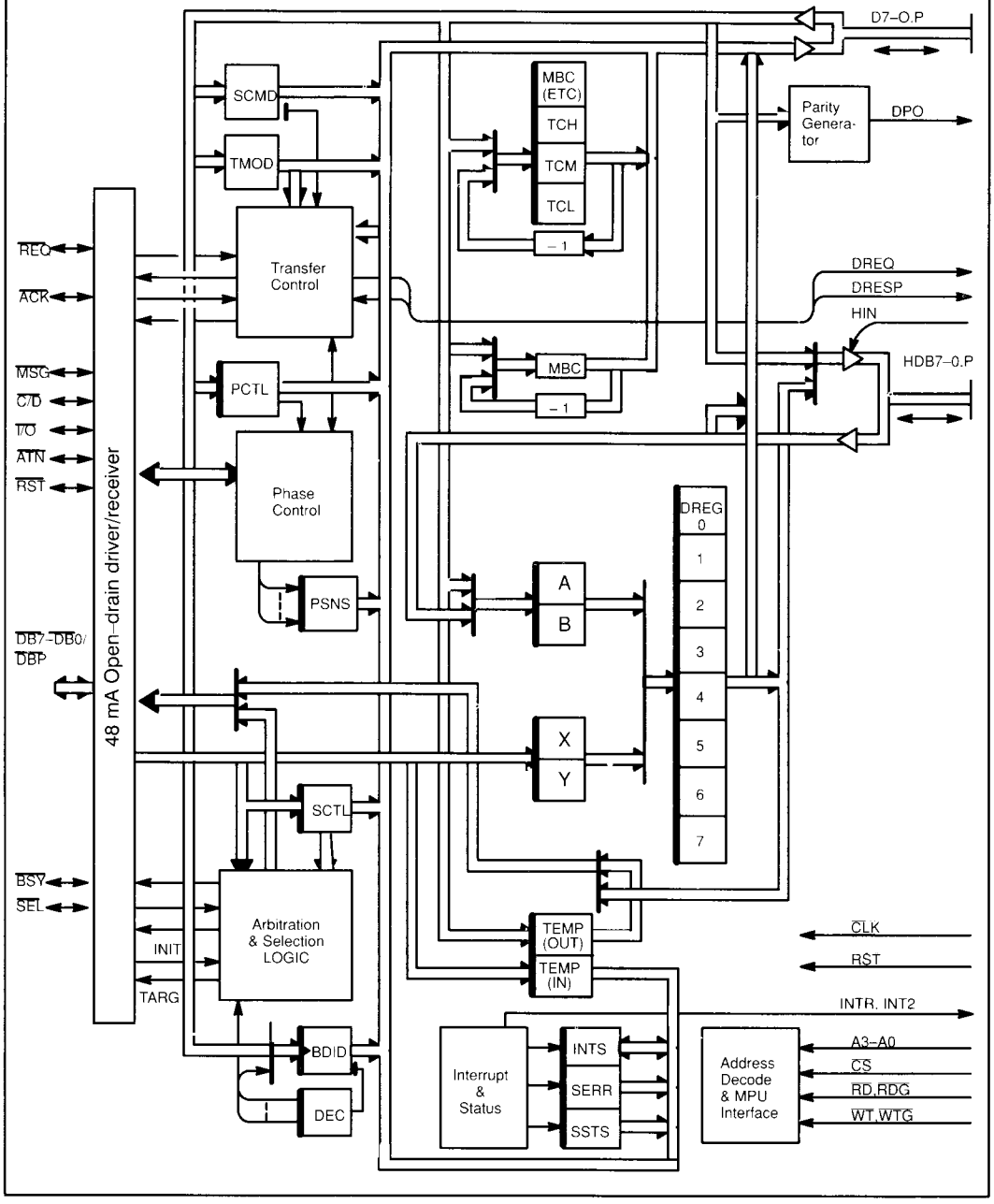
Rating	Symbol	Values		Unit
		Min.	Max.	
Supply Voltage	V_{DD}	V_{SS}[2] –0.3	6.0	V
Input Voltage	V_I	V_{SS}[2] –0.3	V_{DD} + 0.3	V
Output Voltage[2]	V_O	V_{SS}[2] –0.3	V_{DD} + 0.3	V
Storage Temperature (Ceramic)	T_{STG}	–65	+125	°C

Notes: 1 Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2 V_{SS} = 0V.

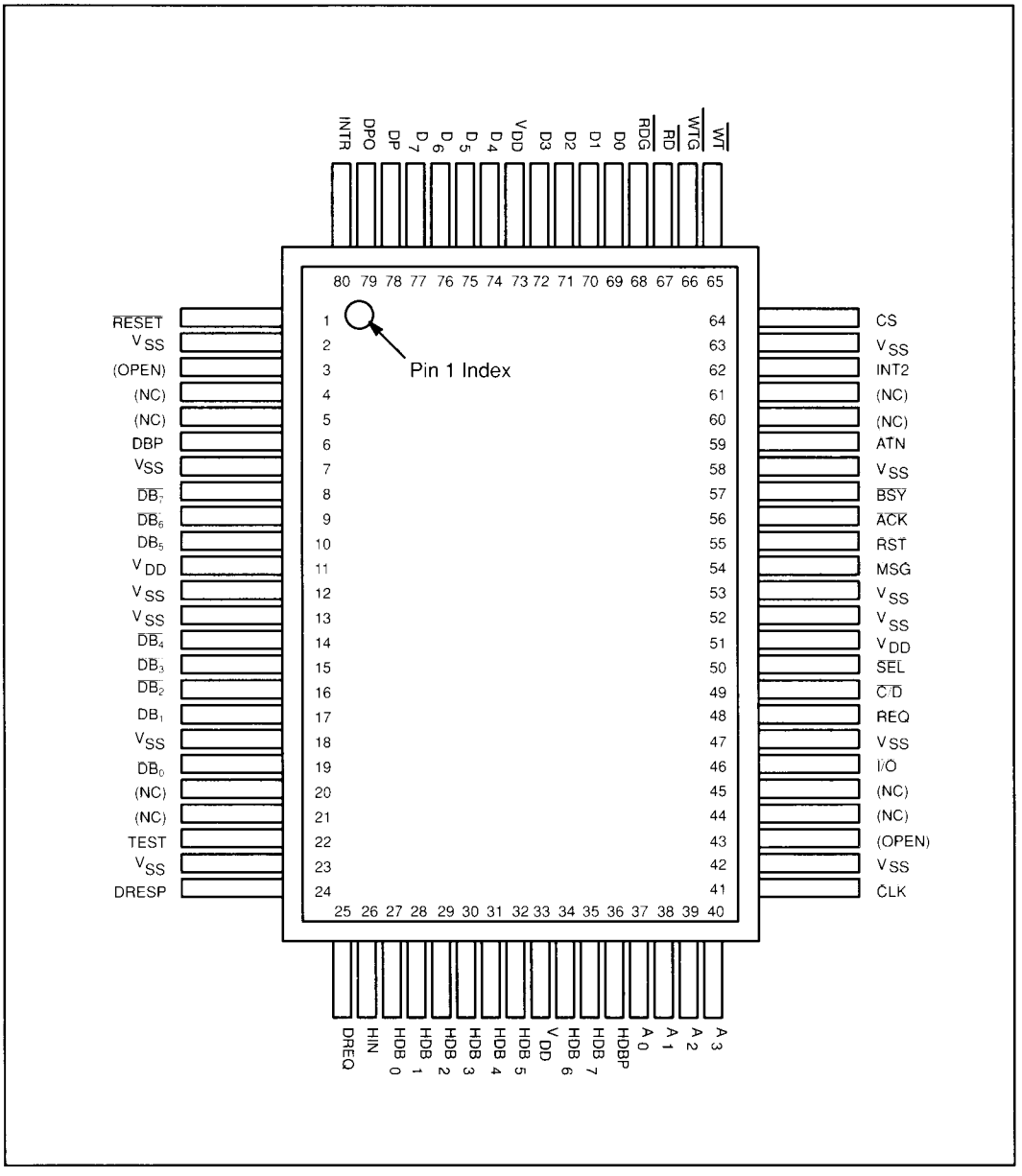
3 Not more than one output may be shorted at a time for a maximum duration of one second.

MB87033B BLOCK DIAGRAM



PIN ASSIGNMENTS

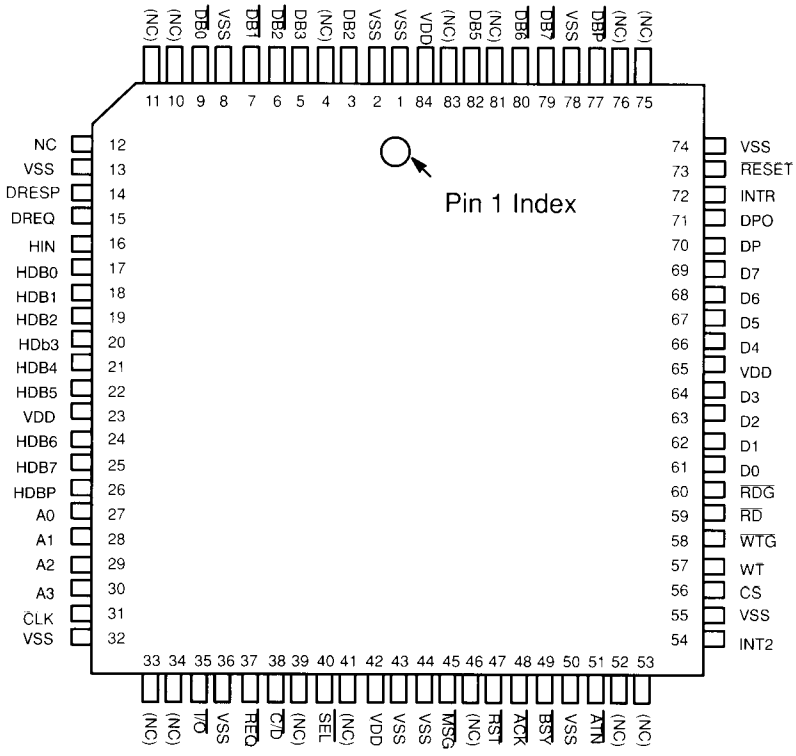
80-Pin Plastic Flat Package



PIN ASSIGNMENTS

84-Pin Plastic Leadless Chip Carrier

(Top View)



PIN DESCRIPTIONS

Pin Number		Designator	Function
FPT	PLCC		
1	73	$\overline{\text{RESET}}$	When set to the active-low state, an asynchronous reset signal that clears all internal circuits of the SPC.
2,7, 12,13 18,23 42,47 52,53 58,63	1,2 8,13 32,36 43,44 50,55 74,78	V_{SS}	Power supply ground.
3,43	—	Open	Reserved. (Note: Do not make external connections to these pins.)
4,5 20,21 44,45 60,61	4,10 11,12 33,34 39,41 46,52 53,75 76,81,83	NC	No internal connection. (Note: These pins must be open connections at all times.)
8 9 10 14 15 16 17 19 6	79 80 82 3 5 6 7 9 77	$\overline{\text{DB7}}$ $\overline{\text{DB6}}$ $\overline{\text{DB5}}$ $\overline{\text{DB4}}$ $\overline{\text{DB3}}$ $\overline{\text{DB2}}$ $\overline{\text{DB1}}$ $\overline{\text{DB0}}$ $\overline{\text{DBP}}$	Inputs/outputs for the SCSI data bus; these I/O pins connect directly to the SCSI connector. $\overline{\text{DB7}}$ is the MSB; $\overline{\text{DB0}}$ is the LSB. $\overline{\text{DBP}}$ is an odd parity bit.
11,33 51,73	23,42 65,84	VDD	+5V power supply.
22		TEST	Reserved for test functions. (Note. Do not make external connections to these pins.)
24	14	DRESP	DRESP is a response signal to the data transfer request signal DREQ. The DRESP pin must be refreshed with an applied pulse after each byte of data is transferred. In the DMA mode, DRESP is used as a timing signal for completion of a data-byte transfer.

Continued on following page

PIN DESCRIPTIONS

Pin Number		Designator	Function
FPT	PLCC		
25	15	DREQ	When executing a data transfer cycle in the DMA mode, DREQ is used to indicate a request for a data transfer between the SPC and external buffer memory. In the DMA mode, routing of data is as shown below. **Output Operation:** External buffer memory to SPC to SCSI bus. **Input Operation:** SCSI bus to SPC to external buffer memory. In an output operation, DREQ becomes active to request a data transfer to the external buffer memory when the FIFO contains valid data.
26	16	HIN	Indicates direction of transmission along data bus lines HDB0-HDB7 and HDBP in the DMA transfer mode. To be executed, direction of transmission must be properly coordinated with internal operation of the SPC. When HIN is low (inactive), the data bus lines are placed in the high-impedance state (input mode). When HIN is high (active) all bus lines are switched to the output mode.
35 34 32 31 30 29 28 27 36	25 24 22 21 20 19 18 17 26	HDB7 HDB6 HDB5 HDB4 HDB3 HDB2 HDB1 HDB0 HDBP	3-state bidirectional data bus for transferring data to or from the external buffer memory in the DMA mode. As shown below, the direction of data transmission depends on the HIN input signal. **HIN** **HDBn** **Operation** L Input Mode Output H Output Mode Input
37–40	27–30	A0–A3	Address input signals for selecting an internal register in the SPC. The MSB is A3; the LSB is A0. When $\overline{CS}$ is active low, read/write is enabled and an internal register is selected by these address inputs via data bus lines D0-D7 and DP.
41	31	$\overline{CLK}$	Input clock for controlling internal operations and data-transfer speeds of SPC.

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PIN DESCRIPTIONS

Pin Number		Designator	Function
FPT	PLCC		
57 50 48 56 54 49 46 59 55	49 40 37 48 45 38 35 51 47	$\overline{BSY}$ $\overline{SEL}$ $\overline{REQ}$ $\overline{ACK}$ $\overline{MSG}$ $\overline{C/D}$ $\overline{I/O}$ $\overline{ATN}$ $\overline{RST}$	Input/output control signals for SCSI bus.
62	54	INT2	A non-maskable interrupt request signal that indicates a reset condition on the SCSI bus.
64	56	$\overline{CS}$	Selection enable signal for accessing an internal register in the SPC. When CS is active low, the following signals are valid: $\overline{RD}$, $\overline{WT}$, A0–A3, D0–D7 and DP.
65	57	$\overline{WT}$	Input strobe used for writing data into an internal register of the SPC; this signal is asserted only if $\overline{CS}$ is active low. On the trailing edge of $\overline{WT}$, data placed on data bus lines D0-D7/DP is loaded into the internal register selected by address inputs A0-A3, except when all address lines are high (A0-A3 = H).
66	58	$\overline{WTG}$	While this signal is active low, data placed on data bus lines D0-D7/DP is output to HDB0-HDB7/HDBP, provided the following input conditions are satisfied: CS and HIN = H $\overline{A0}$–A3 = H
67 68	59 60	$\overline{RD}$ $\overline{RDG}$	Input strobes used for reading out contents of internal register; strobes are effective only when $\overline{CS}$ is active low. When $\overline{RDG}$ is active low, the contents of an internal register selected by address inputs A0–A3 are placed on data bus lines D0–D7/DP. For a data transfer cycle in the program transfer mode, the trailing edge of RD is used as a timing signal to indicate the end of data read.

Continued on following page

PIN DESCRIPTIONS

Pin Number		Designator	Function
FPT	PLCC		
69 70 71 72 74 75 76 77	61 62 63 64 66 67 68 69	D0 D1 D2 D3 D4 D5 D6 D7	Used for writing or reading data into or from an internal register of the SPC; these bus lines are 3-state and bidirectional. The MSB is D7; the LSB is D0. DP is an odd parity bit.
78	70	DP	When the $\overline{CS}$ and $\overline{RDG}$ inputs are active low, contents of the internal register are output to the data bus (read operation). In operations other than read, these bus lines are kept in a high-impedance state.
79	71	DPO	An odd parity output for data byte D7–D0. DPO represents an output when D7–D0/DP are placed in a high-impedance state; DPO is in a high-impedance state when D7–D0/DP serve as outputs. If a parity bit is not generated for external memory, DPO can be used as an input for DP.
80	72	INTR	When active high, requests an interrupt to indicate completion of an SPC internal operation or the occurrence of an error; the INTR interrupt request can be masked by user software. When an interrupt request is honored, INTR remains in the active state until cause of the interrupt is cleared.

ADDRESSING OF INTERNAL REGISTERS

The MB87033B SPC contains16 byte-wide registers that are externally accessible. These registers are used to control internal operations of the SPC and also to indicate processing/result status. A unique address, identified by address bits A3–A0, is assigned to each of the sixteen registers. These addresses are defined in Table 1.

Note: *The phase sense (PSNS) and SPC diagnostic (SDGC) registers have the same hexadecimal address. However, depending upon whether a read or write command is executed, the register provides two separate functions.*

Table 1. Internal Register Addressing

Register	Mnemonic	Operation	Chip Select ($\overline{CS}$)	Address Bits A3	A2	A1	A0
Bus Device ID	BDID	R	0	0	0	0	0
		W					
SPC Control	SCTL	R	0	0	0	0	1
		W					
Command	SCMD	R	0	0	0	1	0
		W					
Transfer Mode	TMOD	R	0	0	0	1	1
		W					
Interrupt Sense	INTS	R	0	0	1	0	0
Reset Interrupt		W					
Phase Sense	PSNS	R	0	0	1	0	1
SPC Diagnostic Control	SDGC	W					
SPC Status	SSTS	R	0	0	1	1	0
SPC Error Status	SERR	R	0	0	1	1	1
Phase Control	PCTL	R	0	1	0	0	0
		W					
Modified Byte Counter	MBC	R	0	1	0	0	1
Extended Transfer Count		W					
Data Register	DREG	R	0	1	0	1	0
		W					

Continued on following page

Table 1. Internal Register Addressing

Register	Mnemonic	Operation	Chip Select ($\overline{CS}$)	Address Bits A3	A2	A1	A0
Temporary Register	TEMP	R	0	1	0	1	1
		W					
Transfer Counter (High)	TCH	R	0	1	1	0	0
		W					
Transfer Counter (Middle)	TCM	R	0	1	1	0	1
		W					
Transfer Counter (Low)	TCL	R	0	1	1	1	0
		W					
External Buffer	EXBF	R	0	1	1	1	1
		W					

BIT ASSIGNMENTS FOR INTERNAL REGISTERS

Table 2 lists the bit assignments for the sixteen internal registers defined in Table 1. In most cases, bit assignments for the MB87033B SPC are identical to those for the MB87030/31; however, in the MB87033B, some features are expanded and others are added to improve overall performance. These modifications and additions are summarized as follows:

MPU Bus Parity Generator

An odd parity bit is output from DPO (pin 79 in FPT, pin 71 in PLCC) for each data byte (D7-D0). DPO is a 3-state pin and is placed in a high-impedance state when data from D7-D0 is output to the MPU. If the MPU interface does not contain a parity generator, the output of DPO can be connected to the DP input pin of the SPC (pin 78 in FPT, pin 70 in PLCC).

Reset Condition Interrupt Request Signal

The INT2 output (pin 62 in FPT, pin 54 in PLCC) is a non-maskable interrupt request that, when driven High, notifies the MPU when a reset condition is detected on the SCSI bus. Bit 4 (Reset Condition Interrupt Mask Enable) of the Phase Control (PCTL) register does not affect the INT2 output pin.

When a bus reset condition is detected, the INTR output (pin 80 in FPT, pin 72 in PLCC) also is driven to the high state; however, the state of INTR can be masked by bit 4 of the PCTL register:

Bit 4 = 0: INTR goes high when a reset condition is detected.

Bit 4 = 1: INTR does not go high when a reset condition is detected.

Lost Arbitration Interrupt Request

If bit 6 (Lost Arbitration Interrupt Enable) of the phase control (PCTL) register is set to "1", a COMMAND COMPLETE interrupt is generated when the SPC (serving as initiator or target) loses in the ARBITRATION process. To determine the cause of a COMMAND COMPLETE interrupt (completion of SELECTION, RESELECTION, or lost ARBITRATION), refer to bits 6 (TARGET) and 7 (INITIATOR) of the SPC status (SSTS) register. If both bits are set to "0", the COMMAND COMPLETE interrupt is a result of lost arbitration.

Attention Condition Interrupt

If bit 5 (Attention Condition Interrupt Enable) of the phase control (PCTL) register is set to "1" and the SPC serves as a target, a service required interrupt occurs. To reset the service required interrupt, set bit 3 of the interrupt sense (INTS) register to "1" or revoke the current target role of the SPC.

Expansion of Transfer Byte Counter

If bit 0 of the transfer mode (TMOD) register is set to "1", the transfer byte counter is expanded to 28-bits. In the expanded mode, the high nibble (bits 24 through 27) are entered into the four most significant bit positions (7 bits through 4) of the modified byte count (MBC) register.

Note: *When a hardware data transfer or execution of a SELECT command is in process, access to the TMOD register is forbidden.*

Bit 0 of the TMOD register =1

To access the highest four bits (bits 27 through 24) of the transfer byte counter, data reads or writes are addressed to the high nibble of the modified byte counter (MBC) register. When a TRANSFER or SELECT command is issued, the transfer byte count (or t_{WAIT}) should be placed in the high nibble of the MBC register rather than the TCH, TCM, and TCL registers.

Bit 0 of the TMOD register = 0

The transfer byte counter is not expanded to 28-bits; hence, reading the high nibble of MBC yields a "0" even though some particular value is written into the register. In this case, t_{WAIT} or the transfer byte count is based on a 24-bit transfer byte counter (identical to the MB87030/MB87031).

During read/write access of an internal register, the following rules are invoked:

(1) Internal registers include only those registers identified in Table 2.
(2) A write command to a read-only register is ignored.
(3) For write operations, all bit positions with a "—" (blank) designator can be written as "0" or as a "1".
(4) All bit positions with an assigned "0" are always read as a zero (0).

Table 2. Bit Assignments For Internal Registers

HEX Address	Register and Mnemonic	R/W Operation	7 (MSb)	6	5	4	3	2	1	0 (LSb)	Parity
0	Bus Device ID (BDID)	R	#7	#6	#5	#4	#3	#2	#1	#0	0
		W	SCSI Bus Device ID ID4					ID2		ID1	—
1	SPC Control (SCTL)	R	Reset & Disable	Control Reset	Diag Mode	ARBIT Enable	Parity Enable	Select Enable	Reselect Enable	INT Enable	P
		W									
2	Command (SCMD)	R	Command Code			RST Out	Intercept Xfer	Transfer PRG Xfer	Modifer 0	Term Mode	P
		W									
3	Transfer Mode (TMOD) Command	R	Sync. Xfer	Max. Transfer Offset 4	2	1	Min. Transfer Period 2	1	0	Xfer Counter Expand	P
		W									
4	Interrupt Sense (INTS)	R	Selected	Reselected	Disconnect	Command Complete	Service Required	Time Out	SPC Hard Error	Reset Condition	P
		W	Reset Interrupt								—
5	Phase Sense (PSNS)	R	REQ	ACK	ATN	SEL	BSY	MSG	C/D	I/O	P
	SPC Diag Control (SDGC)	W	Diag. REQ	Diag. ACK		—	Diag. BSY	Diag. MSG	Diag. C/D	Diag. I/O	—
6	SPC Status (SSTS)	R	Connected INIT	TARG	SPC BSY	Xfer In Progress	SCSI RST	TC=0	DREG Status Full	Empty	P
7	SPC Error Status (SERR)	R	Data Error SCSI	SPC	0	0	TC Parity Error	Phase Error	Short Xfer Period	Offset Error	P

Continued on following page

Table 2. Bit Assignments For Internal Registers

HEX Address	Register and Mnemonic	R/W Operation	7 (MSb)	6	5	4	3	2	1	0 (LSb)	Parity
8	Phase Control (PCTL)	R	Bus Free Interrupt Enable	Arbitration Fail Interrupt Enable	Attention Condition Interrupt Enable	Reset Condition Interrupt Mask	0	Transfer Phase			P
		W						MSG Out	C/D Out	I/O Out	
9	Modified Byte Counter (MBC)	R	Extended Transfer Counter				Bit 3	Bit 2	Bit 1	Bit 0	
		W	Bit 27	Bit 26	Bit 25	Bit 24					P
A	Data Register (DREG)	R	Internal Data Register (8 Byte FIFO)								
		W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	P
B	Temporary Register (TEMP)	R	Temporary Data (Input: From SCSI)								
			Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	P
		W	Temporary Data (Output: To SCSI)								
			Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	P
C	Transfer Counter High (TCH)	R	Transfer Counter High (MSB)								
		W	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16	P
D	Transfer Counter Mid (TCM)	R	Transfer Counter Middle (2nd Byte)								
		W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	P
E	Transfer Counter LOW (TCL)	R	Transfer Counter Low (LSB)								
		W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	P
F	External Buffer (EXBF)	R	External Buffer								
		W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	P

DC CHARACTERISTICS
(Recommended operating conditions unless otherwise specified)

SCSI Bus Pins

Parameter	Designator	Condition	Values			Unit
			Min.	Typ.	Max.	
Input Voltage	V_{IH}		2.0		5.25	V
	V_{IL}		0.0		0.8	V
Input Current	I_{IH}	V_{IH} = 5.25V			10	µA
	I_{IL}	V_{IL} = 0.0V			–10	µA
Output Voltage	V_{OL}	V_{DD} = 4.75V I_{OL} = 48 mA			0.5	V
Input Hysteresis Width	V_{HW}		0.2			V

Other than SCSI Bus Pins

Parameter	Designator	Condition	Values			Unit
			Min.	Typ.	Max.	
Input Voltage	V_{IH}		2.2		V_{DD} + 0.3	V
	V_{IL}		V_{SS}–0.3		0.8	V
Output Voltage	V_{OH}	I_{OH} = –0.4mA	4.2		V_{DD}	V
	V_{OL}	I_{OL} = 3.2mA	V_{SS}		0.4	
Input Leakage Current	I_{LIH}	V_{IH} = 5.25V			10	µA
	I_{LIL}	V_{IL} = 0.0V			–10	µA
Input/Output Leakage Current	I_{LIH}	V_{IH} = 5.25V			10	µA
	I_{LIL}	V_{IL} = 0.0V			–10	µA
Supply Current	I_{DD}	10 MHz Clock Outputs Open			30	mA

TA = 0 – 70°C, V_{DD} + 5V ± 5%

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DC CHARACTERISTICS
(Recommended operating conditions unless otherwise specified)

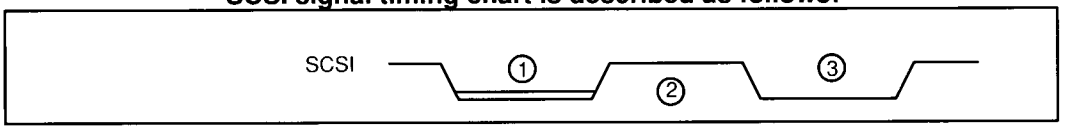
Capacitance

Parameter	Designator	Condition	Values			Unit
			Min.	Typ.	Max.	
Input pin capacitance	C_{IN}	$_TA_=$ 25C, V_{DD}= V_I=OV, f – 1MHz			9	pF
Output capacitance	C_{OUT}	$_TA_=$ 25C, V_{DD}= V_I=OV, f – 1MHz			9	pF
I/O pin capacitance[2]	$C_{I/O}$	$_TA_=$ 25C, V_{DD}= V_I=OV, f – 1MHz			11	pF
I/O pin capacitance[3]	$C_{I/O}$	$_TA_=$ 25C, V_{DD}= V_I=OV, f – 1MHz			30	pF

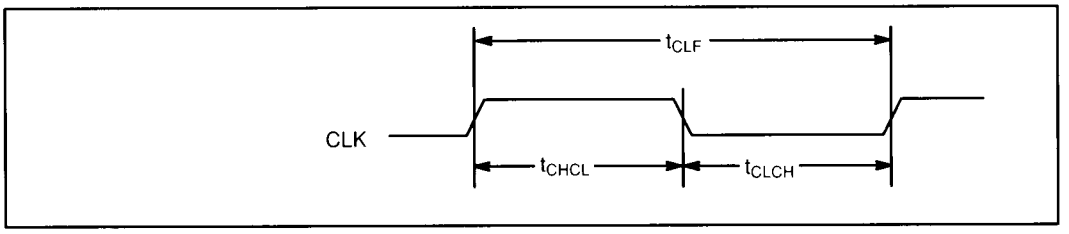
Notes: [1]SCSI bus Pins are $\overline{DB7}$–$\overline{DB0}$, $\overline{DBP}$, $\overline{RST}$, $\overline{SEL}$, $\overline{I/O}$, $\overline{C/D}$, $\overline{MSG}$, $\overline{ATN}$, $\overline{REQ}$, $\overline{ACK}$, and $\overline{BSY}$.
[2]For all I/O pins except SCSI bus pins.
[3]For SCSI bus pins only (see note 1).

AC CHARACTERISTICS

SCSI signal timing chart is described as follows:

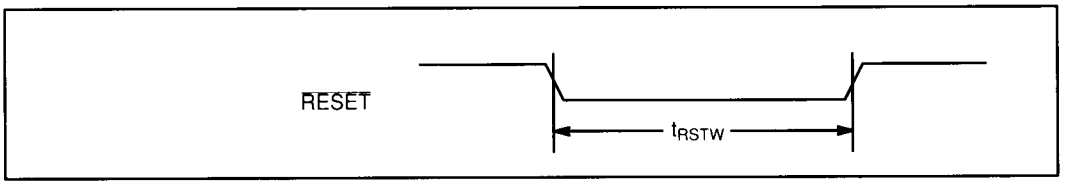


Notes: 1 Output "L"
2 No device is outputting "L".
3 The other device is outputting "L".



Clock

Parameter	Designator	Values			Unit
		Min.	Typ.	Max.	
Clock cycle time	t_{CLF}	100		200	ns
Clock "H" Pulse width	t_{CHCL}	50			ns
Clock "L" Pulse width	t_{CLCH}	40			ns

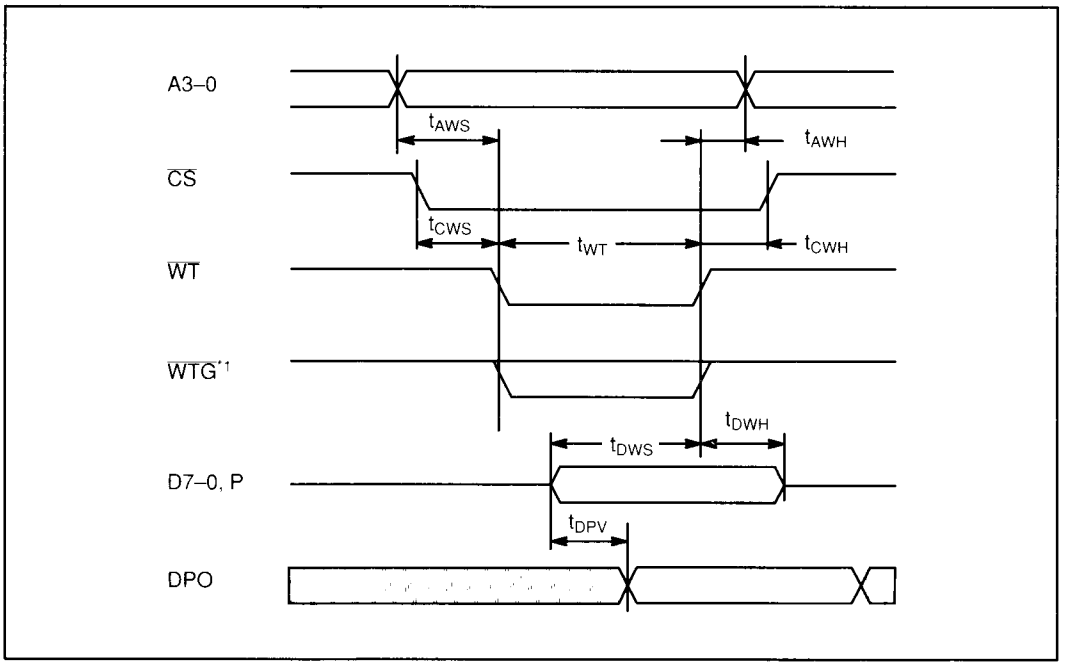


Hardware Reset

Parameter	Designator	Values			Unit
		Min.	Typ.	Max.	
Reset Pulse Width	t_{RSTW}	50			ns

AC CHARACTERISTICS (Continued)

Register Write (except EXBF)



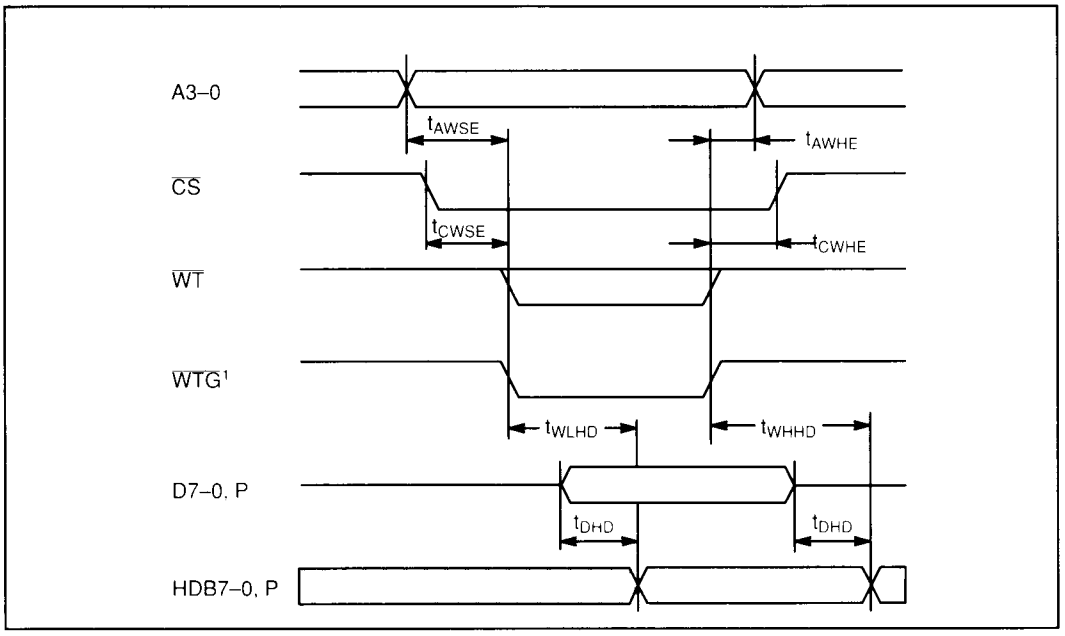
Register Write

Parameter	Designator	Values			Unit
		Min.	Typ.	Max.	
Address set-up	t_{AWS}	35			ns
Address hold	t_{AWH}	5			ns
$\overline{CS}$ set-up	t_{CWS}	20			ns
$\overline{CS}$ hold	t_{CWH}	10			ns
Data bus set-up	t_{DWS}	25			ns
Data bus hold	t_{DWH}	20			ns
$\overline{WT}$ Pulse width	t_{WT}	50			ns
Data bus valid → DPO valid	t_{DPV}			55	ns

Note: 1 $\overline{WTG}$ is input at the same timing as $\overline{WT}$ or held to "H".

AC CHARACTERISTICS (Continued)

Register Write (EXBF)

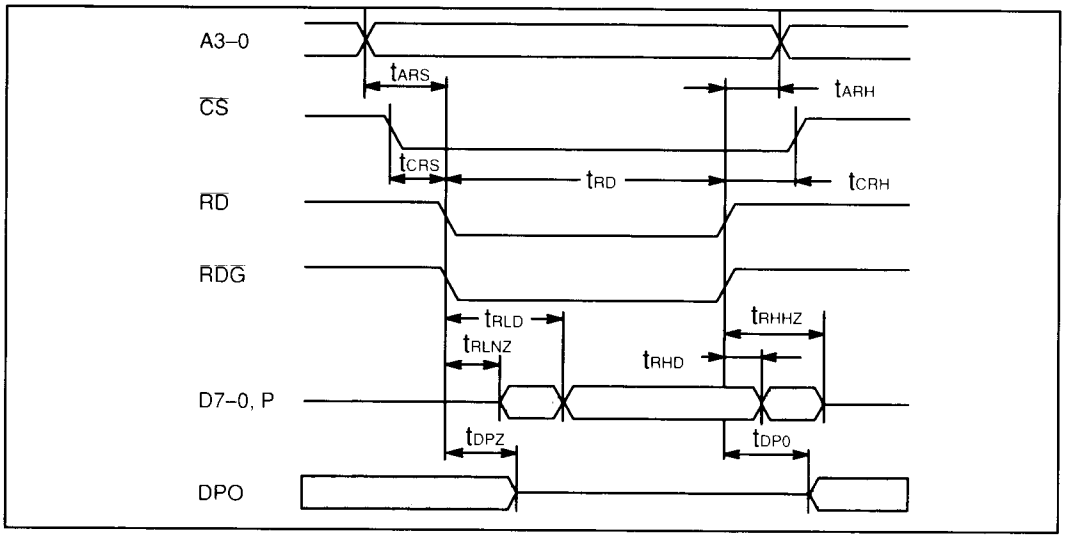


Register Write					
Parameter	Designator	Values			Unit
		Min.	Typ.	Max.	
Address set-up	t_{AWSE}	35			ns
Address hold	t_{AWHE}	5			ns
$\overline{CS}$ set-up	t_{CWSE}	20			ns
$\overline{CS}$ hold	t_{CWHE}	10			ns
$\overline{WTG}^1$ "L" → DMA pulse output valid	t_{WLHD}			55	ns
$\overline{WTG}^1$ "H" → DMA pulse output invalid	t_{WHHD}	10			ns
MPU data bus → DMA bus delay	t_{DHD}			50	ns

Note: 1 $\overline{WTG}$ is input at the same timing as $\overline{WT}$ or held to "H".

AC CHARACTERISTICS (Continued)

Register Read (except EXBF)



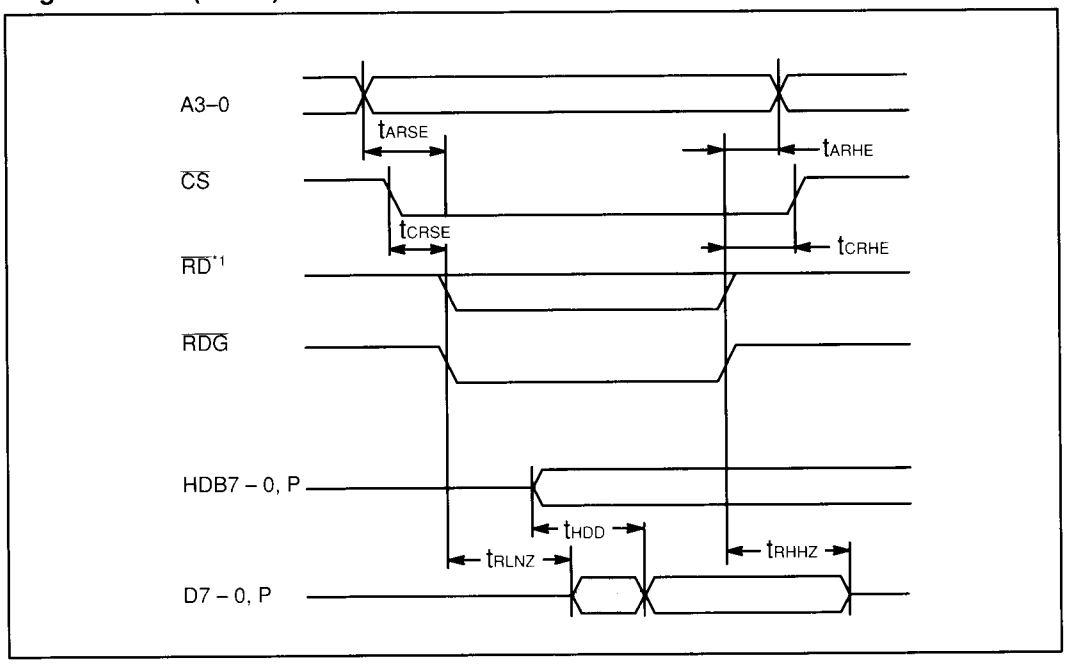
Register Read

Parameter		Designator	Values			Unit
			Min.	Typ.	Max.	
Address set-up		t_{ARS}	35			ns
Address hold		t_{ARH}	5			ns
$\overline{CS}$ set-up		t_{CRS}	20			ns
$\overline{CS}$ hold		t_{CRH}	10			ns
$\overline{RDG}$ "L" " Data bus ourpur valid		t_{RLNZ}	10		40	ns
$\overline{RDG}$ "H" " Data bus output valid		t_{RHHZ}	10		40	ns
$\overline{RD}$ "L" " Data Valid	D7–0	t_{RLD}			70	ns
	DP				85	ns
$\overline{RD}$ "H" " Data Invalid		t_{RHD}	10			ns
$\overline{RD}$ Pulse width		t_{RD}	50			ns
*1 $\overline{RDG}$ "L" " Data High-Z		t_{DPZ}	10		40	ns
*1 $\overline{RDG}$ "H" " DPO		t_{DPO}	10		40	ns

Note: 1 = DPO goes to High-Z when both $\overline{RDG}$ and $\overline{CS}$ are "L".

AC CHARACTERISTICS (Continued)

Register Read (EXBF)



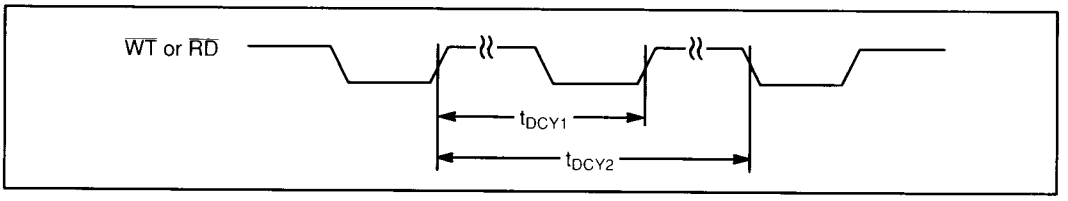
Note: 1 $\overline{RD}$ is input at the same timing as $\overline{RDG}$ or held to "H".

Register Read

Parameter	Designator	Values			Unit
		Min.	Typ.	Max.	
Address set-up	t_{ARSE}	35			ns
Address hold	t_{ARHE}	5			ns
$\overline{CS}$ set-up	t_{CRSE}	20			ns
$\overline{CS}$ hold	t_{CRHE}	10			ns
$\overline{RDG}$ "L" → Data bus output	t_{RLNZ}	10		40	ns
$\overline{RDG}$ "H" → Data bus High-Z	t_{RHHZ}	10		40	ns
DMA bus → MPU data bus delay	t_{HDD}			50	ns

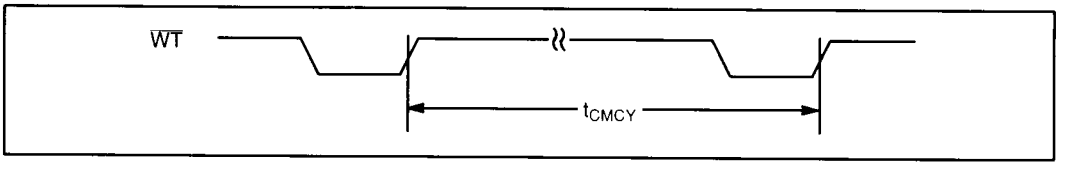
AC CHARACTERISTICS (continued)

DREG Access Cycle Time



DREG

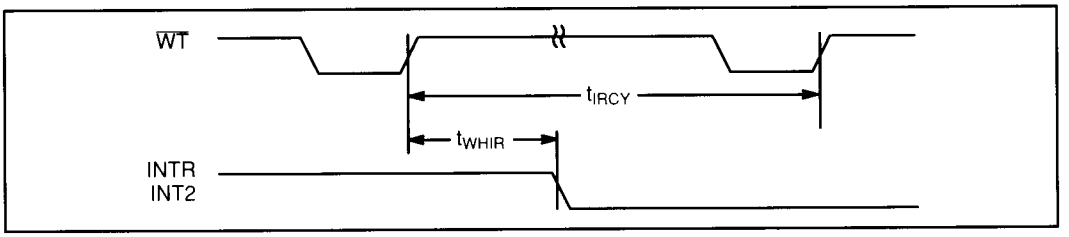
Parameter	Designator	Values			Unit
		Min.	Typ.	Max.	
DREG access cycle time	t_{DCY1}	$2t_{CLF}$			ns
DREG access cycle time	t_{DCY2}	$3t_{CLF}$			ns



Command Issue Cycle Time

Parameter	Designator	Values			Unit
		Min.	Typ..	Max	
SCMD register access cycle time	t_{CMCY}	$4t_{CLF}$			ns

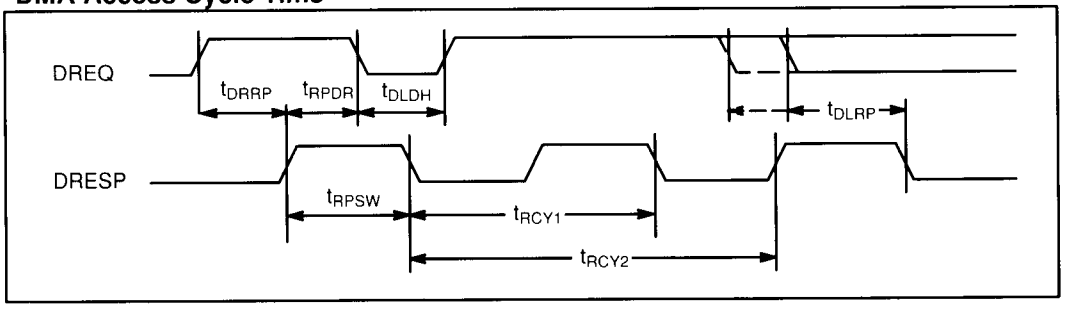
AC CHARACTERISTICS (continued)



Interrupt Reset

Parameter	Designator	Values			Unit
		Min.	Typ.	Max.	
WT "H" " Interrupt output (INTR.INT2) "L"	t_{WHIR}	t_{CLF}		$3t_{CLF} + 80$	ns
INTS register access cycle time	t_{IRCY}	$4t_{CLF}$			ns

DMA Access Cycle Time

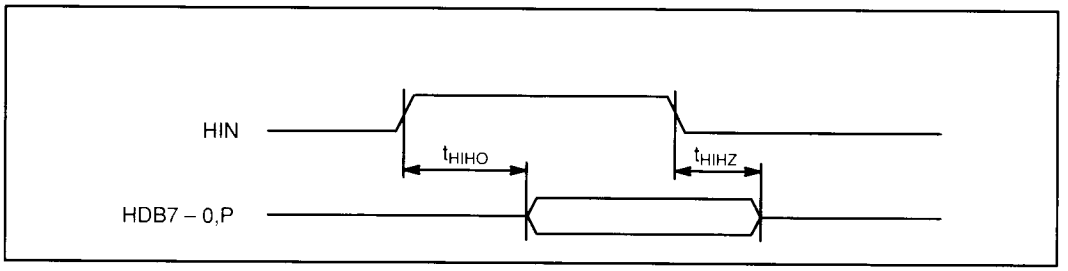


DMA Access Timing

Parameter	Designator	Values			Unit
		Min.	Typ.	Max.	
DREQ "H" → DRESP "H"	t_{DRRP}	t_{CLF}			ns
DRESP "H" → DREQ "L"	t_{RPDR}	5		70	ns
DREQ "L" → DREQ "H"	t_{DLDH}	0			ns
DRESP Pulse Width	t_{RPSW}	50			ns
DRESP Cycle time	t_{RCY1}	$2t_{CLF}$			ns
DRESP Cycle time	t_{RCY2}	$3t_{CLF}$			ns
DREQ "L" → DRESP "L"[1]	t_{DLRP}			$5t_{CLF}$	ns

Note: 1 This parameter is applicable when the data buffer hold function or the Transfer Pause command is used and DREQ goes low asynchronously to DRESP. Under these conditions, data cannot be written to the data buffer until t_{DLRP} and t_{RPSW} are satisfied.

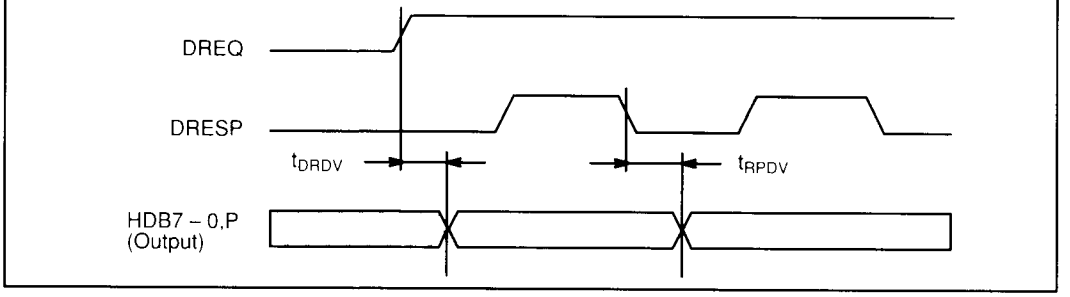
AC CHARACTERISTICS (continued)



DMA Bus Output Control

Parameter	Designator	Values			Unit
		Min.	Typ.	Max.	
HIN "H" → DMA bus output	t_{HIHO}	5		40	ns
HIN "L" → DMA bus High-Z	t_{HIHZ}	5		40	ns

DMA Transfer – Data Input from SCSI

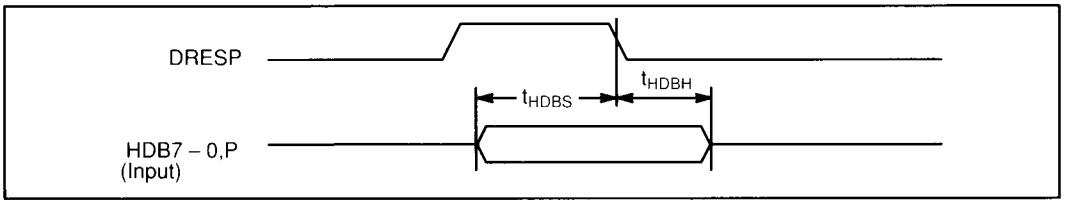


DMA Transfer (1) – Data Input from SCSI

Parameter	Designator	Values			Unit
		Min.	Typ.	Max.	
DREQ "H" → Output data[1] valid	t_{DRDV}			60	ns
DRESP "L" → Output data switch	t_{RPDV}	15		90	ns

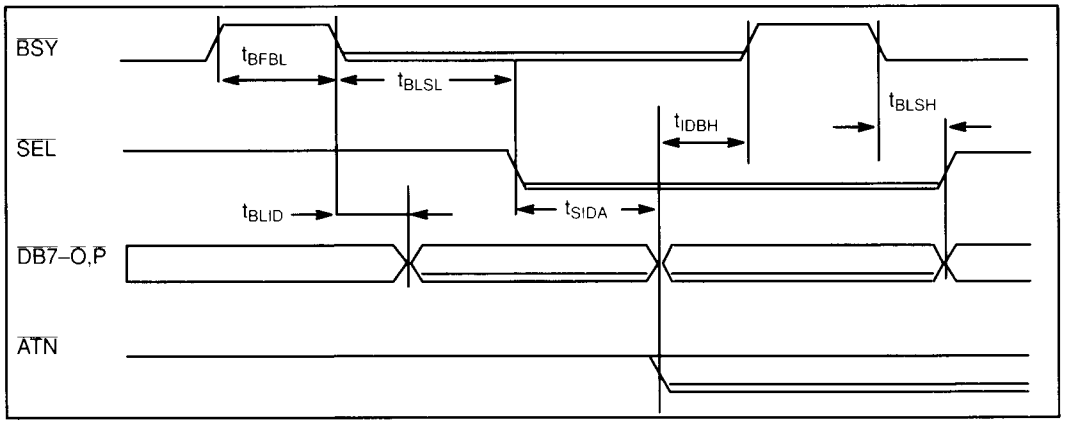
Note: 1 This parameter is applied when the internal data buffer goes Not Empty from Empty.

AC CHARACTERISTICS (continued)



DMA Transfer – Data Output to SCSI					
Parameter	Designator	Values			Unit
		Min.	Typ.	Max.	
Input data set up	t_{HDBS}	20			ns
Input data hold	t_{HDBH}	20			ns

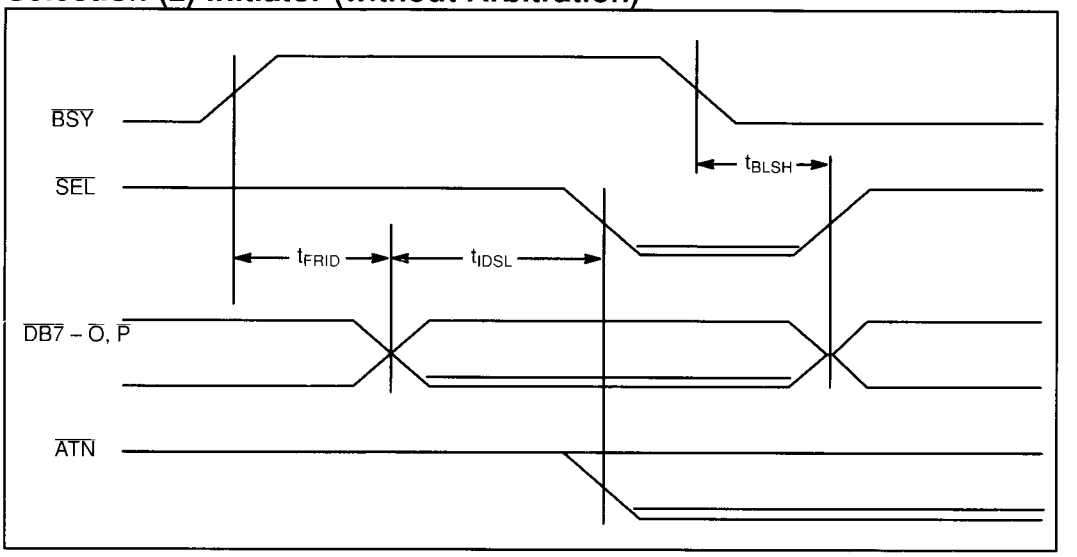
Selection (1) Initiator (with Arbitration)



Selection (1) Initiator (with Arbitration)					
Item	Symbol	Min.	Typ.	Max.	Unit
Bus free→ $\overline{BSY}$ 'L'[1]	t_{BFBL}	(6+n) t_{CLF}		(7+n) t_{CLF}+80	ns
$\overline{BSY}$ 'L' - sends its own ID bit	t_{BLID}	10		60	ns
$\overline{BSY}$ 'L' → SEL 'L'	t_{BLSL}	$32t_{CLF}$ – 40		$32t_{CLF}$ + 30	ns
$\overline{SEL}$ 'L' → ID, $\overline{ATN}$ send	t_{SIDA}	$11t_{CLF}$ – 30		$11t_{CLF}$ + 60	ns
ID send → $\overline{BSY}$ 'H'	t_{IDBH}	$2t_{CLF}$ – 60		$2t_{CLF}$ + 30	ns
$\overline{BSY}$ 'L' → $\overline{SEL}$ 'H' ID hold	t_{BLSH}	$2t_{CLF}$		$3t_{CLF}$ + 120	ns

Note: 1 TCL register setting

Selection (2) Initiator (without Arbitration)

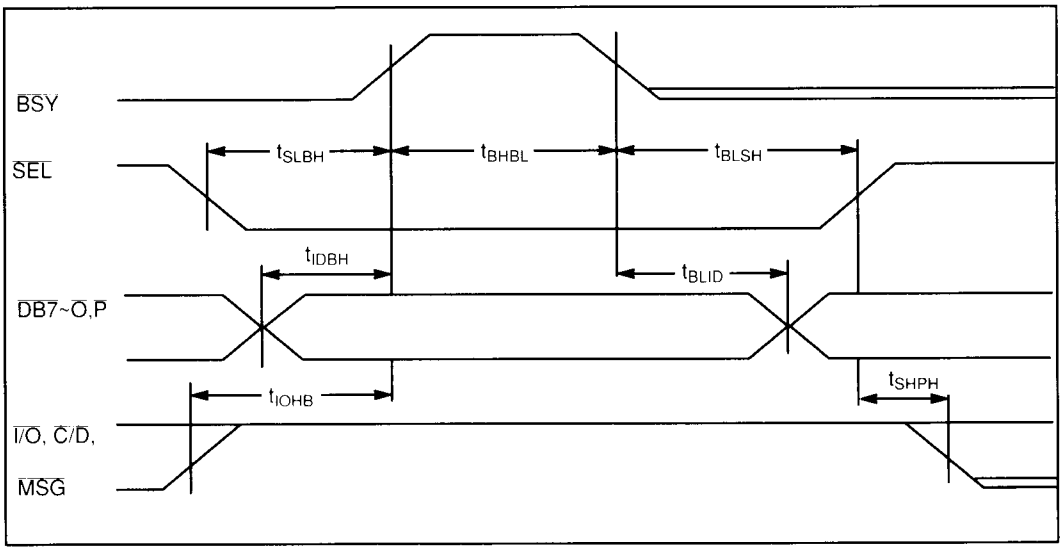


Selection (2) Initiator (without Arbitration)

Item	Symbol	Min.	Typ.	Max.	Unit
Bus free → ID send[1]	t_{FRID}	(6+n) t_{CLF}		(7+n) t_{CLF} + 100	ns
ID send → SEL 'L', ATN 'L'	t_{IDSL}	$11t_{CLF}$ – 60		$11t_{CLF}$ + 40	ns
BSY 'L'→ SEL 'H'. ID hold	t_{BLSH}	$2t_{CLF}$		$3t_{CLF}$ + 120	ns

Note: 1 :n = TCL register setting

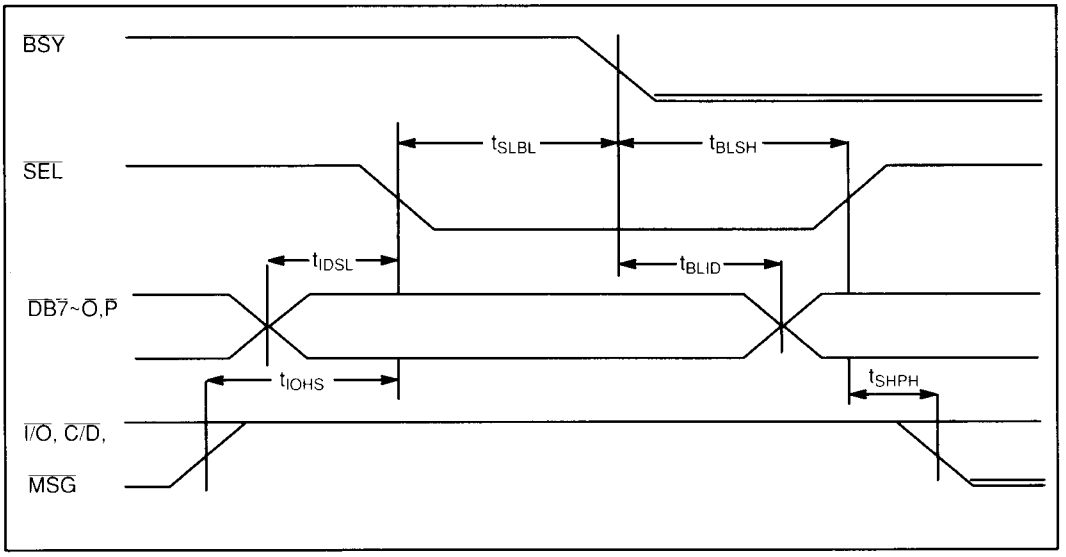
Selection (3) Target (with Arbitration)



Selection (3) Target (with Arbitration)

Item	Symbol	Min.	Typ.	Max.	Unit
SEL 'L' → BSY 'H'	t_{SLBH}	0			ns
ID confirmation → BSY 'H'	t_{IDBH}	0			ns
I/O 'H' → BSY 'H'	t_{IOHB}	0			ns
BSY 'H' → BSY 'L'	t_{BHBL}	$4t_{CLF}$		$5t_{CLF}$ + 80	ns
BSY 'L' → SEL 'H'	t_{BLSH}	0			ns
BSY 'L' → ID hold	t_{BLID}	30			ns
SEL 'H' phase signal output	t_{SHPH}	$3t_{CLF}$		$4t_{CLF}$ + 100	ns

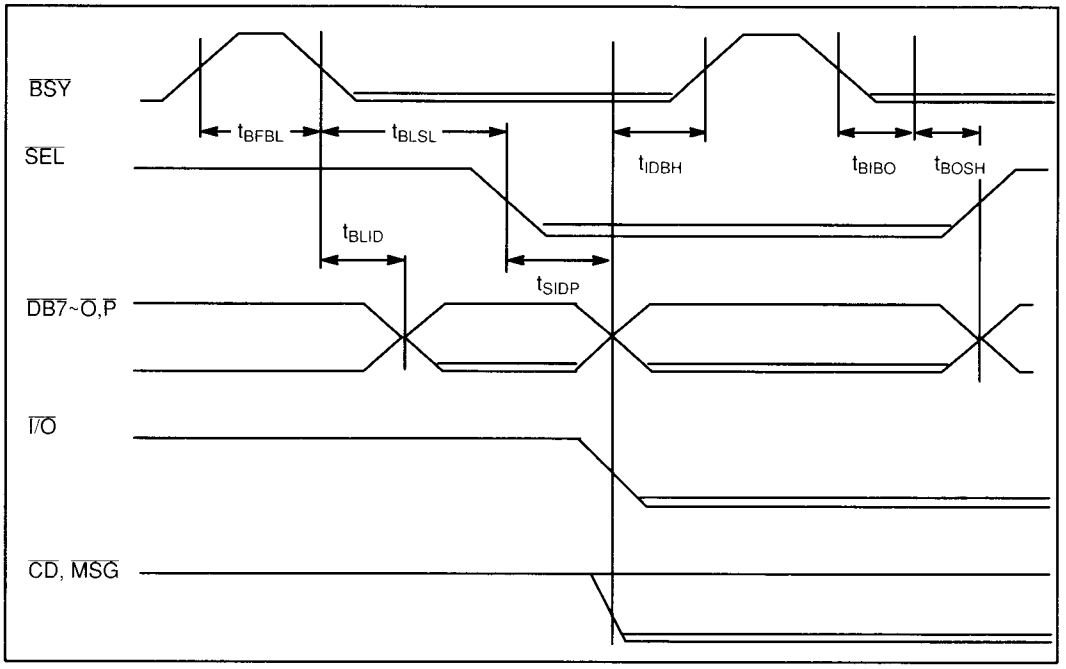
Selection (4) Target (without Arbitration)



Selection (4) Target (without Arbitration)

Item	Symbol	Min.	Typ.	Max.	Unit
ID confirmation → SEL 'L'	t_{IDSL}	0			ns
I/O 'H' → SEL 'L'	t_{IOHS}	0			ns
SEL 'L' → BSY 'L'	t_{SLBL}	$2t_{CLF}$		$3t_{CLF}$ + 100	ns
BSY 'L' → SEL 'H'	t_{BLSH}	0			ns
BSY 'L' → ID hold	t_{BLID}	30			ns
SEL 'H' → phase signal output	t_{SHPH}	$3t_{CLF}$		$4t_{CLF}$ + 100	ns

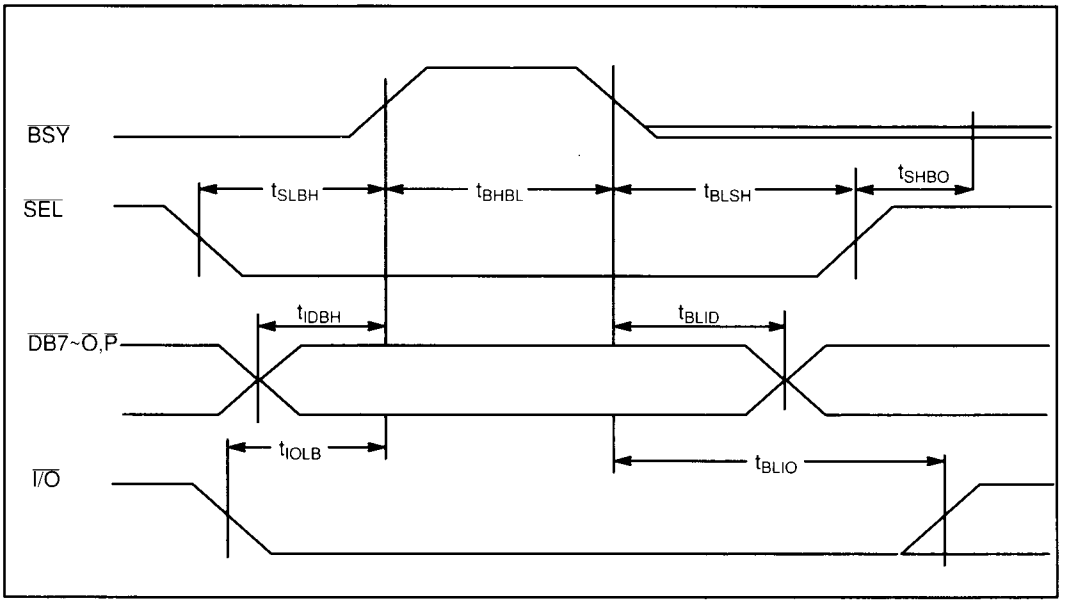
Reselection (1) Target



Reselection (1) Target					
Item	**Symbol**	**Min.**	**Typ.**	**Max.**	**Unit**
Bus free → BSY 'L' [1]	t_{BFBL}	(6+n) t_{CLF}		(7+n) t_{CLF} + 80	ns
BSY 'L' – sends its own ID bit	t_{BLID}	–10		60	ns
BSY 'L'→ SEL 'L'	t_{BLSL}	$32t_{CLF}$ – 40		$32t_{CLF}$ + 30	ns
SEL 'L' → ID, phase signal send	t_{SIDP}	$11t_{CLF}$ – 30		$11t_{CLF}$ + 60	ns
ID send → BSY 'H'	t_{IDBH}	$2t_{CLF}$ – 60		$2t_{CLF}$ + 30	ns
BSY 'L'→ BSY 'L' send	t_{BIBO}	$2t_{CLF}$		$3t_{CLF}$ + 90	ns
BSY 'L' send → SEL ID hold	t_{BOSH}	t_{CLF} – 20		t_{CLF} + 60	ns

Note: 1 n = TCL register setting

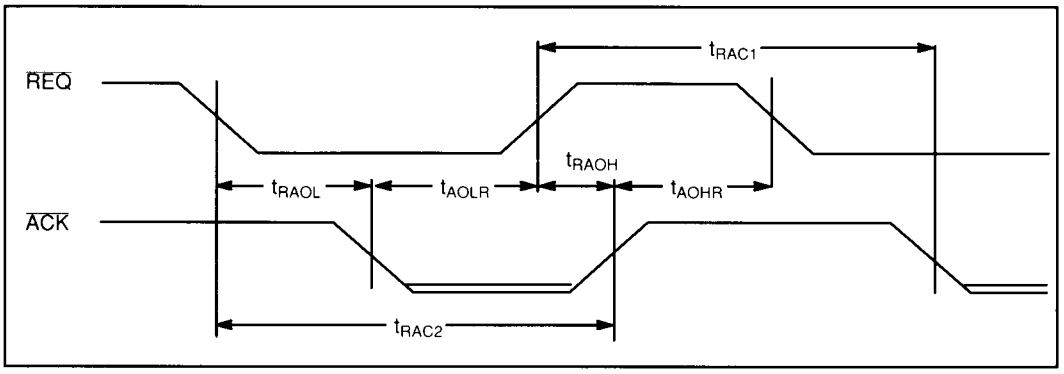
Reselection (2) Initiator



Reselection (2) Initiator

Item	Symbol	Min.	Typ.	Max.	Unit
SEL 'L' → BSY 'H'	t_{SLBH}	0			ns
ID confirmation → BSY 'H'	t_{IDBH}	0			ns
I/O 'L' → BSY 'H'	t_{IOLB}	0			ns
BSY 'H' → BSY 'L'	t_{BHBL}	$4t_{CLF}$		$5t_{CLF}$ + 80	ns
BSY 'L' → SEL 'H'	t_{BLSH}	0			ns
BSY 'L' → ID hold	t_{BLID}	30			ns
BSY 'L' → I/O signal hold	t_{BLIO}	20			ns
SEL 'H' → BSY 'L' send stop	t_{SHBO}	$2t_{CLF}$		$3t_{CLF}$ + 100	ns

Asynchronous Transfer Initiator (1) REQ-ACK Timing



Asynchronous Transfer Initiator (1) REQ-ACK Timing					
Item	**Symbol**	**Min.**	**Typ.**	**Max.**	**Unit**
$\overline{REQ}$ 'L' → $\overline{ACK}$ 'L'[3]	t_{RAOL}	15		90	ns
$\overline{ACK}$ 'L' → $\overline{REQ}$ 'H'	t_{AOLR}	0			ns
$\overline{REQ}$ 'H' → $\overline{ACK}$ 'H'[3]	t_{RAOH}	15		100	ns
$\overline{ACK}$ 'H' → $\overline{REQ}$ 'L'	t_{AOHR}	10			ns
$\overline{REQ}$ 'H' → $\overline{ACK}$ 'L'[1,3]	t_{RAC1}	$2t_{CLF}$		$3t_{CLF}$ + 120	ns
$\overline{REQ}$ 'L' → $\overline{ACK}$ 'H'[2,3]	t_{RAC2}	$2t_{CLF}$		$3t_{CLF}$ + 130	ns

Notes: [1]The time for $\overline{REQ}$ 'H' → $\overline{ACK}$'L' is determined by the longer of (t_{RAOH} + t_{AOHR} + t_{RAOL}) and t_{RAC1}.

[2]Apply for input operations. The time of $\overline{REQ}$'L' → $\overline{ACK}$'H' is determined by the longer of (t_{RAOL} + t_{AOLR} + t_{RAOH}) and t_{RAC1}.

[3]The times assigned in this section do not apply in the following cases:

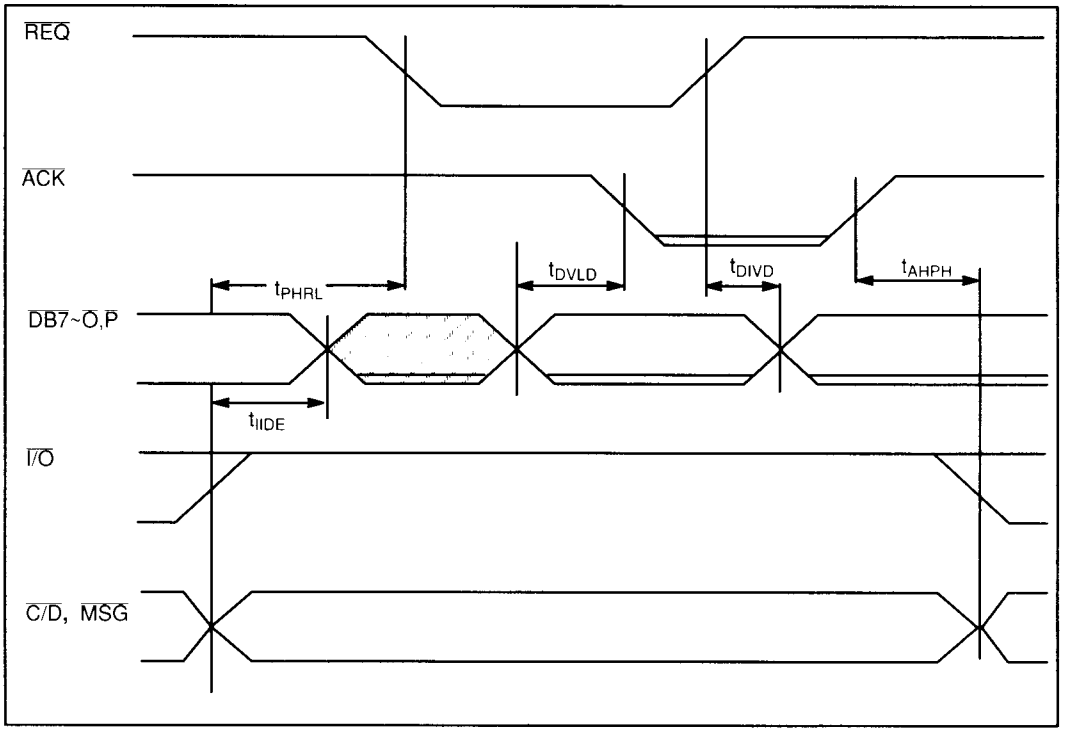
(1) For output operations, if the data buffer is empty.

(2) For input operations, if the data buffer is full.

(3) During transfer of the first or last byte.

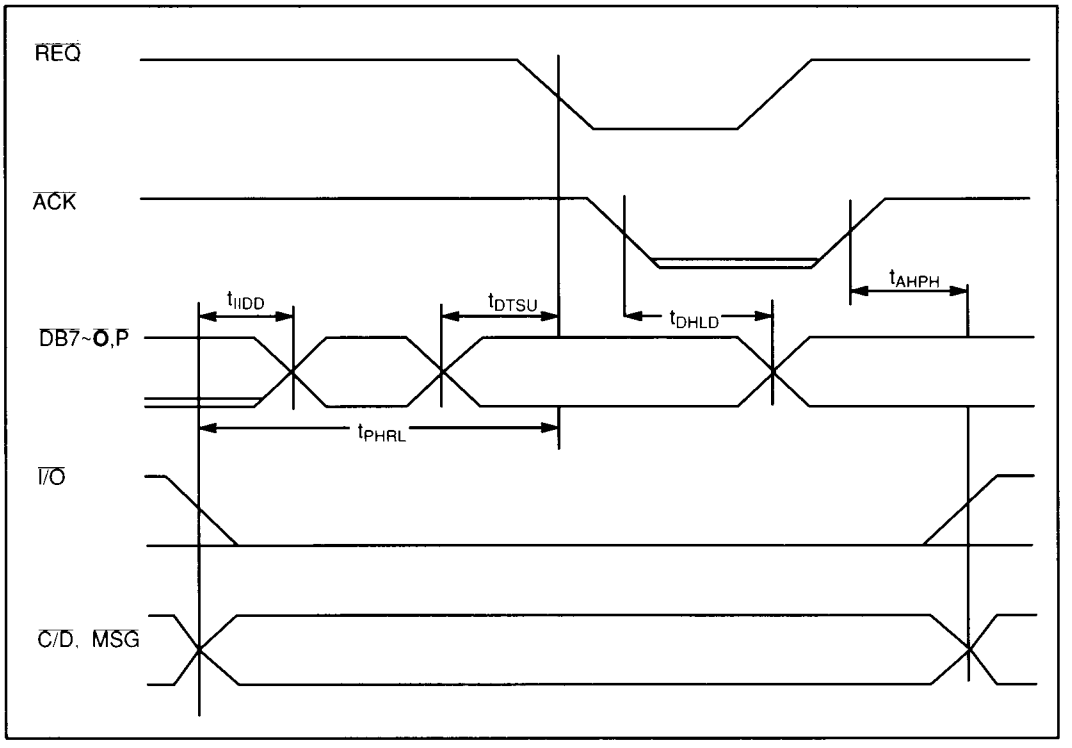
(4) During input operations, when the SPC automatically sends the $\overline{ATN}$ signal.

Asynchronous Transfer Initiator (2) Output Operation



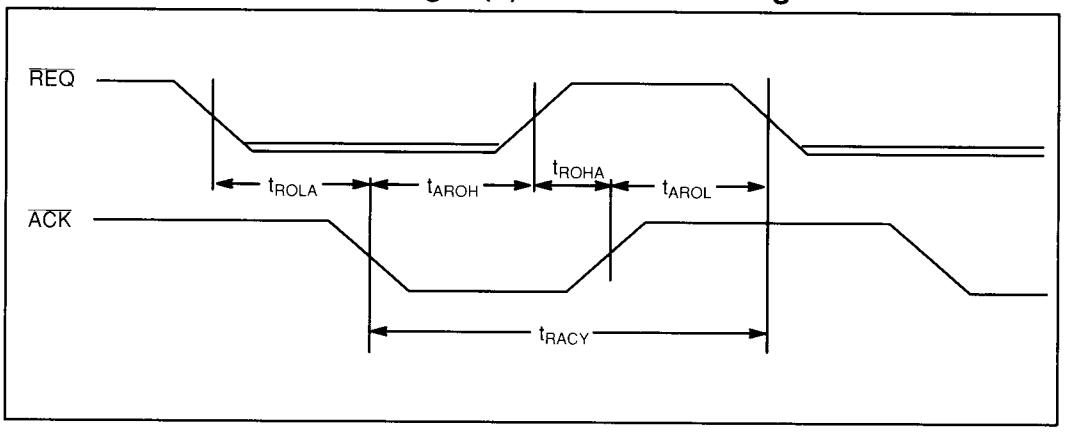
Asynchronous Transfer Initiator (2) Output Operation					
Item	**Symbol**	**Min.**	**Typ.**	**Max.**	**Unit**
I/O 'H' → data bus output	t_{IIDE}	10		110	ns
Phase designation → REQ 'L'	t_{PHRL}	100			ns
Data bus output confirmation → ACK 'L'	t_{DVLD}	$2t_{CLF}-80$			ns
REQ 'H' → data bus hold	t_{DIVD}	15			ns
ACK 'H' → phase change	t_{AHPH}	10			ns

Asynchronous Transfer Initiator (3) Input Operation



Asynchronous Transfer Initiator (3) Input Operation					
Item	Symbol	Min.	Typ.	Max.	Unit
I/O 'L' → data bus output stop	t_{IIDD}			110	ns
Phase designation → REQ 'L'	t_{PHRL}	100			ns
Data bus confirmation → REQ 'L'	t_{DTSU}	10			ns
ACK 'L' → data bus hold	t_{DHLD}	15			ns
ACK 'H' → phase change	t_{AHPH}	10			ns

Asynchronous Transfer Target (1) REQ-ACK Timing

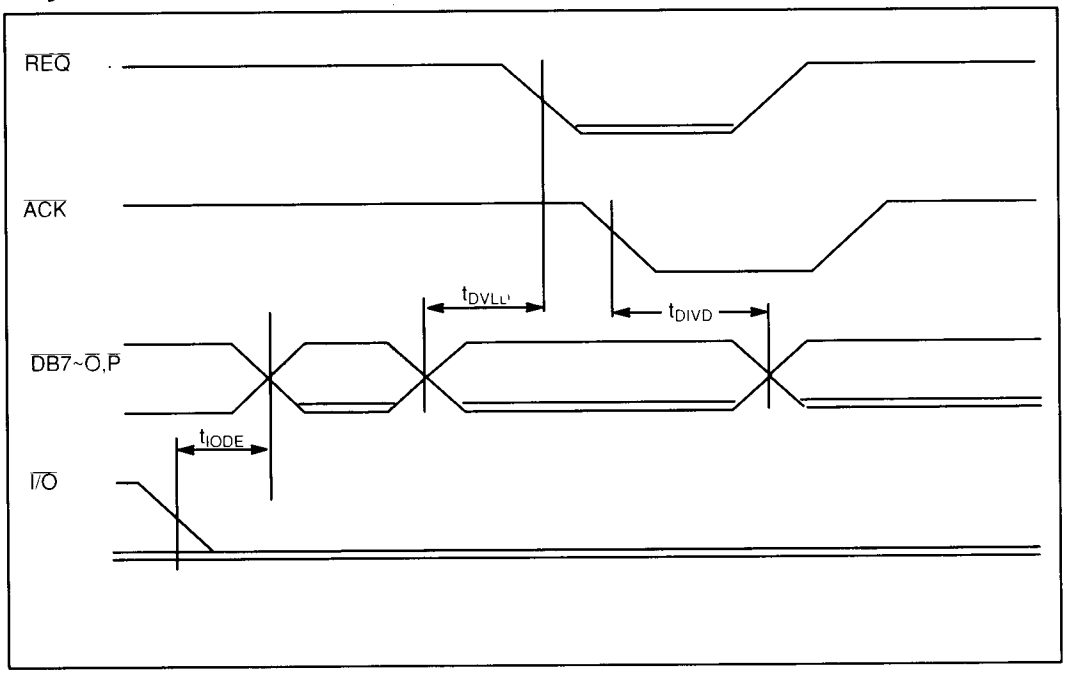


Asynchronous Transfer Target (1) REQ-ACK Timing

Item	Symbol	Min.	Typ.	Max.	Unit
$\overline{REQ}$ 'L' — $\overline{ACK}$ 'L'	t_{ROLA}	0			ns
$\overline{ACK}$ 'L' → $\overline{REQ}$ 'H'	t_{AROH}	10		90	ns
$\overline{REQ}$ 'H' → $\overline{ACK}$ 'H'	t_{ROHA}	0			ns
$\overline{ACK}$ 'H' → $\overline{REQ}$ 'L' *2	t_{AROL}	10		70	ns
$\overline{ACK}$ 'H' → $\overline{REQ}$ 'L' *1, *2	t_{RACY}	$2t_{CLF}$		$3t_{CLF}$ + 110	ns

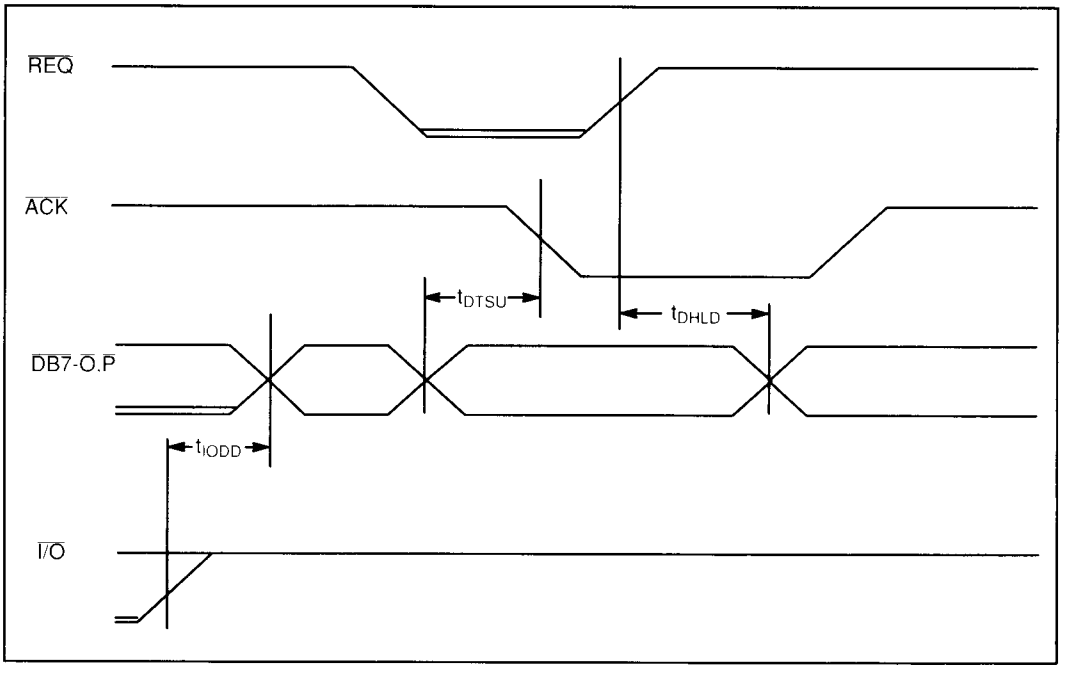
Notes: 1 The time for $\overline{ACK}$ 'L' → $\overline{REQ}$ 'L' is determined by the longer of (t_{AROH} + t_{ROHA} + t_{AROL}) and t_{RACY}.
2 The times assigned in this section do not apply to the following:
(1) For output operations, if the data buffer is empty.
(2) For input operations, if the data buffer is full.

Asynchronous Transfer (2) Output Operation



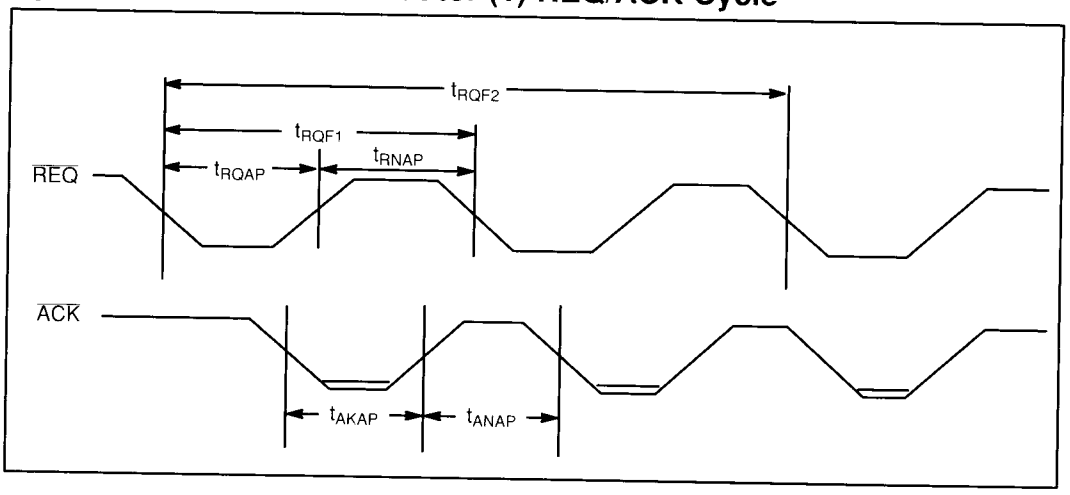
Asynchronous Transfer (2) Output Operation					
Item	**Symbol**	**Min.**	**Typ.**	**Max.**	**Unit**
$\overline{I/O}$ 'L' → data bus output	t_{IODE}	$7t_{CLF}$		$8t_{CLF}$ + 110	ns
Data bus output confirmation → $\overline{REQ}$ 'L'	t_{DVLD}	$2t_{CLF}$ - 80			ns
ACK 'L' → data bus hold	t_{DIVD}	15			ns

Asynchronous Transfer Target (3) Input Operation



Asynchronous Transfer Target (3) Input Operation					
Item	Symbol	Min.	Typ.	Max.	Unit
I/O 'H' → data bus output stop	t_{IODD}			60	ns
Data bus confirmation → ACK 'L'	t_{DTSU}	10			ns
REQ 'H' → data hold	t_{DHLD}	15			ns

Synchronous Transfer Initiator (1) REQ/ACK Cycle

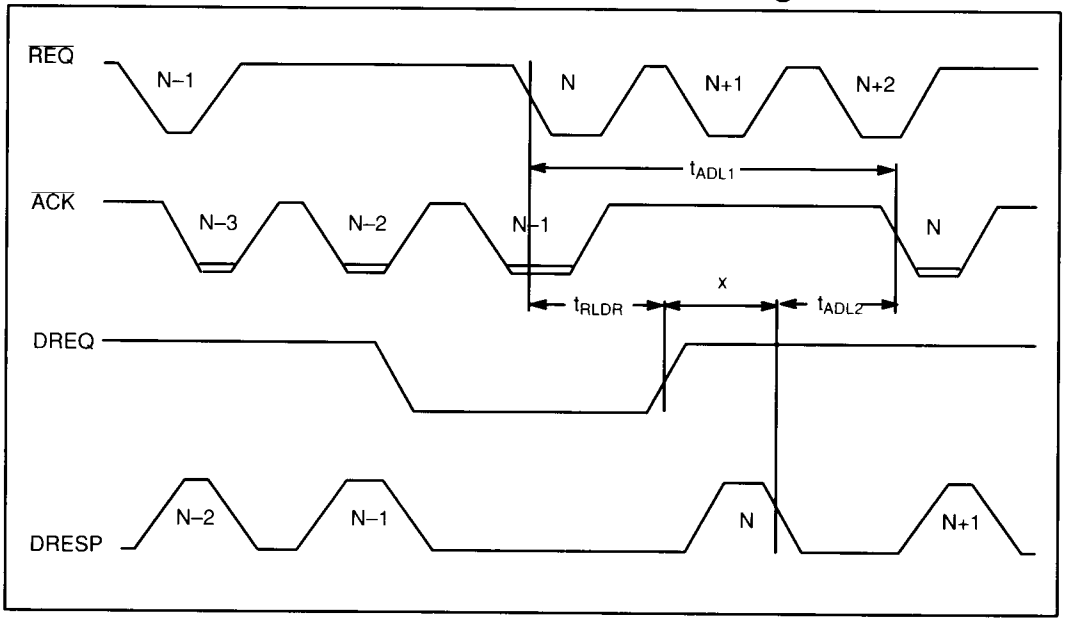


Synchronous Transfer Initiator (1) REQ/ACK Cycle					
Item	**Symbol**	**Min.**	**Typ.**	**Max.**	**Unit**
$\overline{REQ}$ Assertion Period	t_{RQAP}	50			ns
$\overline{REQ}$ Nonassertion Period	t_{RNAP}	50			ns
$\overline{REQ}$ cycle time	t_{RQF1}	t_{CLF}			ns
$\overline{REQ}$ cycle time	t_{RQF2}	$3t_{CLF}$			ns
$\overline{ACK}$ Assertion Period	t_{AKAP}	t_{CLF} - 10			ns
ACK Nonassertion Period[1]	t_{ANAP}	$n.t_{CLF}$ - 30			ns

Note: 1 n depends on the TMOD register setting.

TMOD Register		
Bit 3	**Bit 2**	**n**
0	0	1
0	1	2
1	0	3
1	1	4

Synchronous Transfer Initiator (2) REQ/ACK Timing

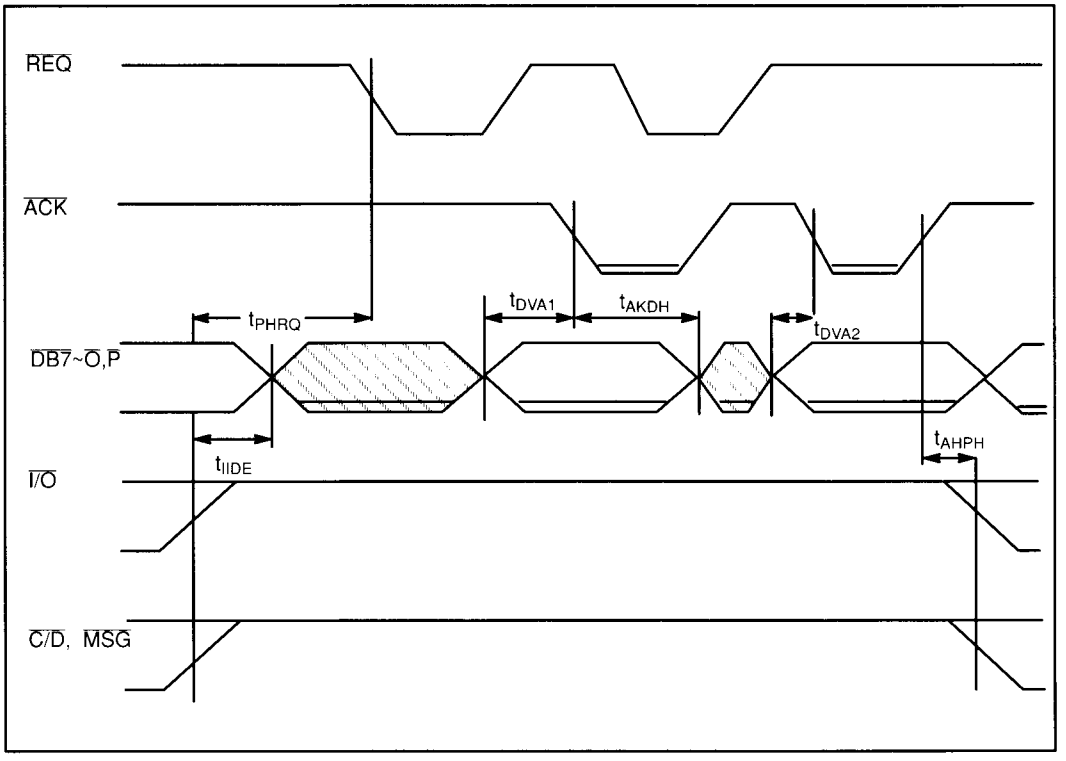


Synchronous Transfer Initiator (2) REQ/ACK Timing					
Item	**Symbol**	**Min.**	**Typ.**	**Max.**	**Unit**
$\overline{ACK}$ Assertion delay time[1]	t_{ADL1}	$3t_{CLF}$		$4t_{CLF} + 100$	ns
$\overline{REQ}$ 'L' " DREQ 'H'[2]	t_{RLDR}	$t_{CLF} + 50$		$3t_{CLF} + 60$	ns
$\overline{ACK}$ Assertion delay time [2,3]	t_{ADL2}	$3t_{CLF}$		$4t_{CLF} + 120$	ns

Notes: [1]Apply to output operations and to input operations when the maximum offset value is 4 or less.
[2]Apply to input operations.
[3]Apply to input operations when the maximum offset value is 5.8.

This is the minimum time after receiving the DRESP of byte N, until the ACK of byte N is transferred. In this case, the minimum time required from receiving the REQ of byte N until transferring the ACK of byte N is t_{RLDR} + (DRESP assertion time x) + t_{ALD2} .

Synchronous Transfer Initiator (3) Output Operation

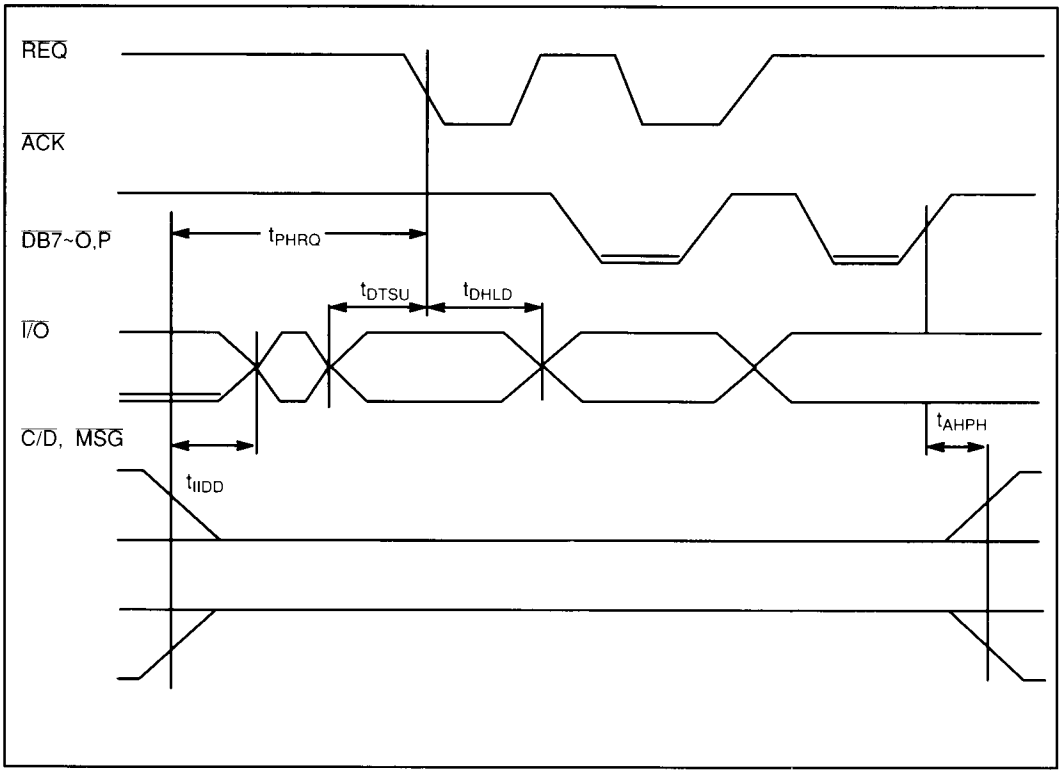


Synchronous Transfer Initiator (3) Output Operation (Continued)					
Item	**Symbol**	**Min.**	**Typ.**	**Max.**	**Unit**
$\overline{I/O}$ 'H' → data bus output	t_{IIDE}	10		110	ns
Phase designation → $\overline{REQ}$ 'L'	t_{PHRQ}	100			ns
Data bus output[1]	t_{DVA1}	$2t_{CLF}$ - 70			ns
confirmation → $\overline{ACK}$ 'L'[2]	t_{DVA2}	$n.t_{CLF}$ - 60			
$\overline{ACK}$ 'L' → data bus hold	t_{AKDH}	t_{CLF} - 20			ns
$\overline{ACK}$ 'H' → phase change	t_{AHPH}	10			ns

Notes: 1 n depends on the TMOD register setting.
2 The time from data bus output confirmation to $\overline{ACK}$ 'L' is set by the shorter of t_{DVA1} and t_{DVA2}.

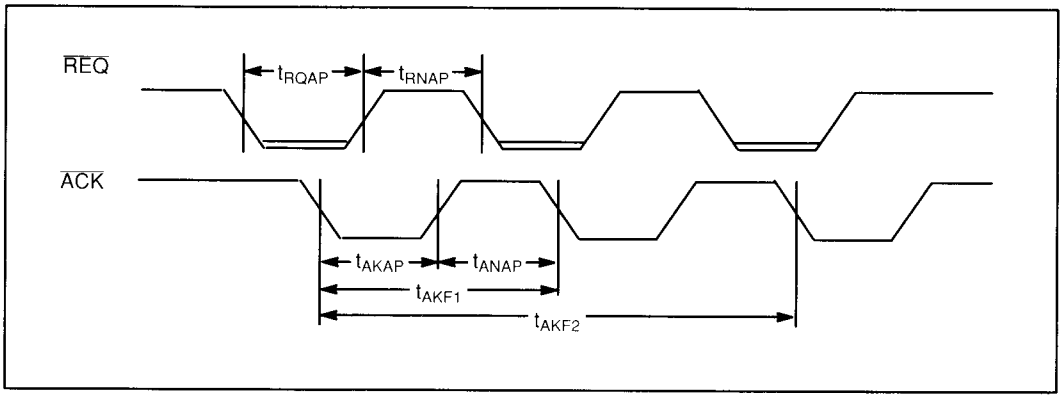
TMOD Register		
Bit 3	**Bit 2**	**n**
0	0	1
0	1	2
1	0	3
1	1	4

Synchronous Transfer Initiator (4) Input Operation



Synchronous Transfer Initiator (4) Input Operation					
Item	**Symbol**	**Min.**	**Typ.**	**Max.**	**Unit**
$\overline{I/O}$ 'H' → data bus output stop	t_{IIDD}			110	ns
Phase designation → $\overline{REQ}$'L'	t_{PHRQ}	100			ns
Data bus confirmation → $\overline{REQ}$'L'	t_{DTSU}	10			ns
$\overline{ACK}$ 'L' → data bus hold	t_{DHLD}	40			ns
$\overline{ACK}$ 'H' → phase change	t_{AHPH}	10			ns

Synchronous Transmission Target (1) REQ/ACK Synchronization

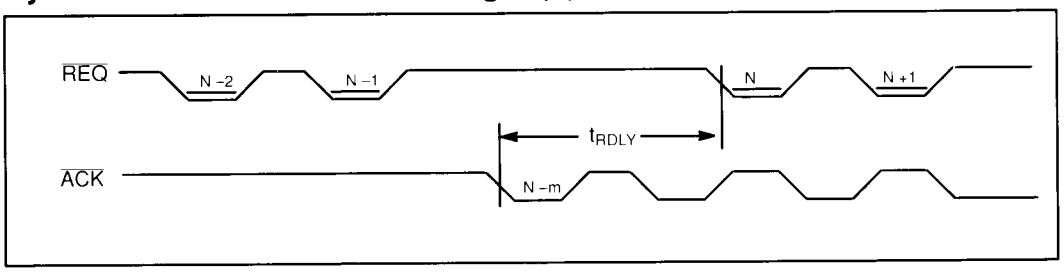


Synchronous Transmission Target (1) REQ/ACK Synchronization					
Item	Symbol	Min.	Typ.	Max.	Unit
REQ Assertion Period	t_{RQAP}	t_{CLF} –10			ns
REQ Non Assertion Period	t_{RNAP}	nt_{CLF} –30			
ACK Assertion Period	t_{AKAP}	50			
ACK Non Assertion Period	t_{ANAP}	50			
ACK Cycle Time (1)	t_{AKF1}	t_{CLF}			
ACK Cycle Time (2)	t_{AKF2}	$3t_{CLF}$			

n is set by the TMOD register.

TMOD Register		
Bit 3	Bit 2	n
0	0	1
0	1	2
1	0	3
1	1	4

Synchronous Transmission Target (2) REQ/ACK Timing

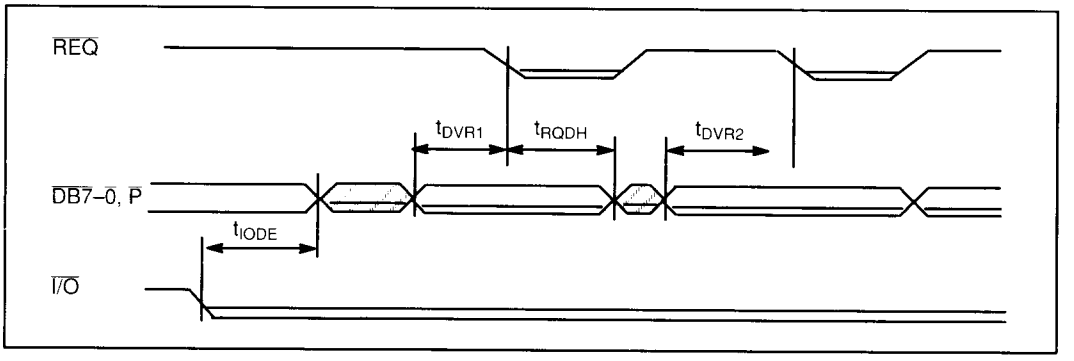


Synchronous Transmission Target (2) REQ/ACK Timing

Item	Symbol	Min.	Typ.	Max.	Unit
$\overline{REQ}$ Propagation delay time (skew)[1]	t_{RDLY}	$3t_{CLF}$		$4t_{CLF}+100$	ns

Note: [1] Minimum time required when the maximum offset value is set to m(m = 1 to 8) from receiving $\overline{ACK}$ signal for byte N–m to transmitting the $\overline{REQ}$ signal for byte N. The above timing diagram shows the case where the result of sending $\overline{REQ}$ for byte N–1 and the offset amount, namely the number of the preceding $\overline{REQ}$ transmitted, continues up to the maximum offset value of m after which $\overline{REQ}$ is deasserted.

Synchronous Transmission Target (3) Output Operation



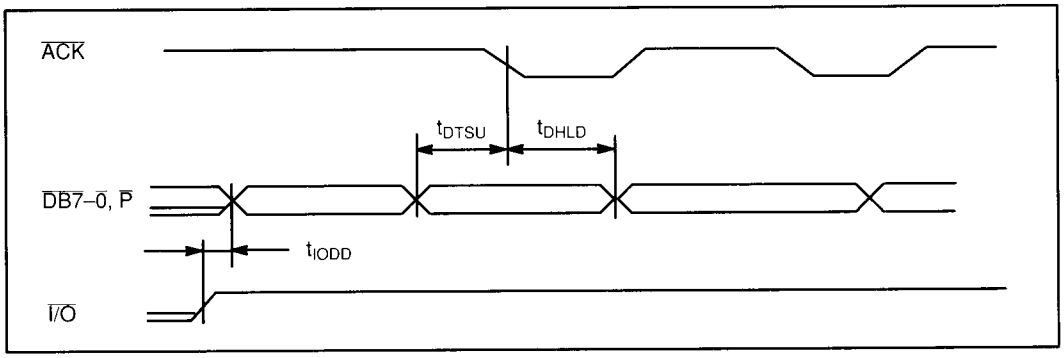
Synchronous Transmission Target (3) Output Operation					
Item	**Symbol**	**Min.**	**Typ.**	**Max.**	**Unit**
I/O "L" → data bus output	t_{IODE}	$7t_{CLF}$		$8t_{CLF}+110$	ns
Data bus output settles	t_{DVR1}	$2t_{CLF}-70$		—	
→ REQ "L"[1,2]	t_{DVR2}	$nt_{CLF}-60$		—	
I/O "L" → data bus hold	t_{RQDH}	$t_{CLF}-20$		—	

Notes: [1] n is set by the TMOD register.
[2] The time from data bus output setting to ACK going 'L' is the shorter of the time t_{DVA1} and t_{DVA2}.

TMOD Register

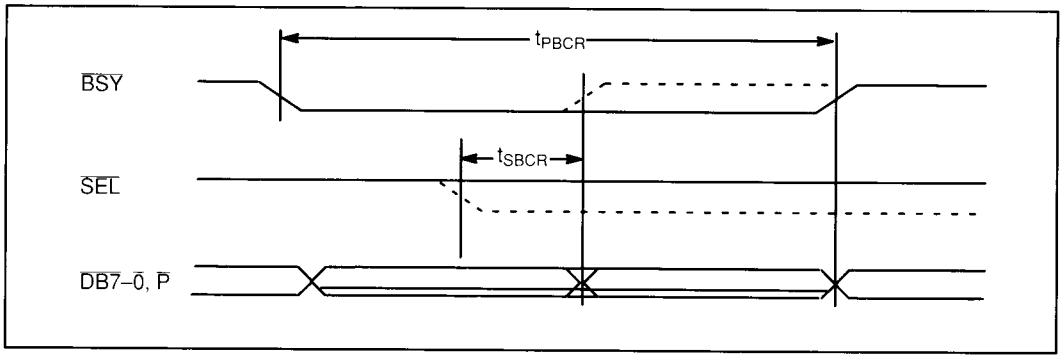
Bit 3	Bit 2	n
0	0	1
0	1	2
1	0	3
1	1	4

Synchronous Transmission Target (4) Input Operation



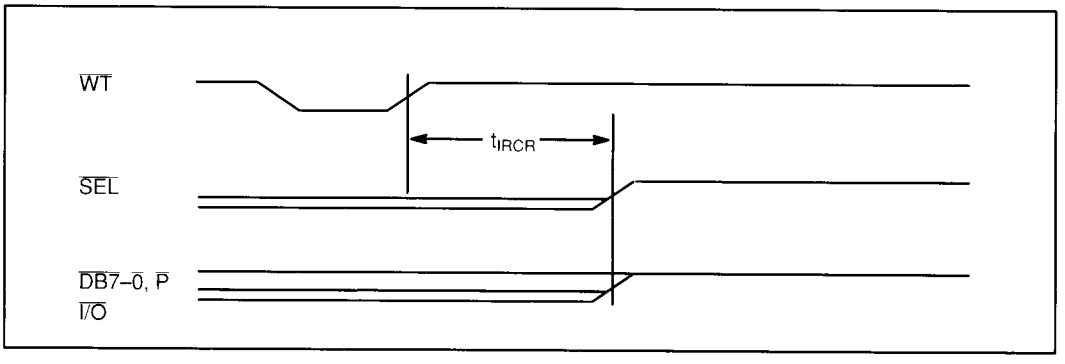
Synchronous Transmission Target (4) Input Operation					
Item	**Symbol**	**Min.**	**Typ.**	**Max.**	**Unit**
I/O "H" → data bus output disabled	t_{IODD}	—		60	ns
Data bus output settles → ACK "L"	t_{DTSU}	10		—	
ACK "L" → data bus hold	t_{DHLD}	40		—	

Bus Free (1) Arbitration Failure



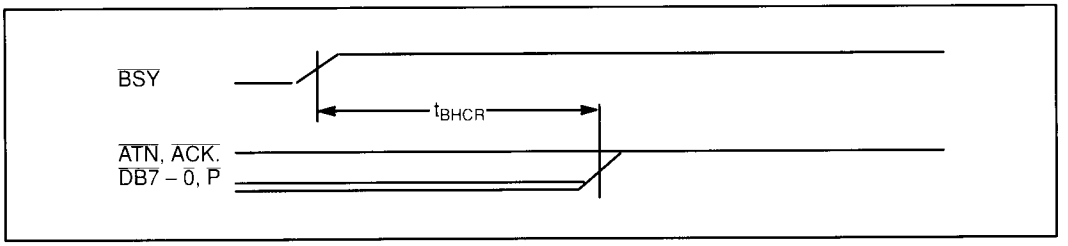
Bus Free (1) Arbitration Failure					
Item	Symbol	Min.	Typ.	Max.	Unit
Arbitration start → BSY "H" and ID bit transmission stops[1]	t_{PBCR}	$32t_{CLF}$–30		$32t_{CLF}$+60	ns
SEL "L" by other bus devices → BSY "H" and ID bit transmission stops[1]	t_{SBCR}	$2t_{CLF}$		$32t_{CLF}$+130	

Bus Free (2) Selection/Reselection Timeout



Bus Free (2) Selection/Reselection Timeout					
Item	Symbol	Min.	Typ.	Max.	Unit
Timeout Interrupt set → SEL "H" and bus cleared	t_{IRCR}	—	$3t_{CLF}$+130		ns

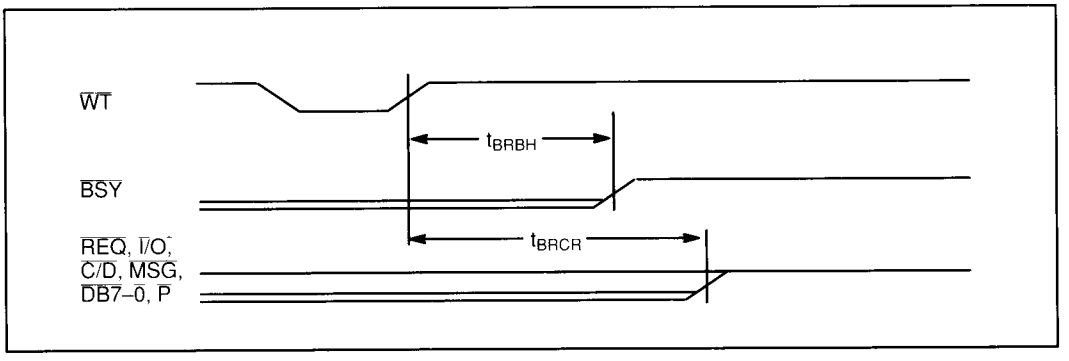
Bus Free (3) Enable



Bus Free (3) Enable

Item	Symbol	Min.	Typ.	Max.	Unit
BSY "H" → bus cleared	t_{BHCR}	—		$5t_{CLF}+120$	ns

Bus Free (4) Target



Bus Free (4) Target

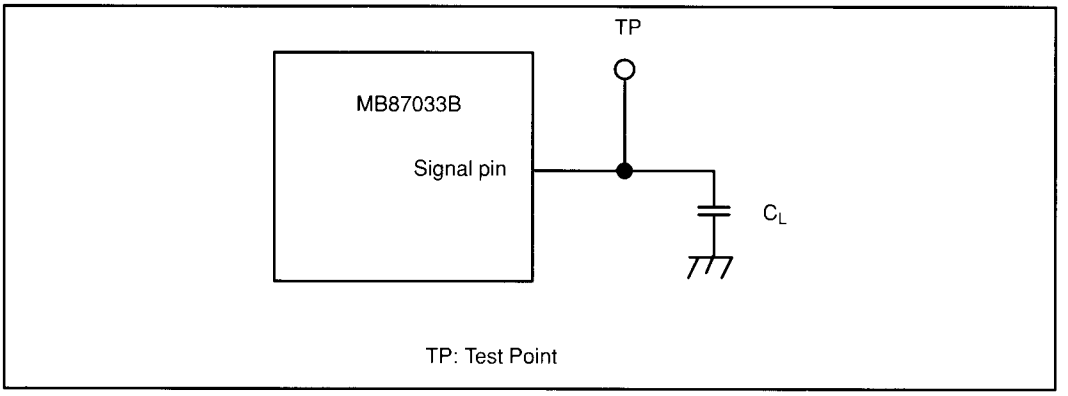
Item	Symbol	Min.	Typ.	Max.	Unit
Bus release command Issued → BSY "H"	t_{BRBH}	—	$3t_{CLF}+100$		ns
Bus release command Issued → bus cleared	t_{BRCR}		$3t_{CLF}+130$		

AC Characteristics

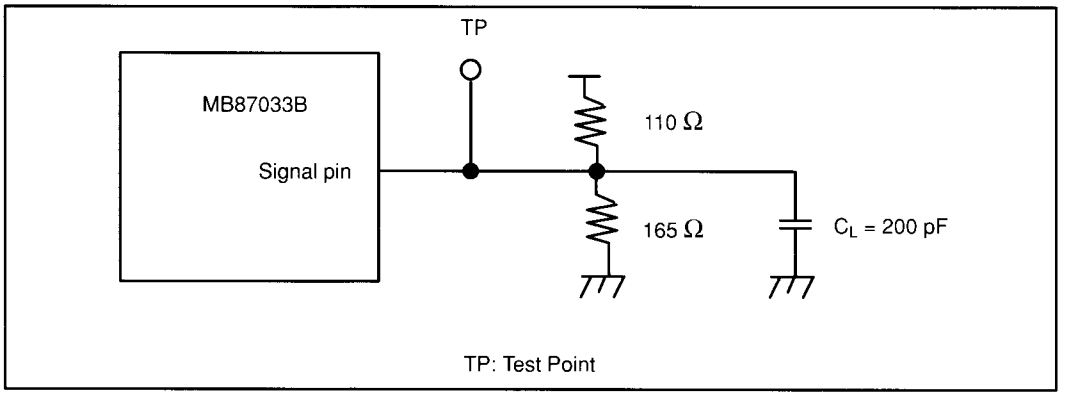
T_A = 0 to 70°C, V_{DD} = +5 V ±5%, V_{SS} = 0 V

Non-SCSI Pins

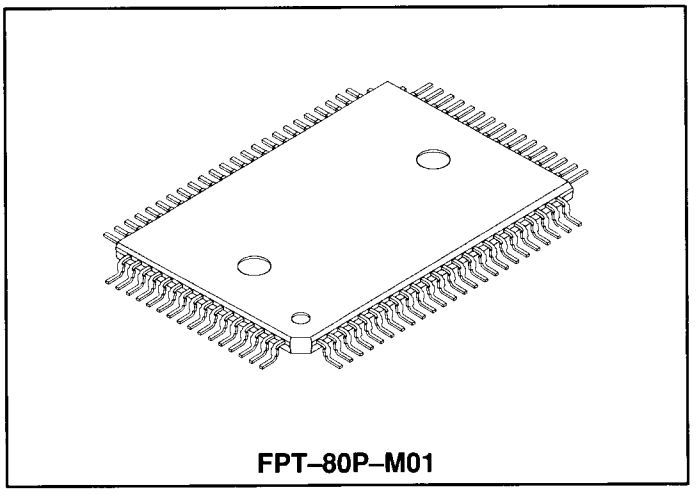
Pin Name	C_L	Unit
INTR, INT2, DREQ	60	pF
DPO	65	
D7 – D0, DP, HDB7 – O, HDBP	85	



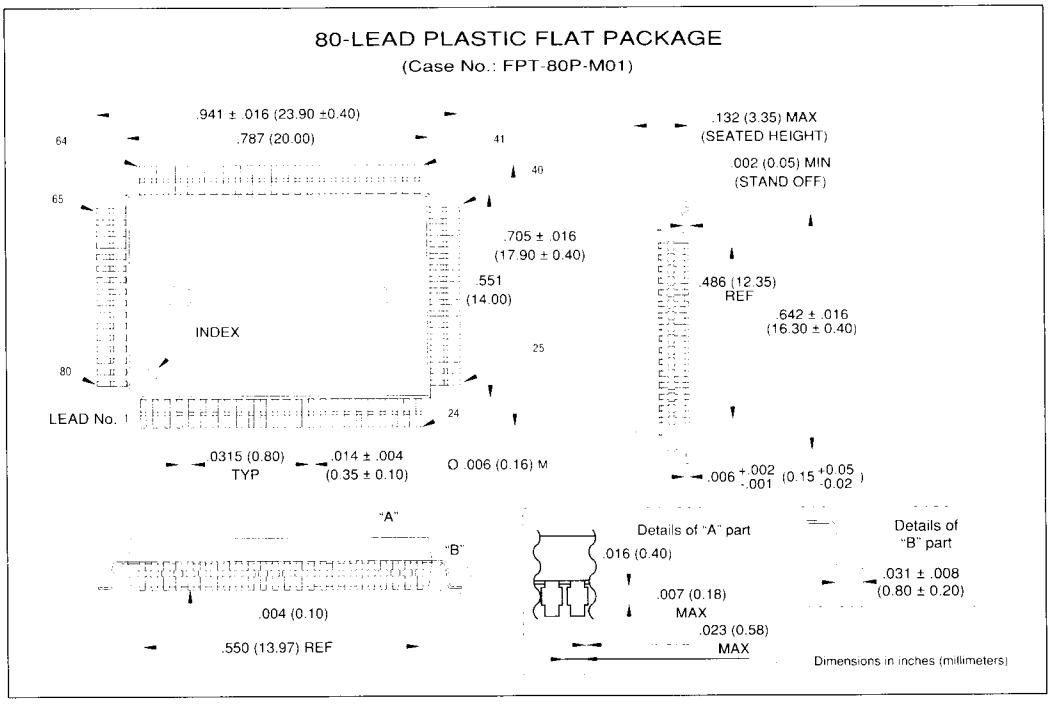
SCSI Pins



PACKAGE DIMENSIONS

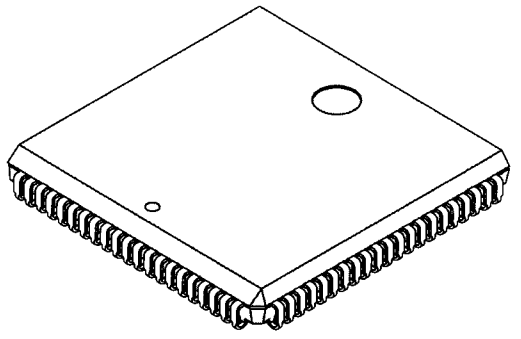


FPT–80P–M01



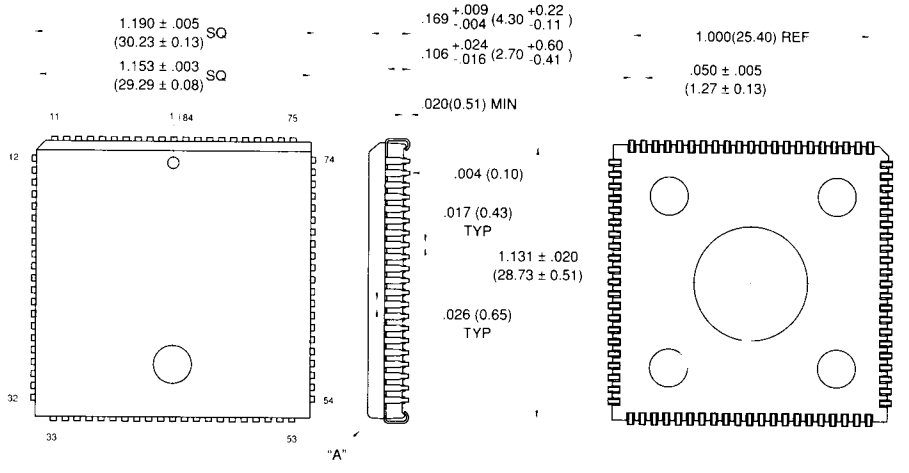
PACKAGE DIMENSIONS

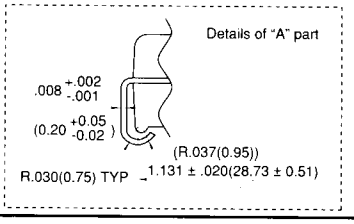
84–Lead Plastic Leaded Chip Carrier



LCC–84P–M01

84-LEAD PLASTIC LEADED CHIP CARRIER
(CASE NO.: LCC–84P–M01)





No.: LEAD No.
Dimensions in inches
(millimeters)