MB86703

PLUG AND PLAY ISA CONTROLLER

FUJITSU

DATA SHEET

MARCH 1996

FEATURES

- Provides Plug and Play compatibility for ISA add-in cards
- Conforms to Plug and Play ISA specification v1.0a
- Provides interface to serial EEPROM with read and write capability for storage of card and resource requirements descriptors, default setup parameters and user-defined data
- Auto-configuration and optional activation at power-up using default parameters stored in EEPROM allows use of card in non-PnP environment or where otherwise required
- Configurable to support 1, 2 or 4 logical devices
- Supports the following resources
  - Four interrupt inputs with programmable polarity steered to any four of eight interrupt channels on the ISA bus
  - Four I/O mapped chip select outputs, f{A0-A15}
  - Two memory mapped chip select outputs, f{A0-A23}, *or* two device DMA channels steered to any two of five DMA channels on the ISA bus
- Generates /IOCS16 and /MEMCS16 control signals
- Can be used in non-Plug and Play environment
- 5 volt power supply
- 80-pin, 14mm x 20mm, 0.8mm lead pitch plastic quad flat package

BENEFITS

- Single chip configurable for a wide range of applications
- Enables rapid time to market for Plug and Play products
  - Don't have to wait until an ASSP with integrated PnP is available
  - Don't have to respin a proprietary ASIC to incorporate PnP capability
- Adds Plug and Play functionality to existing board designs with a minimum of hardware and software re-engineering
- Reduces costs of customer support by reducing or totally eliminating installation-related problems
- Eliminates jumpers, switches and corresponding decoding logic
- Eliminates the need for special hardware and software related to proprietary schemes for software configuration

GENERAL DESCRIPTION

The MB86703 Plug and Play ISA Controller (PPIC) is a single-chip solution offering all the hardware resources required to build ISA cards compliant with the Plug and Play ISA Specification v1.0a. An external serial EEPROM stores card resource requirements information and can also store additional user-defined data, such as an Ethernet ID or manufacturing traceability information. Configuration information provided by the Plug and Play software is stored in registers as defined in the specification. The MB86703 performs all I/O and memory address decoding as well as interrupt and DMA request routing. Stored configuration information is decoded to properly route interrupt and DMA requests. Users may direct card DMA to any of five DMA channels on the ISA bus and interrupts to any of eight interrupt channels on the ISA bus.

The MB86703 operates in two basic modes:

- DMA Mode: In this mode the device supports interrupts, I/O chip selects and DMA requests
- MEMORY Mode: In this mode the device supports interrupts and I/O and memory chip selects

Within each basic mode there are four submodes, designated as submodes 0, 1, 2 and 3, supporting 1, 2, 2 and 4 logical devices respectively. In each submode, the supported resources are allocated amongst the available logical devices as detailed later in this document.

The MB86703 is fabricated using a low-power CMOS process and is available in an 80-pin plastic quad flat package.

SUMMARY OF BASIC CAPABILITIES

RESOURCE	CAPABILITIES
Logical Devices	1, 2 or 4
Interrupts	
Number	4
Levels Supported	3, 4, 5, 7, 10, 11, 12, 15
DMA Channels*	
Number	2
Levels Supported	0, 3, 5, 6, 7
I/O Chip Selects	
Number	4
Address Decode	16 bits
Window Size	2, 4, 8, 16, 32, 64 or 128 bytes
Base Address	Any multiple of the window size
Memory Chip Selects*	
Number	2
Decode	24 bits
Window Size	Specified as upper limit
Base Address	Any multiple of 256 bytes

* The MB86703 supports either two memory chip select outputs or two device DMA channels depending on mode

PIN ASSIGNMENT

PIN NO.	PIN NAME (1)	TYPE (1, 2)	OTHER (3)
1	GND	-	-
2	/MEMCS16{DREQ7}	O 24	Note 4
3	/IOCS16	O 8	OD
4	SA0	I	-
5	SA1	I	-
6	SA2	I	-
7	SA3	I	-
8	SA4	I	-
9	SA5	I	-
10	SA6	I	-
11	SA7	I	-
12	SA8	I	-
13	SA9	I	-
14	SA10	I	-
15	SA11	I	-
16	SA12	I	-
17	SA13	I	-
18	SA14	I	-
19	SA15	I	-
20	VDD	-	-
21	GND	-	-
22	IOCHRDY	O 24	OD
23	/IOCSA	O 4	-
24	/IOCSB	O 4	-
25	/IOCSC	O 4	-
26	/IOCSD	O 4	-
27	/MCSA{DRQA}	O 4 {I}	PD
28	/REFRESH{DRQB}	I	PD
29	/MCSB{/DACKA}	O 4	-
30	GND	-	-
31	CLK	I	-
32	NC{/DACKB}	{O 4}	-
33	/IOR	I	-
34	/IOW	I	-
35	AEN	I	-
36	RESET_DRV	I	PD
37	/RESET	O 4	-
38	RDY	I	-
39	INTA	I	PD
40	VDD	-	-

PIN NO.	PIN NAME (1)	TYPE (1, 2)	OTHER (3)
41	GND	-	-
42	INTB	I	PD
43	INTC	I	PD
44	INTD	I	PD
45	IRQ7	O 12	-
46	IRQ5	O 12	-
47	IRQ4	O 12	-
48	IRQ3	O 12	-
49	IRQ10	O 12	-
50	IRQ11	O 12	-
51	IRQ12	O 12	-
52	IRQ15	O 12	-
53	ACTENA	I	PU
54	SD0	I/O 24	-
55	SD1	I/O 24	-
56	GND	-	-
57	SD2	I/O 24	-
58	SD3	I/O 24	-
59	SD4	I/O 24	-
60	VDD	-	-
61	GND	-	-
62	SD5	I/O 24	-
63	SD6	I/O 24	-
64	SD7	I/O 24	-
65	GND	-	-
66	SK	O 4	-
67	EEPCS	O 4	-
68	DI	O 4	-
69	DO	I	PU
70	VDD	-	-
71	BALE{/DACK7}	I	-
72	GND	-	-
73	LA17{DREQ0}	I {O 24}	-
74	LA18{/DACK0}	I	-
75	LA19{DREQ3}	I {O 24}	-
76	LA20{/DACK3}	I	-
77	LA21{DREQ5}	I {O 24}	-
78	LA22{/DACK5}	I	-
79	LA23{DREQ6}	I {O 24}	-
80	SA16{/DACK6}	I	-

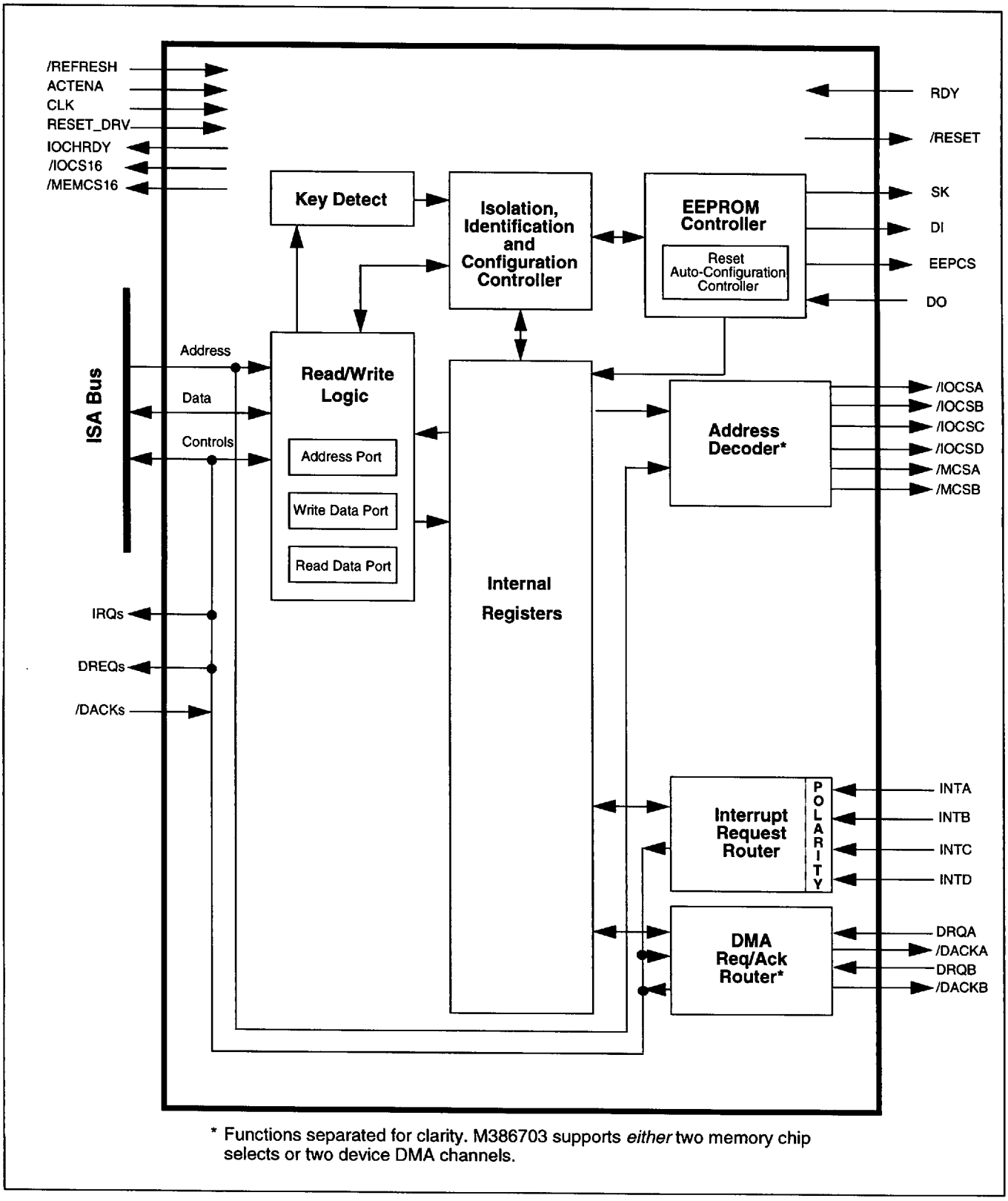
NOTES

(1) Pin names enclosed in brackets indicate pin function in DMA mode. If not in brackets the function is the same in both modes.
(2) Numeric suffix indicates output current sink capability. See DC Characteristics section.
(3) PU indicates input pull-up. PD indicates input pull-down. OD indicates open-drain output.
(4) Open drain output in MEMORY mode.

ORDERING CODE

PACKAGE STYLE	V_{CC} = +5V 5%, T_A = 0 to + 70°C
80-pin Plastic Flat Package	MB86703PF

BLOCK DIAGRAM



* Functions separated for clarity. M386703 supports *either* two memory chip selects or two device DMA channels.

LOGIC CONVENTION

Unless otherwise noted, a positive logic (active high) convention is assumed throughout this document, whereby the presence at a pin of a higher, more positive voltage (nominally 5VDC) causes assertion of the signal. A preceding slash, e.g., /RESET, indicates that the signal is asserted in a low state (nominally 0 volts). Whenever a signal is separated into numbered bits, e.g., SD7, SD6, ..., SD0, the family of bits may also be shown collectively, e.g., as SD<7:0>.

Some pins have different functions in MEMORY mode and in DMA mode. For those pins, the function in DMA mode is enclosed in brackets. Dual function pins are categorized based on their function in MEMORY mode in the tables below.

SIGNAL DESCRIPTIONS

ISA Bus Interface Signals

PIN NUMBER	SYMBOL	TYPE	DESCRIPTION
36	RESET_DRV	I	**CHIP RESET**: Resets the chip and initializes internal registers and logic. When this signal is asserted, the MB86703 enters the *Wait for Key* state.
19-4	SA<15:0>	I	**SYSTEM ADDRESS**: Inputs are connected to the corresponding signals from the system bus.
80	SA16{/DACK6}	I	**SYSTEM ADDRESS 16{DMA ACKNOWLEDGE 6}:** In MEMORY mode, an address input connected to the corresponding signal from the ISA bus. In DMA mode, an active low signal from the ISA bus indicating that a DMA acknowledge cycle is in progress.
73 75 77 79	LA17{DREQ0} LA19{DREQ3} LA21{DREQ5} LA23{DREQ6}	I {O }	**LATCHED ADDRESS{DMA REQUEST}:** In MEMORY mode, address inputs connected to the corresponding signal from the ISA bus. In DMA mode, outputs indicating that the peripheral device is ready to transfer data. Used for both read and write operations. Pins not configured as outputs are maintained in the three-state condition.
74 76 78	LA18{/DACK0} LA20{/DACK3} LA22{/DACK5}	I	**LATCHED ADDRESS{DMA ACKNOWLEDGE}:** In MEMORY mode, address inputs connected to the corresponding signals from the ISA bus. In DMA mode, active low signals from the ISA bus indicating that a DMA acknowledge cycle is in progress.
71	BALE{/DACK7}	I	**BUS ADDRESS LATCH ENABLE{DMA ACKNOWLEDGE 7}:** In MEMORY mode, an active high input signal driven by the platform CPU to indicate when the address and AEN signals are valid. In DMA mode, an active low signal from the ISA bus indicating that a DMA acknowledge cycle is in progress.
64-62, 59-57, 55, 54	SD<7:0>	I/O	**SYSTEM DATA**: All data, command and status transfers take place over this bus.
33	/IOR	I	**I/O READ**: Active low signal from the system bus which indicates that the current bus cycle is an I/O read operation.
34	/IOW	I	**I/O WRITE**: Active low signal from the system bus which indicates that the current bus cycle is an I/O write operation.
35	AEN	I	**ADDRESS ENABLE**: Input signal from the system bus. When low, indicates that an I/O slave may respond to addresses and I/O commands on the system bus.
45 46-48 49-51 52	IRQ7, IRQ5-3, IRQ10-12	O	**INTERRUPT REQUEST**: Output to the system bus which indicates that the controller chip is requesting an interrupt. Pins not configured as outputs are in the three-state condition.

ISA Bus Interface Signals (continued)

PIN NUMBER	SYMBOL	TYPE	DESCRIPTION
22	IOCHRDY	O	**I/O CHANNEL READY**: Open drain output to the system bus which when high indicates that the addressed I/O device is ready for the bus transaction. The output is driven low when negated.
31	CLK	I	**CLOCK:** A free-running clock used to control internal timing operations. A possible source is OSC, the 14.3 MHz ISA bus clock.
3	/IOCS16	O	**I/O CHIP SELECT 16:** Asserted (low) to indicate that the addressed I/O window (/IOCSA, /IOCSB, /IOCSC or /IOCSD) supports 16-bit data transfers. The user controls whether this signal is asserted or not asserted for a specific chip select through values stored in the EEPROM. See Table 12, EEPROM addresses 0x00D, 0x010, 0x013 and 0x016.
2	/MEMCS16 {DREQ7}	O	**MEMORY CHIP SELECT 16{DREQ7}:** In MEMORY mode, asserted (low) to indicate that the addressed memory window supports 16-bit data transfers. This signal will be asserted for a specific address through values stored in the Plug and Play standard registers. /MEMCS16 will be asserted for any assertion of /MCSA if bit 1 of register 0x42 of logical device 0 is programmed to a '1' by the Plug and Play configuration software. It will also be asserted for any assertion of /MCSB under the following conditions: - In submodes 0 and 1, if bit 1 of register 0x4A of logical device 0 is set to a '1' by the Plug and Play configuration software. - In submodes 2 and 3, if bit 1 of register 0x42 of logical device 1 is set to a '1' by the Plug and Play configuration software. Note that the assertion of /MEMCS16 is based only on the comparison of the LA<23:17> signal lines against the corresponding upper and lower address values programmed for the two chip selects by the Plug and Play configuration software. Thus, the output will be asserted for the entire 128K address block(s) within which the chip select lies. The entire block must be all 8 bits or all 16 bits. Problems may arise if only a portion of the block is associated with the 16-bit resource and another portion with an 8-bit resource. This output is open drain when negated. In DMA mode, this pin is an an ouput indicating that the peripheral device is ready to transfer data. Used for both read and write operations. If not configured as an output the pin is maintained in the three-state condition.
28	/REFRESH {DRQB}	I	**REFRESH CYCLE{ DMA REQUEST B}:** In MEMORY mode this pin is an active low input which indicates that a refresh cycle is in progress on the platform. Memory chip select outputs are not generated while this input is asserted. In DMA mode, it is an active high input which is asserted to indicate that the device is requesting bus ownership to transfer data.

EEPROM Bus Interface Signals

PIN NUMBER	SYMBOL	TYPE	DESCRIPTION
68	DI	O	**EEPROM DATA IN**: Serial data to the EEPROM from the MB86703. This pin remains in three-state mode while the MB86703 is in *Wait for Key* state, except while the default values are being downloaded from the EEPROM at power-on reset.
66	SK	O	**EEPROM SHIFT CLOCK**: Signal generated by the MB86703 to shift data in and out of the EEPROM. This pin remains in three-state mode while the MB86703 is in *Wait for Key* state, except while the default values are being downloaded from the EEPROM at power-on reset.
67	EEPCS	O	**EEPROM CHIP SELECT**: A high signal selects the EEPROM for read and write operations. This pin remains in three-state mode while the MB86703 is in *Wait for Key* state, except while the default values are being downloaded from the EEPROM at power-on reset.
69	DO	I	**EEPROM DATA OUT**: Serial data from the EEPROM to the MB86703. Forcing this input to ground during RESET_DRV places the MB86703 in 'NEC Mode'. This changes the addresses of the ADDRESS and WRITE_DATA ports to 0x0259 and 0x0A59, respectively, to provide compatibility with NEC98 series computers. When not in NEC Mode, the port addresses are 0x0279 and 0x0A79, respectively.

Device Interface Signals

PIN NUMBER	SYMBOL	TYPE	DESCRIPTION
23 24 25 26	/IOCSA /IOCSB /IOCSC /IOCSD	O	**I/O CHIP SELECTS:** These active low outputs are assigned to different logical devices depending on the sub-mode in which the MB86703 is operating. Can be used by any device that requires I/O space
27	/MCSA {DRQA}	O {I}	**MEMORY CHIP SELECT A{DMA REQUEST A}:** This pin is always assigned to logical device 0 in any submode. In MEMORY mode, it is an active low output which can be used by any device that requires memory space. In DMA mode, it is an active high input which is asserted to indicate that the device is requesting bus ownership to transfer data.
29	/MCSB {/DACKA}	O	**MEMORY CHIP SELECT B{DMA ACKNOWLEDGE A}:** This pin is assigned to different logical devices depending on the sub-mode in which the MB86703 is operating. In MEMORY mode, it is an active low output which can be used by any device that requires memory space. In DMA mode, it is an active low output which indicates that the platform is ready to proceed with the requested DMA cycle. It is produced in response to receipt of /DACKn from the system bus.
32	NC{/ DACKB}	{O}	**NO CONNECT{DMA ACKNOWLEDGE B}:** Not used in MEMORY mode. In DMA mode, this is an active low output which indicates that the platform is ready to proceed with the requested DMA cycle. It is produced in response to receipt of /DACKn from the system bus.
39 42 43 44	INTA INTB INTC INTD	I	**INTERRUPT REQUESTS:** Inputs from the I/O controller which indicate that it is requesting an interrupt. These inputs are assigned to different logical devices depending on the submode in which the MB86703 is operating. The inputs can be programmed to be active high or active low. See Table 12, EEPROM addresses 0x017, 0x018, 0x019 and 0x01A.
53	ACTENA	I	**ACTIVATE ENABLE:** This pin, when asserted, causes the Activate bit in PnP register 0x30 for each logical device to be set or reset on power up depending on the value of the corresponding Activate bit in the EEPROM, address 0x01B. If the ACTENA pin is negated, the values in the EEPROM are ignored and the logical devices are not activated at power up or software reset. The state of the pin has no effect on the ability of software to set the Activate bit(s) in the 0x30 registers for each logical device during the configuration process.
38	RDY	I	**READY**: Input from the I/O device which goes low at the beginning of a read or write cycle and is set high when the peripheral controller is ready to complete the requested transaction.
37	/RESET	O	**BOARD RESET**: An active low output to the board produced in response to receipt of RESET_DRV on the ISA bus or if a reset command is issued by writing a "0x07" to the Configuration Control Register, 0x02.
1, 21, 30, 41, 56, 61, 65, 72	GND	-	**GROUND**: Signal and power ground.
20, 40, 60, 70	VDD	-	**POWER SUPPLY**: +5 volts 5%.

FUNCTIONAL OVERVIEW

The MB86703 is a generic Plug and Play device which when attached to ISA compatible controllers enables them to operate in the Plug and Play environment. In the Plug and Play environment users may plug peripheral cards such as LAN cards, graphics adapters or hard-disk controllers into their machines and system software configures each card automatically at power-up time. The need for configuration jumpers and switches on the adapter card is eliminated and installation of cards becomes more user friendly.

The MB86703 is based on the Plug and Play ISA Specification v1.0a and meets all ISA timing specifications as well.

The Plug and Play concept is built around the following four states: (1) *Wait for Key* (2) *Sleep* (3) *Isolation* and (4) *Configuration*. At power up, the cards begin in the *Wait for Key* state, awaiting the initiation key with outputs disabled. Once the initiation key is received, the *Sleep* state begins. The card remains in the *Sleep* state until it receives a Wake[CSN] command with the parameter data set to zero upon which the *Isolation* state is entered. After the card is isolated, it receives a unique Card Select Number (CSN). Once the CSN is written, the card moves into the *Configuration* state and its resources are read. All cards in a system follow the same procedure until their resource requirements are known.

Note: The following sections provide a brief overview of the Plug and Play configuration process. Please refer to the Plug and Play ISA specification for additional information.

Plug and Play Card Configuration Sequence

The MB86703 contains all the hardware resources required to allow the card to be identified and auto-configured by the Plug and Play software resident in the host system.

The auto configuration process consists of the following steps:

- All Plug and Play ISA cards are placed in the *Sleep* state.
- All Plug and Play ISA cards are isolated one at a time.
- As each card is isolated, assign a handle and read the card's resource data structure.
- After the resource requirements and capabilities are determined for all cards, the handle is used to place the card in *Configuration* state and assign conflict free resources to each card.
- All Plug and Play ISA cards are activated and removed from *Configuration* state.

The Plug and Play software uses three 8-bit I/O ports to execute a set of commands that identify and configure devices. A sequence of data writes to one of the ports, referred to as the initiation key, is used to enable the Plug and Play logic on all cards in the system.

Because all Plug and Play cards can respond to the same I/O port addresses, an isolation mechanism is required for the Plug and Play software to address each card independently. During *Isolation*, an isolation protocol is used to read a unique identifier on each card to isolate one Plug and Play card at a time. Following *Isolation*, the Plug and Play software assigns each card a handle (CSN) which is used to address that unique Plug and Play card. The software then reads the resource data structure which describes the resources supported and those requested by functions on the card.

When all resource capabilities and demands of the cards are known, the process of resource arbitration is invoked to determine resource allocation to each ISA card. A conflict detection mechanism is invoked to insure that resources assigned are not in conflict with standard ISA cards.Then, using the previously assigned handle, each Plug and Play card is placed in the *Configuration* state and the card is configured with the allocated resources through the Plug and Play standard registers. If the resources requested are not reconfigurable, equivalent resources will be supported. The resource data structure will inform the arbiter that the requested resources cannot be assigned to other Plug and Play cards in the system.

The command set also supports the ability to activate or deactivate the functions on the card.

Once the configuration is completed, Plug and Play cards are removed from the *Configuration* state and placed in normal system operation mode. To enter the *Configuration* state again, the initiation key must be reissued. This process prevents accidental erasure of the configuration information.

State Summary

The Plug and Play logic is quiescent on power up (*Wait for Key* state) and must be enabled by software. A predefined series of writes to the ADDRESS port places the Plug and Play logic into *Sleep* state. This is referred to as the initiation key. The write sequence is decoded by on-chip logic, and if the proper series of I/O writes is detected, the auto-configuration ports are enabled. If the data does not match, the internal logic is reinitialized and the chip remains in the *Wait for Key* state.

On the MB86703 there exists an 8-bit register called the Card Select Number (CSN) register (0x06) used to select one or more ISA cards when those cards are in certain states. The CSN mechanism allows a wide variety of devices to manage their configuration and control. The CSN register is set to 0x00 on all cards on power up. Once a card has been isolated, the CSN on that card is assigned a unique value which enables the

Plug and Play software to select this card later in the configuration process, without going through the protocol again.

The four Plug and Play states (see Figure 1) are summarized as follows:

- *Wait for Key* - Upon power-up reset and *Wait for Key* commands, all cards enter this state. No commands are active in this state until the initiation key is detected on the ISA bus. It is the default state for Plug and Play cards during normal system operation. After configuration and activation, software should return all cards to this state.While in the *Wait for Key* state, cards do not respond to any access to their auto-configuration ports until the initiation key is detected. All ISA accesses from the Plug and Play interface to the cards are ignored.
- *Sleep* - Plug and Play cards wait for a Wake[CSN] command in this state. Based on the write data and the value of the CSN on each card, this command will selectively enable one or more cards to the *Isolation* or *Configuration* states. To exit this state, the value of the write data bits[7:0] of the Wake[CSN] command must match the card's CSN. If the write data for Wake[CSN] is zero, then all cards that have not been assigned a CSN will enter the *Isolation* state. If the write data for the Wake[CSN] command is nonzero, then the one card whose assigned CSN matches the parameter of the Wake[CSN] command will enter the *Configuration* state.
- *Isolation* - The first time the cards enter the *Isolation* state, it is necessary to set the READ_DATA port address using the Set RD_DATA port command. Seventy-two pairs of reads are performed to the Serial Isolation register to isolate a card. If the checksum read from the card is valid, then one card has been isolated. The isolated card remains in the *Isolation* state. All other cards which have failed the isolation protocol will return to the *Sleep* state. The isolated card is assigned a unique value called the Card Select Number (CSN) and transitions to the *Configuration* state. The Wake[0] command causes the card to transition back to the *Sleep* state and all cards with a CSN value of zero to transition to the *Isolation* state. This entire process is repeated until all Plug and Play cards are detected.
- *Configuration* -In this state, the card responds to all configuration commands including reading the card's resource configuration information and programming the card's resource selections. Only one card may be in this state at a time.

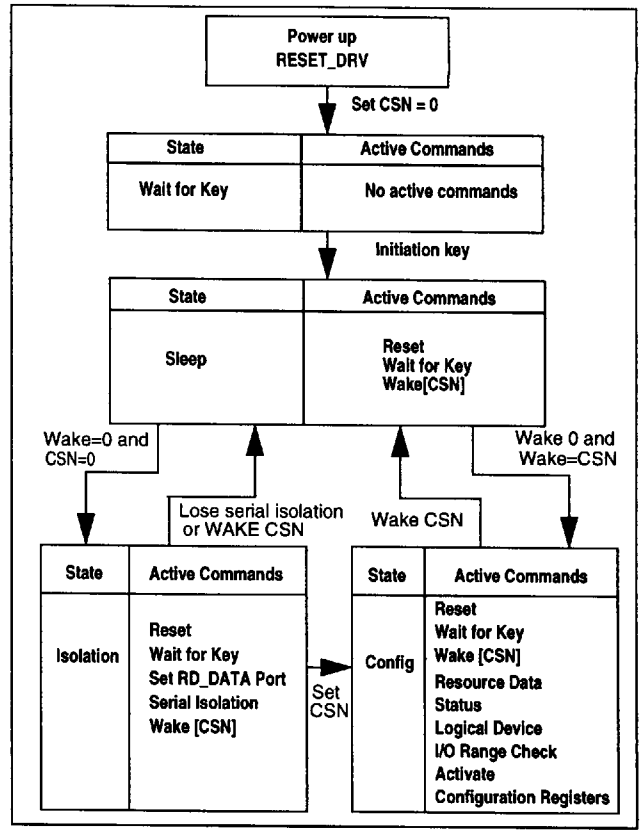


Figure 1. Plug and Play Configuration Process States

Notes:

1. CSN = Card Select Number.
2. RESET_DRV causes a state transition from the current state to *Wait for Key* and sets all CSNs to zero. All logical devices are set to their power-up configuration values.
3. The *Wait for Key* command causes a state transition from the current state to *Wait for Key*.

Auto-Configuration Ports

Three 8-bit ports are used by the software to access the configuration space on each Plug and Play ISA card. The ports are listed in Table 1. These registers are used by the Plug and Play software to issue commands, check status, access the resource data information, and configure the Plug and Play hardware. The ports have been chosen to avoid conflicts in the installed base of ISA functions, while at the same time minimizing the number of ports needed in the ISA I/O space.

Table 1. Auto-Configuration Ports

PORT NAME	LOCATION	TYPE
ADDRESS	0x0279(1)	Write-only
WRITE_DATA	0x0A79(2)	Write-only
READ_DATA	Relocatable in range 0x0203 to 0x03FF	Read-only

Notes:

1. Address is 0x0259 if the MB86703 is in NEC mode.
2. Address is 0x0A59 if the MB86703 is in NEC mode.

The three auto-configuration ports use a 12-bit ISA address decode. The ADDRESS and WRITE_DATA ports are located at fixed addresses. The WRITE_DATA port is located at an address alias of the ADDRESS port. The READ_DATA port, which is the only readable auto-configuration port, is relocatable within the I/O range from 0x0203 to 0x03FF. The address of the READ_DATA port is assigned by the system software and is set by writing the proper value to Plug and Play control register 0x00 (Set RD_DATA Port command). The isolation protocol verifies that the location selected for the READ_DATA port is free of conflict.

The Plug and Play registers within the MB86703 are accessed by writing the address of the desired register to the ADDRESS port, followed by a read of data from the READ_DATA port or a write of data to the WRITE_DATA port. A write to the ADDRESS port may be followed by any number of WRITE_DATA or READ_DATA accesses to the same register location without the need to write to the ADDRESS port before each access.

Obtaining The Device Configuration

The driver or other application software requires a mechanism to determine the configuration information in order to communicate with the card. An Application Programming Interface (API) exists to provide the required data. Called the Plug and Play Configuration Manager API, it is documented in the "Plug and Play Device Driver Developer's Guide" (Intel Publication Number 485473-001) or equivalent documentation provided by the supplier of the Plug and Play system software. Also see "Plug and Play Device Driver Interface for Microsoft Windows 3.1 and MS-DOS" (available on the Plug and Play forum on CompuServe).

The API requires only two calls to retrieve configuration:

- **CM_GetVersion** verifies the presence of the Configuration Manager.
- **CM_GetConfig** retrieves the configuration information from an indexed, system wide table. This information includes READ_DATA port address, Card Select Number (CSN) and resource allocation for each configured device.

The Configuration Manager also provides a Configuration Access (CA) support interface. Two calls associated with this interface of particular interest are:

- **CA_GetVersion** verifies the presence of the Configuration Access support interface.
- **CA_PnPISA_Get_Resource_Data** retrieves the resource data stored in the EEPROM connected to the MB86703 and can be used to obtain the data stored in the "Vendor Defined" resource data types.

MB86703 DETAILED DESCRIPTION

Operating Modes

The MB86703 features several operating modes that permit it to be used in a variety of environments and applications.

BUS MODES

The MB86703 operates in one of two bus modes:

ISA Mode: In this mode the addresses of the ADDRESS and WRITE_DATA ports are 0x0279 and 0x0A79, respectively.

NEC Mode: In this mode the addresses of the ADDRESS and WRITE_DATA ports are 0x0259 and 0x0A59, respectively, to provide compatibility with NEC PC98-series computers.

The ISA Mode is the normal operating mode. The NEC Mode is entered by forcing the DO input to ground during RESET_DRV.

RESOURCE MODES

The MB86703 operates in one of two resource modes:

DMA Mode: In this mode the device supports interrupts, I/O chip selects and DMA requests.

Memory Mode: In this mode the device supports interrupts and I/O and memory chip selects.

For each of the two resource modes there are four submodes. Each submode supports different numbers of logical devices, as per the table below, and allocates the supported resources amongst the logical devices in different ways. See Table 2 and Figures 2 and 3.

SUBMODE NUMBER	NUMBER OF LOGICAL DEVICES
0	One
1	Two
2	Two
3	Four

Table 2. MB86703 Submodes and Resource Assignments

SUBMODE/ LOGICAL DEVICE #	DMA CHANNELS*		MEMORY CHIP SELECTS*		I/O CHIP SELECTS				INTERRUPTS			
CARD SIDE I/O PINS ------>	DMA A	DMA B	/MCS A	/MCS B	/IOCS A	/IOCS B	/IOCS C	/IOCS D	INT A	INT B	INT C	INT D
0/LD0	DMA0	DMA1	/MCS0	/MCS1	/IOCS0	/IOCS1	/IOCS2	/IOCS3	INT0	INT1	NOT USED	NOT USED
1/LD0	DMA0	DMA1	/MCS0	/MCS1	/IOCS0	/IOCS1			INT0	INT1		
1/LD1							/IOCS0	/IOCS1			INT0	INT1
2/LD0	DMA0		/MCS0		/IOCS0	/IOCS1			INT0	INT1		
2/LD1		DMA0		/MCS0			/IOCS0	/IOCS1			INT0	INT1
3/LD0	DMA0		/MCS0		/IOCS0				INT0			
3/LD1		DMA0		/MCS0		/IOCS0				INT0		
3/LD2							/IOCS0				INT0	
3/LD3								/IOCS0				INT0

* The MB86703 supports either DMAs or memory chip selects, depending on mode.

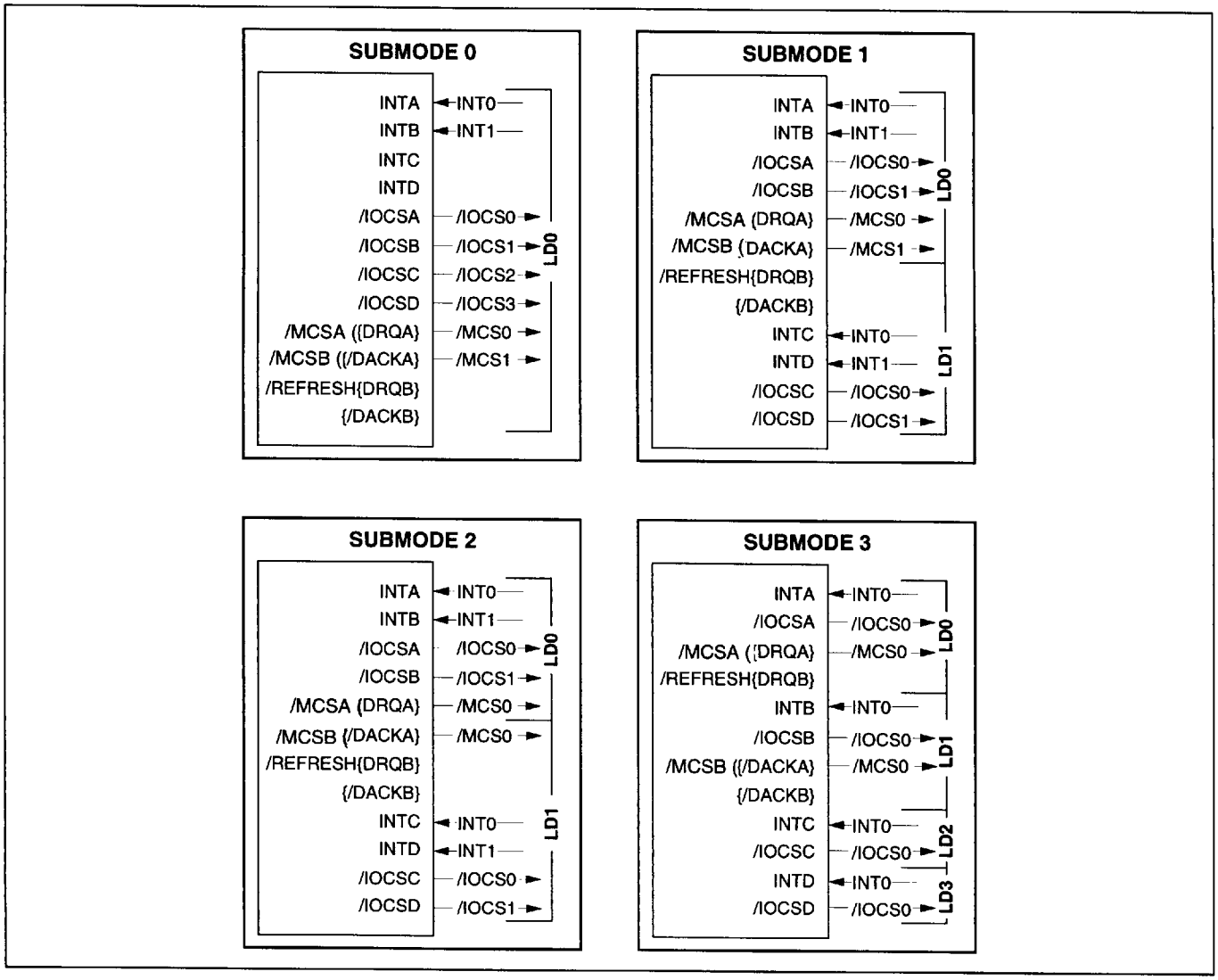


Figure 2. MB86703 Resource Assignments in MEMORY Mode

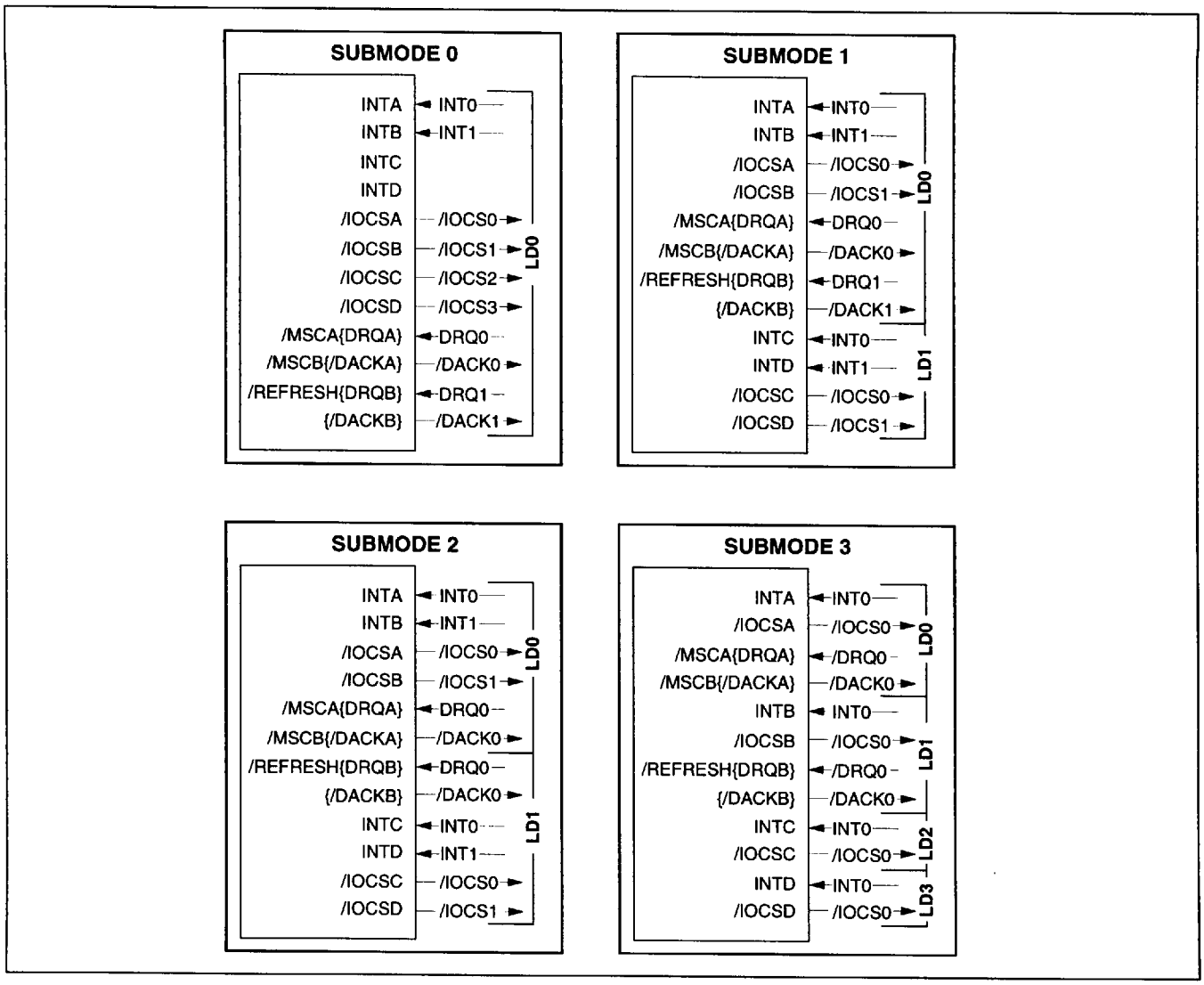


Figure 3. MB86703 Resource Assignments in DMA Mode

Registers

Operation of the MB86703 is controlled by values written into registers within the device, while other registers provide device status. The register set consists of a combination of Plug and Play standard registers and vendor defined registers. Tables 3 and 4 are maps of the user-accessible internal registers implemented in the MB86703 for MEMORY and DMA modes, respectively. In this table, a "Y" in the STD column indicates that this is a standard PnP register and is described in the Plug and Play ISA specification (Appendix A). The table also provides default values and defines, for each Plug and Play state, the type of access available. Exceptions to the specification are detailed in Table 5. Vendor-defined registers contained in the MB86703 are described in Tables 6 to 8.

Table 3. MB86703 Registers in MEMORY Mode

			SUBMODE/LOGICAL DEVICE (NOTE 1)									DEFAULT	ACCESS BY STATE			
			0	1		2		3								
REG	STD. ?	FUNCTION	LD0	LD0	LD1	LD0	LD1	LD0	LD1	LD2	LD3	VALUE	WT4KEY	SLEEP	ISOL	CONFIG
0x00	Y	Set READ_DATA Port	X									UNDEFINED			W	
0x01	Y	Serial Isolation	X									0x00			R	
0x02	Y	Configuration Control	X									0x00		W	W	W
0x03	Y	Wake [CSN]	X									0x00		W	W	W
0x04	Y	Resource Data	X									UNDEFINED				R
0x05	Y	Status	X									UNDEFINED				R
0x06	Y	Card Select Number	X									0x00			W	R
0x07	Y	Logical Device Number	X									0x00				R/W
0x22	N	EEPROM Write Enable	X									UNDEFINED				W
0x23	N	EEPROM Write Data Low	X									0x00				W
0x24	N	EEPROM Write Data High	X									0x00				W
0x25	N	PnP State	X									0x00				R
0x26	N	EEPROM Command	X									0x00				W
0x30	Y	Activate	X	X	X	X	X	X	X	X	X	NOTE 2				R/W
0x31	Y	I/O Range Check	X	X	X	X	X	X	X	X	X	EEPROM				R/W
0x40	Y	Mem. Base Address 0 [23:16]	X	X		X	X	X	X			EEPROM				R/W
0x41	Y	Mem. Base Address 0 [15:8]	X	X		X	X	X	X			EEPROM				R/W
0x42	Y	Memory Control 0	X	X		X	X	X	X			EEPROM				R/W
0x43	Y	Mem. Upper Limit 0 [23:16]	X	X		X	X	X	X			EEPROM				R/W
0x44	Y	Mem. Upper Limit 0 [15:8]	X	X		X	X	X	X			EEPROM				R/W
0x48	Y	Mem. Base Address 1 [23:16]	X	X								EEPROM				R/W
0x49	Y	Mem. Base Address 1 [15:8]	X	X								EEPROM				R/W
0x4A	Y	Memory Control 1	X	X								EEPROM				R/W
0x4B	Y	Mem. Upper Limit 1 [23:16]	X	X								EEPROM				R/W
0x4C	Y	Mem. Upper Limit 1 [15:8]	X	X								EEPROM				R/W
0x60	Y	I/O Base Address 0 [15:8]	X	X	X	X	X	X	X	X	X	EEPROM				R/W
0x61	Y	I/O Base Address 0 [7:0]	X	X	X	X	X	X	X	X	X	EEPROM				R/W
0x62	Y	I/O Base Address 1 [15:8]	X	X	X	X	X					EEPROM				R/W
0x63	Y	I/O Base Address 1 [7:0]	X	X	X	X	X					EEPROM				R/W
0x64	Y	I/O Base Address 2 [15:8]	X									EEPROM				R/W
0x65	Y	I/O Base Address 2 [7:0]	X									EEPROM				R/W
0x66	Y	I/O Base Address 3 [15:8]	X									EEPROM				R/W
0x67	Y	I/O Base Address 3 [7:0]	X									EEPROM				R/W
0x70	Y	Interrupt Request Level 0	X	X	X	X	X	X	X	X	X	EEPROM				R/W
0x71	Y	Interrupt Request Type 0	X	X	X	X	X	X	X	X	X	EEPROM				R/W
0x72	Y	Interrupt Request Level 1	X	X	X	X	X					EEPROM				R/W
0x73	Y	Interrupt Request Type 1	X	X	X	X	X					EEPROM				R/W

Notes

1. An 'X' indicates that the register exists for that submode/logical device
2. Default value = (Corresponding bit in EEPROM 0x01B) AND (ACTENA)

Table 4. MB86703 Registers in DMA Mode

			SUBMODE/LOGICAL DEVICE (NOTE 1)									DEFAULT	ACCESS BY STATE			
			0	1		2		3								
REG	STD. ?	FUNCTION	LD0	LD0	LD1	LD0	LD1	LD0	LD1	LD2	LD3	VALUE	WT4KEY	SLEEP	ISOL	CONFIG
0x00	Y	Set READ_DATA Port					X					UNDEFINED			W	
0x01	Y	Serial Isolation					X					0x00			R	
0x02	Y	Configuration Control					X					0x00		W	W	W
0x03	Y	Wake [CSN]					X					0x00		W	W	W
0x04	Y	Resource Data					X					UNDEFINED				R
0x05	Y	Status					X					UNDEFINED				R
0x06	Y	Card Select Number					X					0x00			W	R
0x07	Y	Logical Device Number					X					0x00				R/W
0x22	N	EEPROM Write Enable					X					UNDEFINED				W
0x23	N	EEPROM Write Data Low					X					0x00				W
0x24	N	EEPROM Write Data High					X					0x00				W
0x25	N	PnP State					X					0x00				R
0x26	N	EEPROM Command					X					0x00				W
0x30	Y	Activate	X	X	X	X	X	X	X	X	X	NOTE 2				R/W
0x31	Y	I/O Range Check	X	X	X	X	X	X	X	X	X	EEPROM				R/W
0x60	Y	I/O Base Address 0 [15:8]	X	X	X	X	X	X	X	X	X	EEPROM				R/W
0x61	Y	I/O Base Address 0 [7:0]	X	X	X	X	X	X	X	X	X	EEPROM				R/W
0x62	Y	I/O Base Address 1 [15:8]	X	X	X	X	X					EEPROM				R/W
0x63	Y	I/O Base Address 1 [7:0]	X	X	X	X	X					EEPROM				R/W
0x64	Y	I/O Base Address 2 [15:8]	X									EEPROM				R/W
0x65	Y	I/O Base Address 2 [7:0]	X									EEPROM				R/W
0x66	Y	I/O Base Address 3 [15:8]	X									EEPROM				R/W
0x67	Y	I/O Base Address 3 [7:0]	X									EEPROM				R/W
0x70	Y	Interrupt Request Level 0	X	X	X	X	X	X	X	X	X	EEPROM				R/W
0x71	Y	Interrupt Request Type 0	X	X	X	X	X	X	X	X	X	EEPROM				R/W
0x72	Y	Interrupt Request Level 1	X	X	X	X	X					EEPROM				R/W
0x73	Y	Interrupt Request Type 1	X	X	X	X	X					EEPROM				R/W
0x74	Y	DMA Channel 0	X	X		X	X	X	X	X	X	EEPROM				R/W
0x75	Y	DMA Channel 1	X	X								EEPROM				R/W

Notes

1. An 'X' indicates that the register exists for that submode/logical device
2. Default value = (Corresponding bit in EEPROM 0x01B) AND (ACTENA)

As previously described, the registers are accessed for read and write operations via the ADDRESS, WRITE_DATA and READ_DATA auto-configuration ports (see Table 1). The ADDRESS and WRITE_DATA ports have defined ISA addresses.
In a PnP system, the READ_PORT address is normally assigned by the PnP system software during *Isolation*. In that environment, the address of the READ_DATA port can be determined by using the CM_GetConfig call to the Configuration Manager as previously described. In a non-PnP system, the READ_DATA port address will have been assigned by the configuration utility used to configure the card, and can be determined as appropriate for that software.

Table 5. MB86703 Standard PnP Register Exceptions

ADD	EXCEPTION
0x71, 0x73	Bit<0> does not perform any function. The type of interrupt (level or edge) cannot be controlled by the MB86703 and will depend entirely on the type of input signal supplied at the INT inputs.
0x42, 0x4A	The MB86703 supports only the 'upper limit' method of specifying the memory chip select range. Thus, bit 0 of these registers is read only and is internally set to a '1'.

Table 6. EEPROM Write Enable/Write Disable (0x22)

BIT	DESCRIPTION
<0>	Setting this bit to a "1" enables writes to the serial EEPROM, clearing it disables such writes. After setting or clearing this bit, a 0x00 command must be issued to the EEPROM Command Register to transfer the enable/disable command to the EEPROM. The EEPROM will remain write enabled (or disabled) until another enable/disable command is issued.
<7:1>	Not implemented.

Table 7. EEPROM Write Data Low (0x23)

BIT	DESCRIPTION
<7:0>	The lower byte of the word which is to be written into the EEPROM at the next EEPROM write operation.

Table 8. EEPROM Write Data High (0x24)

BIT	DESCRIPTION
<7:0>	The upper byte of the word which is to be written into the EEPROM at the next EEPROM write operation.

Table 9. MB86703 PnP State (0x25)

BIT	DESCRIPTION
<0>	0 = Not in the *Wait for Key* state. 1 = In the *Wait for Key* state.
<1>	0 = Not in the *Sleep* state. 1 = In the *Sleep* state.
<2>	0 = Not in the *Isolation* state. 1 = In the *Isolation* state.
<3>	0 = Not in the *Configuration* state. 1 = In the *Configuration* state.
<4>	0 = DMA mode 1 = Memory mode
<6:5>	Submode
<7>	Not used. '0' when read.

Table 10. EEPROM Command (0x26)

BIT	DESCRIPTION
<7:0>	Writing 0x00 into this register causes a write enable/disable command to be sent to the serial EEPROM. Register 0x22 must be set/cleared before this command is issued. See Table 6. Writing a 0x01 into this register initiates an EEPROM write cycle, causing the contents of registers 0x23 and 0x24 to be written into the EEPROM. The EEPROM must have been write enabled before this command is issued. Writing 0x03 into this register causes the EEPROM read pointer to be reset to point at the first word of the EEPROM, address 0x000. **CAUTION:** If this command is invoked, the current EEPROM read pointer address is overwritten, and subsequent operations may be incorrect. The MB86703 should be reset before resuming normal operation.

CONTROL REGISTER SUMMARY

Plug and Play cards respond to commands written to Plug and Play registers as well as certain ISA bus conditions. These commands are summarized below:

RESET_DRV - This is the ISA bus reset signal. Upon detection of this signal, the Plug and Play card enters the *Wait for Key* state and all CSNs are reset to 0x00. Default values are loaded from non-volatile memory to the configuration registers. A logical device becomes active at reset if the /ACTENA pin is asserted (low) and the corresponding Activate bit in the EEPROM, address 0x01B, is set. If the /ACTENA pin is negated, the values in the EEPROM are ignored and the logical devices are not activated at power-up reset. The state of the pin has no effect on the ability of software to set or reset each logical device's Activate register (0x30) during the configuration process.

Note: The software must delay 1 msec after RESET_DRV before accessing the auto-configuration ports.

- Config Control Register - The Config Control Register enables assertions of three independent commands which are activated by writing a "1" to their corresponding register bits. These bits are automatically reset to "0" by the hardware after the commands execute.
  - Reset command - The Reset command is sent to the Plug and Play cards by writing a value of 0x01 to the Config Control register. All Plug and Play cards in any state, except those in *Wait for Key*, respond to this command. This command performs a reset function on all logical devices. This resets the contents of configuration registers to their default state. The configuration registers for all logical devices are loaded with their power up values from non-volatile memory. The READ_DATA port, CSN and Plug and Play state are preserved.
  - Wait for Key command - The Wait for Key command is sent to the Plug and Play cards by writing a value of 0x02 to the Config Control register. All Plug and Play cards in any state will respond to this command. The CSNs are preserved and no logical device status is changed.
  - Reset CSN command - The Reset CSN command is sent to the Plug and Play cards by writing the value of 0x04 to the Config Control register. All Plug and Play cards in any state except *Wait for Key* will reset their CSN to 0x00.
  - Writing 0x07 to the Config Control Register is equivalent to a RESET_DRV event.

  Note: The software must delay for 1 ms after the Reset command before accessing the auto-configuration ports.
- Set RD_DATA Port Command - This command is used in the *Isolation* state and sets the address of the READ_DATA port. Write data bits [7:0] are used as ISA I/O bus address bits [09:02]. The ISA bus address bits [1:0] are fixed at binary "11". The ISA bus address bits [15:10] are fixed at binary "000000".

  Note: After a RESET_DRV or Reset CSN command, this register is considered uninitialized and must be reinitialized.
- Serial Isolation Register - A read from the Serial Isolation Register causes Plug and Play cards in the *Isolation* state to respond to the ISA bus read cycle.
- Card Select Number - A Card Select Number is uniquely assigned to each Plug and Play card when the card has been isolated and is the only card in the *Isolation* state. An unidentified card is assigned a value of zero. Valid Card Select Numbers for identified ISA cards range from 1 to 255 and must be assigned sequentially starting from 1. The Card Select Number is used to select a card via the Wake[CSN] command. The Card Select Number on all ISA cards is set to zero on a RESET_DRV or Reset CSN command. The CSN is never set to zero using the CSN register.
- Wake[CSN] Command - This command is used to bring ISA cards in the *Sleep* state into either the *Isolation* state or the *Configuration* state. A Wake[CSN] command with a parameter of zero will force all cards without a CSN to enter the *Isolation* state. A Wake[CSN] command with a parameter other than zero will force a card with a matching CSN to enter the *Configuration* state. Any card in the *Isolation* or *Configuration* state that receives a Wake[CSN] command with a parameter that does not match its CSN will transition to the *Sleep* state. All Plug and Play cards function as if their 72-bit serial identifier and their resource data come from a single serial device. The pointer to this data is reset to the beginning whenever a card receives a Wake[CSN] command that has a non-zero CSN value.
- Resource Data Register - One byte of resource data from the Plug and Play card is returned upon a read of this register when in the *Configuration* state. This data is always returned byte sequentially and the Status register must be read to confirm that resource data is available before

the register can be read.

- Status register - Bit [0] of the status register indicates that the next byte of resource data is available to be read. If this bit is one, then data is available, otherwise resource data is not yet available. The Plug and Play software will poll this location until bit [0] is set, then the next data byte from the Resource Data register is read.
- Logical Device Number Register - This register is used to select the logical device on which the configuration commands to follow will operate.
- I/O Range Check Register - This register allows the Plug and Play software to determine if another card conflicts with the I/O port range that has been assigned to a logical device. The I/O range check works by having all I/O ranges that would be used by a logical device return 0x55 then 0xAA on I/O read commands. The Plug and Play software performs reads to all the ports that would be used by the logical device and verifies that the correct data is returned. If a conflict is detected, then the Plug and Play software relocates the I/O range of the logical devices a new location. Setting bit [1] of this register enables the I/O range check logic. Setting bit [0] forces the logical device to respond to I/O reads within its assigned I/O range with the value 0x55. If bit [0] is cleared, then the logical device responds to reads within its assigned I/O range with the value of 0xAA. This function operates only when bit [0] of the Activate register is not set.
- Activate register - The Activate register is a read/write register that is used to activate a logical device. An active logical device responds to all ISA bus cycles as allowed by its normal operation. Bit [0] is the activate bit. If it is set to "1" then the logical device is active, otherwise it is inactive.

EEPROM

The MB86703 interfaces to the serial EEPROM through a four-wire interface as described in the Signal Descriptions section of this data sheet. The EEPROM is an industry standard 93C56 or equivalent, a 2048-bit device which is internally organized as 128 words by 16 bits (the 256 word device in this family can also be used).

It should be noted that the data is internally stored in the EEPROM in a bit-reversed format. That is, the least significant bit of the lower byte of data is stored in the most significant bit of the EEPROM word, while the most significant bit of the upper byte of data is stored in the least significant bit of the EEPROM word, as shown in the example below. This rearrangement of data is not important if the EEPROM is programmed via the MB86703, but must be considered if the EEPROM is programmed by other means.

DATA UPPER BYTE								DATA LOWER BYTE							
1	0	1	1	0	0	1	1	0	1	0	1	1	0	1	0

DATA IN EEPROM															
0	1	0	1	1	0	1	0	1	1	0	0	1	1	0	1

EEPROM MEMORY MAP

The memory map of the EEPROM is shown in Table 11. Upon reset, an internal pointer to the EEPROM is initialized to address the first word of the EEPROM and the default configuration values (0x000 - 0x01B) are read and automatically loaded into the appropriate registers, as detailed in Table 12. In the *Isolation* state, an additional nine bytes (0x1C - 0x24, the Plug and Play Serial Identifier) are read from the EEPROM and loaded into an internal shift register for use during the card identification and isolation process. At this point, the internal pointer is pointing to the first byte of the card's resource data structure, 0x25. When the card enters the *Configuration* state in response to the card winning the serial isolation protocol and having a CSN assigned, the resource data will be read and used as an input to the resource allocation process performed by the system software. If the card enters the *Configuration* state directly in response to the Wake[CSN] command, the nine byte serial identifier must be read first before the card's resource data is accessed because the pointer to the serial EEPROM is reset to 0x1C in response to the Wake[CSN] command where the CSN matches the card's CSN and does not equal zero.

Table 11. EEPROM Memory Map

BYTE ADDRESS	CONTENTS
0x000 . . 0x01B	**Default values for configuration registers.** See Table 12.
0x01C 0x024	**Serial Identifier** See Plug and Play Specification v1.0a, Table 2 and Section 6.1: Vendor ID Serial Number Checksum
0x025 . . . . 0x1FF	**Resource Data.** See Plug and Play Specification v1.0a, Section 6.1: PnP Version Number Identifier String Logical Device ID(3) Resource Data(3) Optional Vendor Defined Data(1) End Tag Optional Vendor Defined Data(2)

Notes:

1. Vendor defined data inserted as part of the Resource data must use standard formats per sections 6.2.2.10 and 6.2.3.4 of the PnP specification.
2. Vendor defined data inserted following the End Tag may use any format.
3. Repeated for each logical device.

Table 12. Default Register Values in EEPROM

BYTE ADDRESS	CONTENTS	
	MEMORY MODE	DMA MODE
0x000	Bit <0>: 0 = DMA Mode, 1 = Memory Mode Bits <2:1>: = Submode, 00= 0, 01 = 1, 10 = 2, 11 = 3	
0x001	MCSA: Mem Base Add [15:8]	not used
0x002	MCSA: Mem Base Add [23:16]	not used
0x003	MCSA: Bit <0>: Not used Bit <1>: 8/16 (Memory Control) Bit <2>: AEN in Decode, 0 = N, 1 = Y	DMAA: Bits <6:4>: DMA Channel A 000 = 0 100 = no DMA 001 = not valid 101 = 5 010 = not valid 110 = 6 011 = 3 111 = 7
0x004	MCSA: Mem High Add [15:8]	not used
0x005	MCSA: Mem High Add [23:16]	not used
0x006	MCSB: Mem Base Add [15:8]	not used
0x007	MCSB: Mem Base Add [23:16]	not used

Table 12. Default Register Values in EEPROM (continued)

BYTE ADDRESS	CONTENTS	
	MEMORY MODE	**DMA MODE**
0x008	MCSB: Bit <0>: Not used Bit <1>: 8/16 (Memory Control) Bit <2>: AEN in Decode, 0 = N, 1 = Y	DMAB: Bits <6:4>: DMA Channel B See 0x003 above
0x009	MCSB: Mem High Add [15:8]	not used
0x00A	MCSB: Mem High Add [23:16]	not used
0x00B	IOCSA: I/O Base Add [7:0]	
0x00C	IOCSA: I/O Base Add [15:8]	
0x00D	IOCSA: Bit <0>: Assert /IOCS16, 0 = N, 1 = Y Bits <3:1>: Range in bytes 000 = 2 010 = 8 100 = 32 110 = 128 001 = 4 011 = 16 101 = 64 111 = not valid	
0x00E	IOCSB: I/O Base Add [7:0]	
0x00F	IOCSB: I/O Base Add [15:8]	
0x010	IOCSB: See 0x00D above	
0x011	IOCSC: I/O Base Add [7:0]	
0x012	IOCSC: I/O Base Add [15:8]	
0x013	IOCSC: See 0x00D above	
0x014	IOCSD: I/O Base Add [7:0]	
0x015	IOCSD: I/O Base Add [15:8]	
0x016	IOCSD: See 0x00D above	
0x017 (note 1)	Interrupt Request A: Bits <3:0> = ISA Bus Interrupt Level 0000 = no IRQ 1000 = not valid 0001 = not valid 1001 = not valid 0010 = not valid 1010 = 10 0011 = 3 1011 = 11 0100 = 4 1100 = 12 0101 = 5 1101 = not valid 0110 = not valid 1110 = not valid 0111 = 7 1111 = 15 Bits <5:4> = ISA Bus Interrupt Output Type 00 = low, edge 10 = high, edge 01 = low, level 11 = high, level (Note: Interrupt output type will be a function of input type and bit <6> value. Bit 4 does not perform any internal function but should be programmed to correspond to the type of input supplied, edge or level.) Bit <6>: Input Polarity 0 = input is active HIGH 1 = input is active LOW	

Table 12. Default Register Values in EEPROM (continued)

BYTE ADDRESS	CONTENTS	
	MEMORY MODE	DMA MODE
0x018 (note 1)	Interrupt Request B: See 0x017 above	
0x019 (note 1)	Interrupt Request C: See 0x017 above	
0x01A (note 1)	Interrupt Request D: See 0x017 above	
0x01B	Activate: Bits <3:0>: Logical Devices 3, 2, 1, 0 respectively Note: Enabled/Disabled by state of ACTENA input pin	

Notes:
1. Each interrupt must be programmed to a unique value if it is used.

READING DATA FROM THE EEPROM

In order to read the contents of the EEPROM, the MB86703 must be placed into the *Configuration State*. The flow chart in Figure 4 outlines the process. Data is read sequentially from the Resource Data Register, one byte at a time, starting at address 0x000. Note that the Status Register must be polled before each read of the Resource Data Register to assure that the data from the EEPROM has been obtained and is ready to be read.

CAUTION: The process of resetting the EEPROM read data pointer to address 0x000 by writing 0x03 into PnP register 0x26 overwrites the current EEPROM read pointer value. Subsequent operations may be incorrect if the MB86703 is not reset before resuming normal operation.

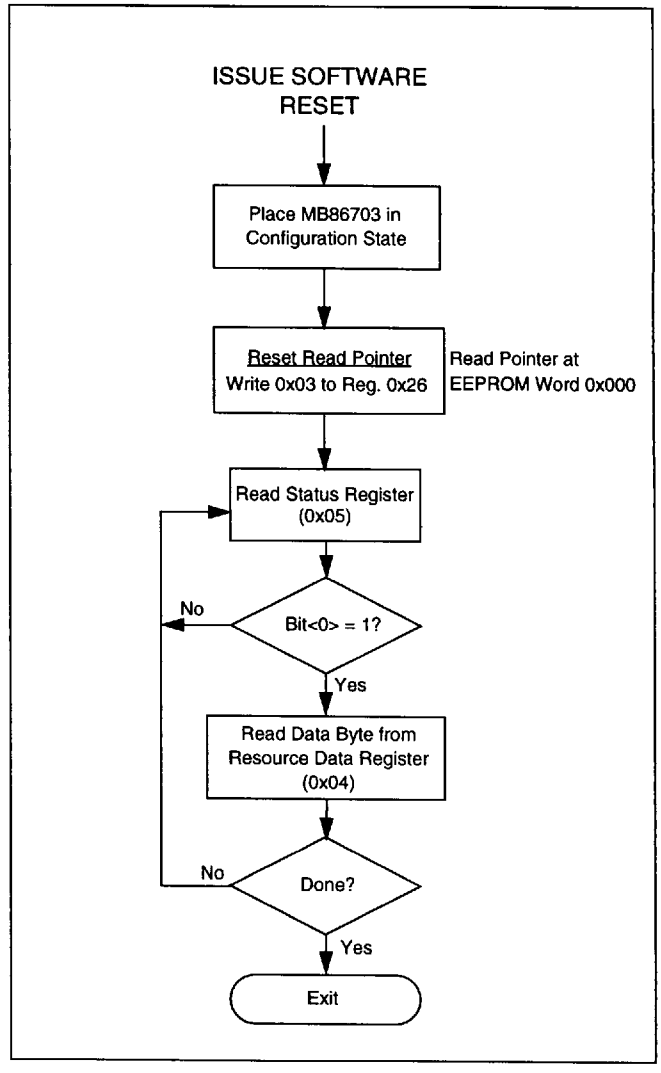


Figure 4. Reading Data from the EEPROM

WRITING DATA TO THE EEPROM

In order to write data into the EEPROM, the MB86703 must be placed into the *Configuration State*. The MB86703 contains a write address pointer which is set to point to address 0x000 in the EEPROM upon reset. Note that this pointer is separate from the read address pointer and is not affected by any EEPROM data read operations.

The flow chart in Figure 5 outlines the EEPROM write process. First, the EEPROM is write enabled. Data is then written sequentially, one word at a time, starting from address 0x000. As a final step, a Write Disable command is sent to the EEPROM to protect the data from any inadvertent writes. Note that a timeout equal to or longer than the specified EEPROM write cycle time (typically 10 ms) is required after the write command for each word of data.

SHARING THE EEPROM WITH OTHER DEVICES

The EEPROM input and output pins are three-stated when the MB86703 is in the *Wait for Key* state, except during power-on reset while the MB86703 reads the default configuration register and other initialization values. Since the device can be placed into this state except during the identification and configuration process, this allows other devices on the card to access the EEPROM during other periods. Any space not used for the initialization data required by the MB86703 and the device resource data (see Table 11) can be used by other devices on the card.

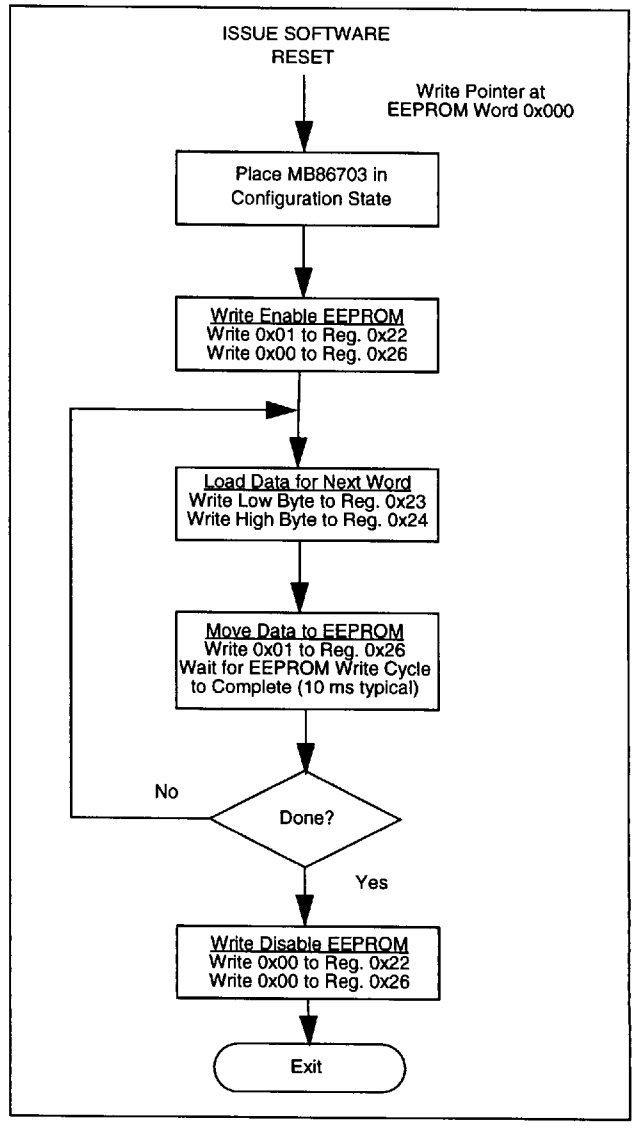


Figure 5. Writing Data into the EEPROM

APPLICATIONS

Figures 6 and 7 illustrate typical applications of the MB86703.

In Figure 6, the chip is combined with Fujitsu's MB86964 Ethernet controller with Twisted Pair transceiver to form a highly integrated Plug and Play ready Ethernet adapter card. The MB86964 uses one I/O chip select and one interrupt. A memory chip select is used to address the boot PROM or flash memory.

A high-speed serial line to Ethernet bridge application is illustrated in Figure 7. In this application the MB86703 is programmed to support four logical devices (three are used) and to support DMA channel configuration. Logical Device 0 provides interrupt, DMA and I/O chip select support for the USART controller. Logical Devices 1 and 2 provide interrupt and I/O chip select support for the modem and MB86964 Ethernet controller. By assigning separate logical devices to each function, each can be activated or deactivated independently and the driver can be partitioned into separate modules,allowing each to be written and debugged independent of the others.

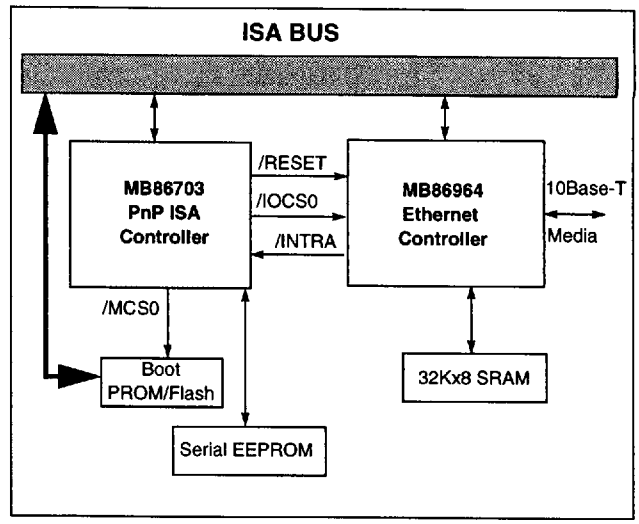


Figure 6. Typical MB86703 Application - Ethernet Controller

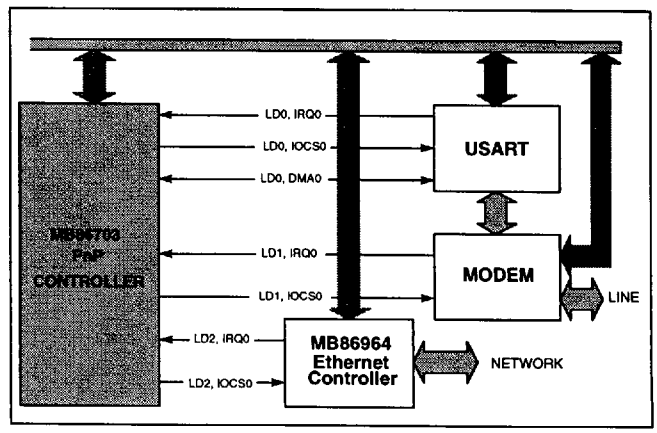


Figure 7. Typical MB86703 Application - Serial Line to Ethernet Bridge

SPECIFICATIONS

DC Characteristics

All Specifications are Valid Over the Recommended Operating Conditions Unless Otherwise Noted.

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER DESCRIPTION	MIN	MAX	UNITS
V_{DD}	Supply Voltage	-0.3	6.0	V
V_{IN}	Input Voltage	-0.3	V_{DD} + 0.3	V
V_{OUT}	Output Voltage	-0.3	V_{DD} + 0.3	V
T_{STG}	Storage Temperature	-40	+125	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER DESCRIPTION	MIN	TYP	MAX	UNITS
V_{DD}	Supply Voltage	4.75		5.25	V
V_{IH}	High Level Input Voltage	2.4			V
V_{IL}	Low Level Input Voltage			0.4	V
T_A	Operating Temperature	0		+70	°C

DC CHARACTERISTICS

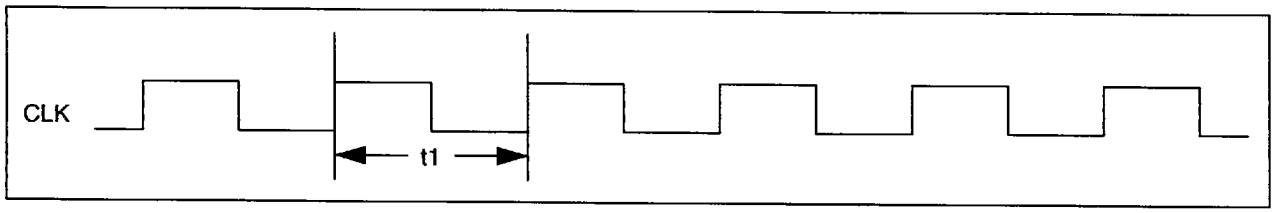
SYMBOL	PARAMETER DESCRIPTION	CONDITION	MINIMUM	TYPICAL	MAXIMUM	UNIT
V_{IL}	Low Level Input Voltage				0.8	V
V_{IH}	High Level Input Voltage		2.2		V_{DD}	V
V_{OL1}(1)	Low Level Output Voltage	I_{OL} = 4mA	0		0.4	V
V_{OH1}(1)	High Level Output Voltage	I_{OH} = -2mA	4.0		V_{DD}	V
V_{OL2}(2)	Low Level Output Voltage	I_{OL} = 8mA	0		0.4	V
V_{OL3}(3)	Low Level Output Voltage	I_{OL} = 12mA	0		0.4	V
V_{OH3}(3)	High Level Output Voltage	I_{OH} = -4mA	4.0		V_{DD}	V
V_{OL4}(4)	Low Level Output Voltage	I_{OL} = 24mA	0		0.4	V
V_{OH4}(4)	High Level Output Voltage	I_{OH} = -8mA	4.0		V_{DD}	V
I_L	Input Leakage Current		-10		10	uA
I_{CCS}	Static Power Supply Current				100	uA
I_{CCA}	Active Power Supply Current				60	mA

Notes:
1. Applies to O 4 type outputs. See Pin Assignment Table.
2. Applies to O 8 type outputs. See Pin Assignment Table.
3. Applies to O 12 type outputs. See Pin Assignment Table.
4. Applies to O 24 and I/O 24 type outputs. See Pin Assignment Table.

AC Characteristics

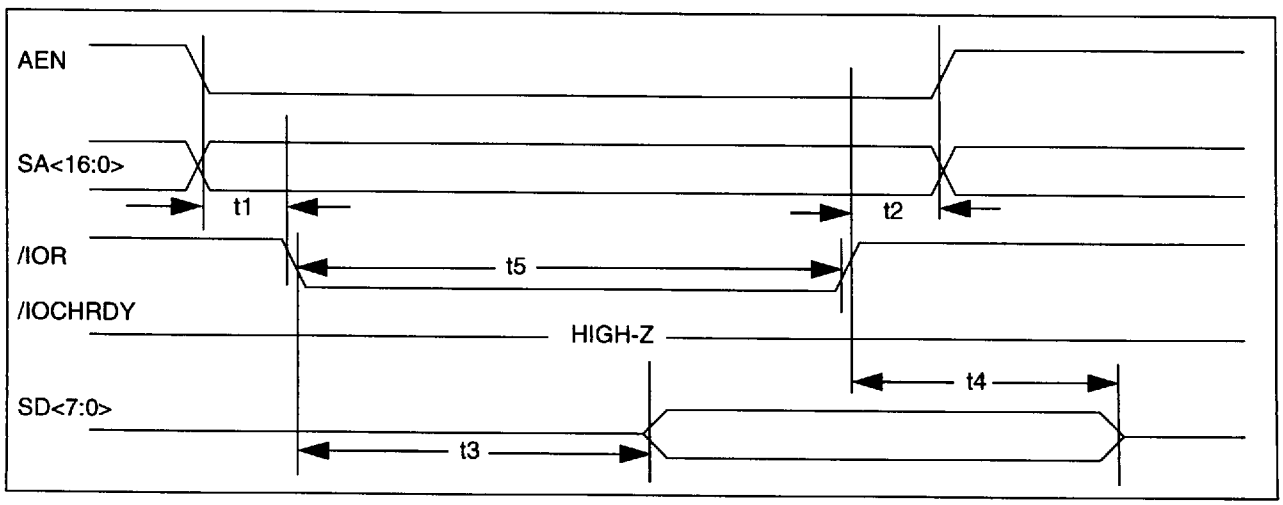
All Specifications are Valid Over the Recommended Operating Conditions Unless Otherwise Noted.

Table 13. CLK Timing



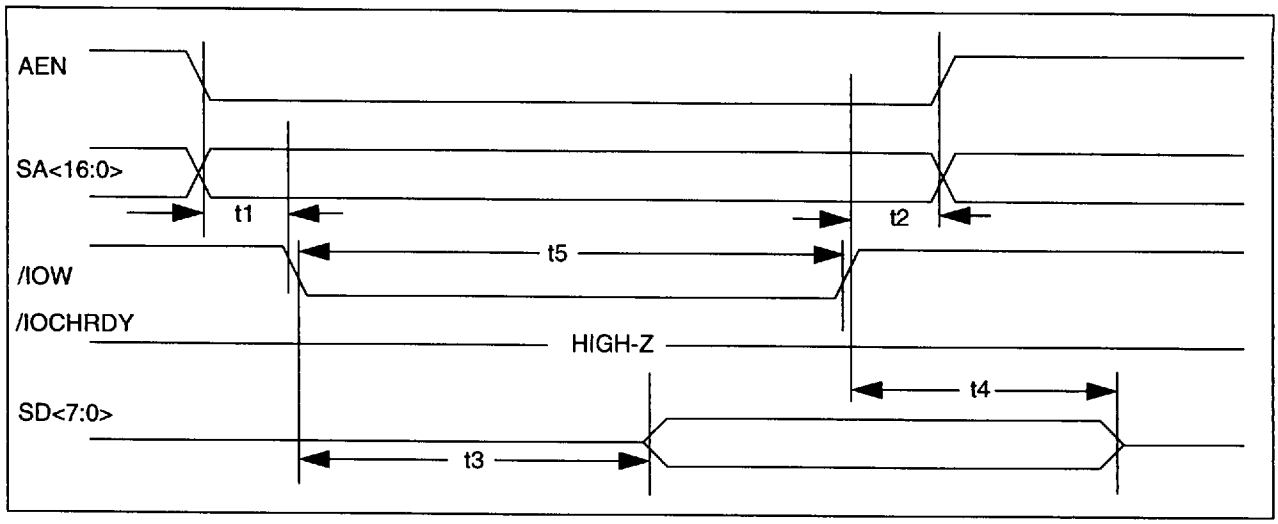
SYMBOL	PARAMETER DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNITS
t1	CLK clock period	66.7	120	166.7	ns

Table 14. Internal Register Read Cycle



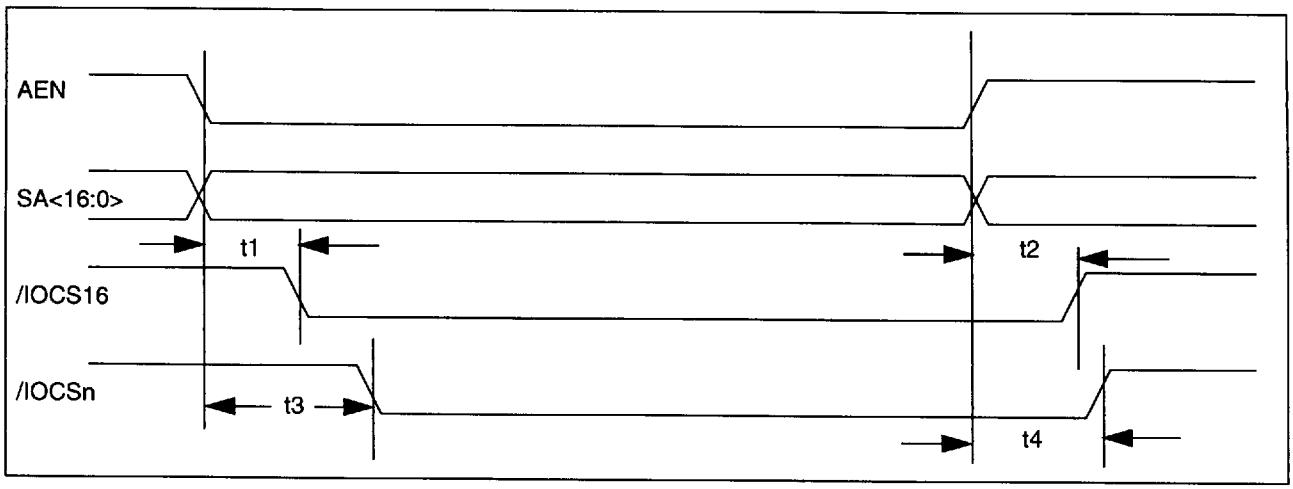
SYMBOL	PARAMETER DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNITS
t1	AEN low, SA<16:0> valid to /IOR low	89			ns
t2	/IOR high to AEN high, SA<16:0> invalid	40			ns
t3	/IOR low to SD<7:0> valid		7	20	ns
t4	/IOR high to SD<7:0>	3	7		ns
t5	/IOR low time	4			CLKs

Table 15. Internal Register Write Cycle



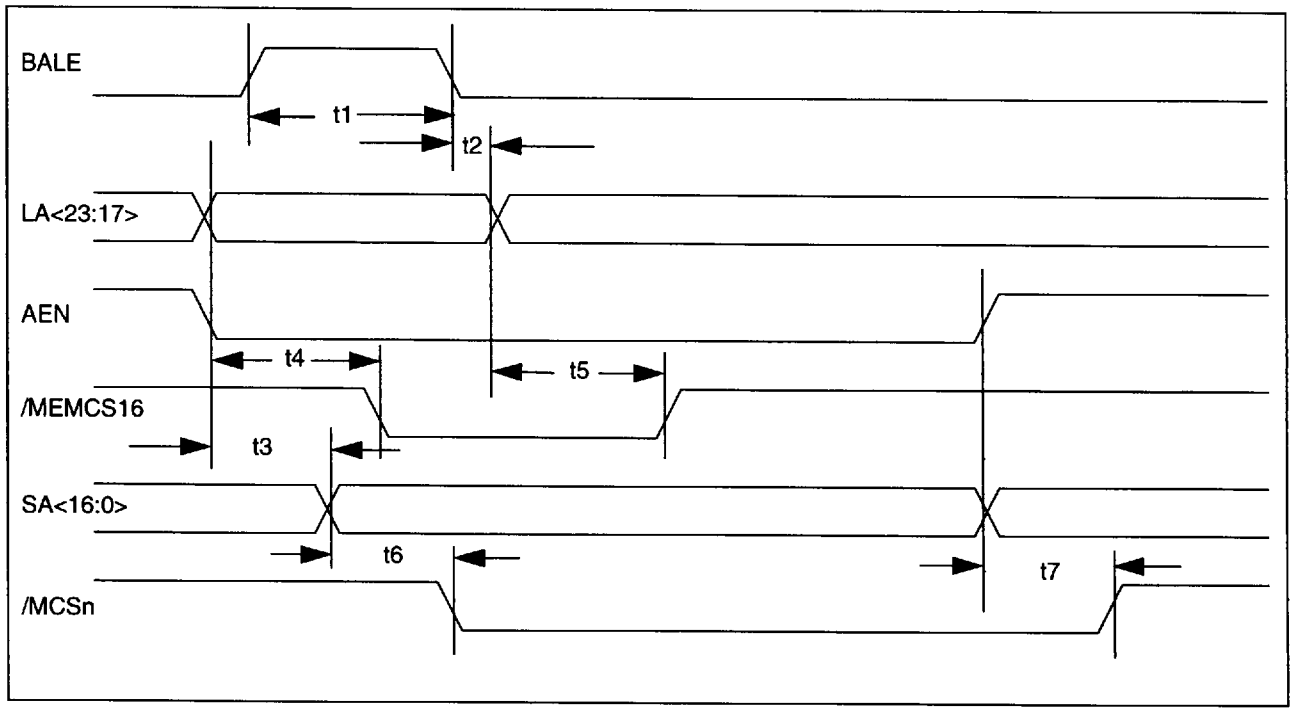
SYMBOL	PARAMETER DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNITS
t1	AEN low, SA<16:0> valid to /IOW low	89			ns
t2	/IOW high to AEN high, SA<16:0> invalid	40			ns
t3	/IOW low to SD<7:0> valid	-4			ns
t4	/IOW high to SD<7:0> invalid	0			ns
t5	/IOW low time	4			CLKs

Table 16. I/O Chip Select Generation Cycle



SYMBOL	PARAMETER DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNITS
t1	AEN low, SA<16:0> valid to /IOCS16 low			28	ns
t2	AEN high, SA<16:0> invalid to /IOCS16 high (depends on pull-up resistor value)	3	7		ns
t3	AEN low, SA<16:0> valid to /IOCSn low		11	28	ns
t4	AEN high, SA<16:0> invalid to /IOCSn high	3	7		ns

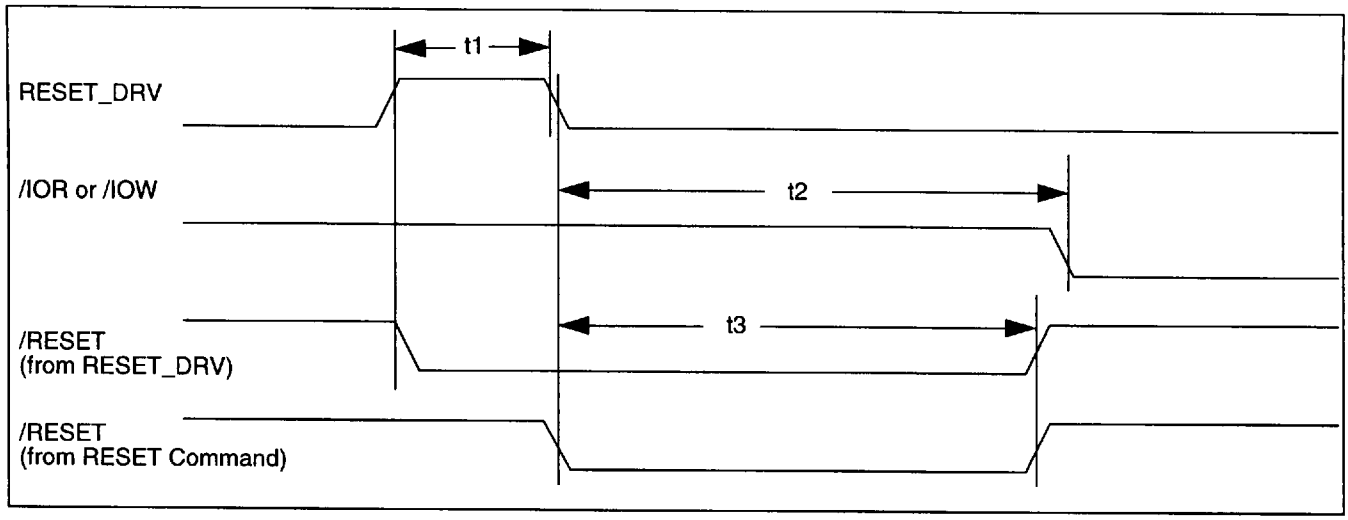
Table 17. Memory Chip Select Generation Cycle (Memory Mode Only)



Note: /MCSn generation is conditional by AEN low only if EEPROM 0x003<2> or 0x008<2> is programmed to a "1".

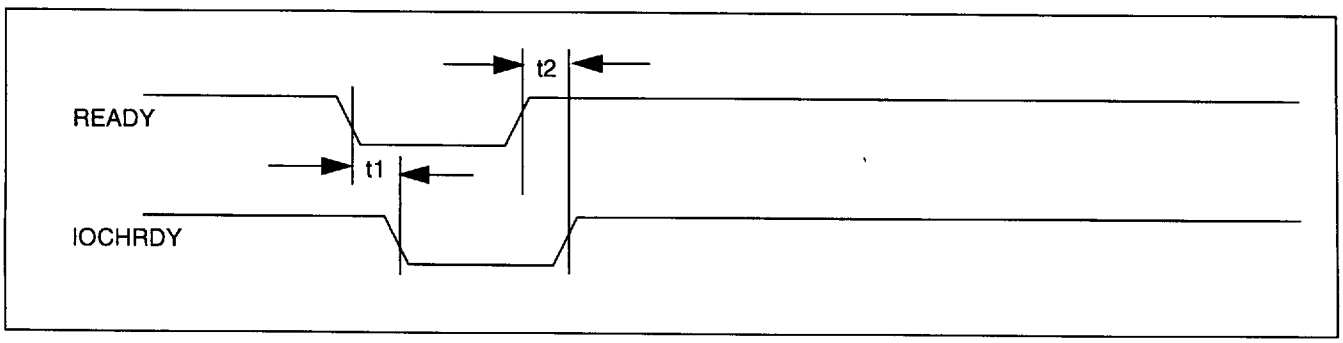
SYMBOL	PARAMETER DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UN
t1	BALE pulse width	48			ns
t2	BALE low to LA<23:17> invalid	15			ns
t3	AEN low, LA<23:17> valid to SA<16:0> valid	0			ns
t4	LA<23:17> valid to /MEMCS16 low		8	18	ns
t5	LA<23:17> invalid to /MEMCS16 high (depends on pull-up resistor value)	3	8		ns
t6	SA<16:0> valid to /MCSn low		12	30	ns
t7	AEN high, SA<16:0> invalid to /MCSn high	3	10		ns

Table 18. RESET_DRV Timing

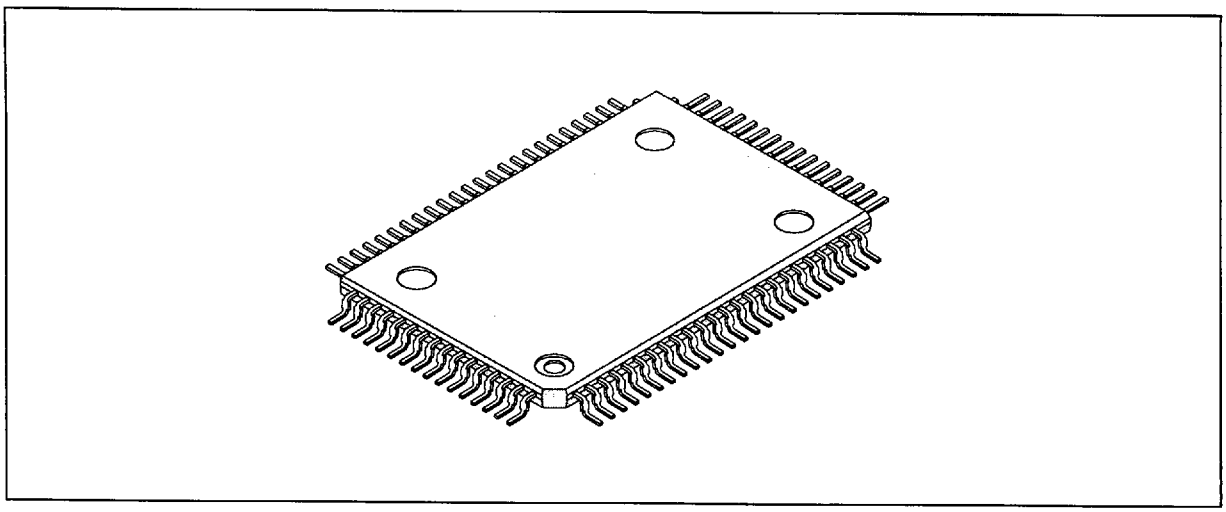


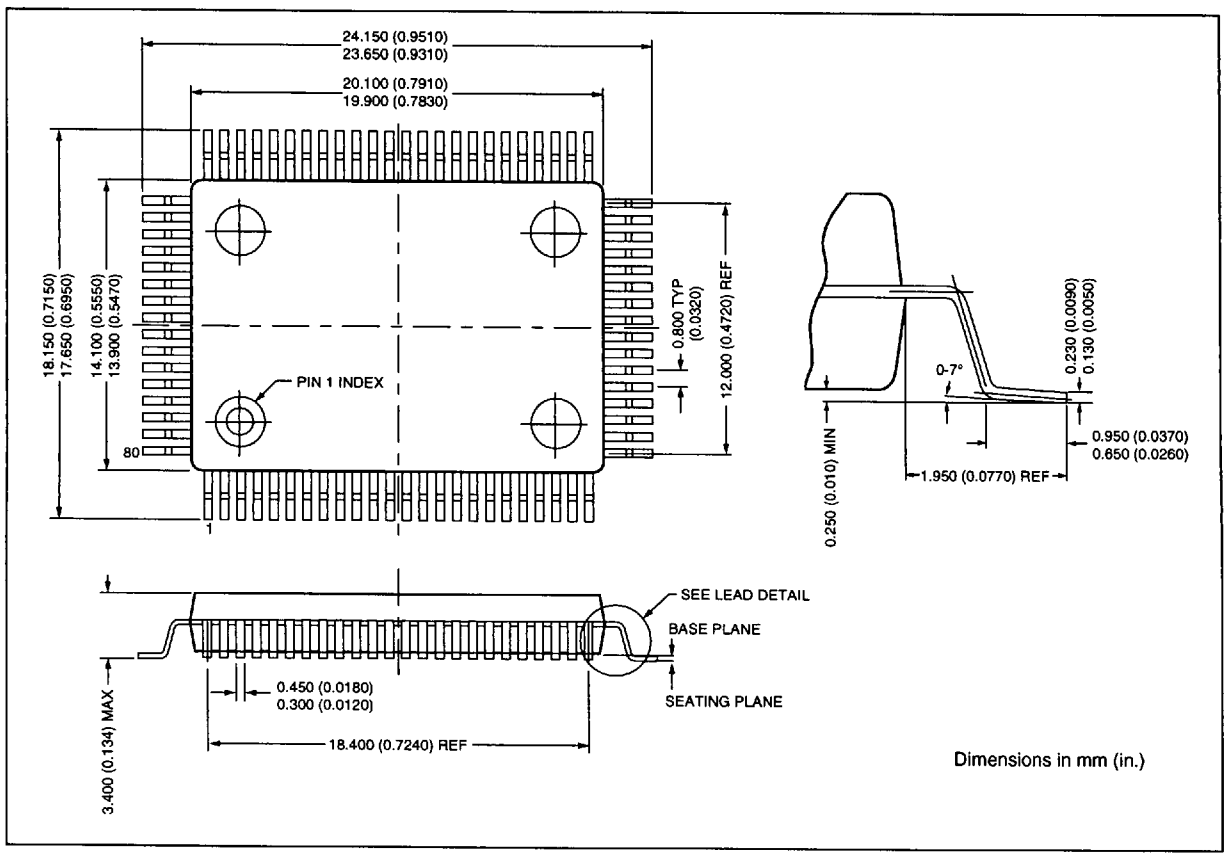
SYMBOL	PARAMETER DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNITS
t1	RESET_DRV pulse width	4			CLKs
t2	RESET_DRV low to first /IOR or /IOW low for an internal MB86703 register	1,000			us
t3	/RESET output pulse width		8816		CLKs

Table 19. IOCHRDY Timing



SYMBOL	PARAMETER DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNITS
t1	READY low to IOCHRDY low		8	16	ns
t2	READY high to IOCHRDY high (depends on pull-up resistor value)		8	16	ns




24.150 (0.9510)
23.650 (0.9310)
20.100 (0.7910)
19.900 (0.7830)
18.150 (0.7150)
17.650 (0.6950)
14.100 (0.5550)
13.900 (0.5470)
PIN 1 INDEX
80
1
0.800 TYP
(0.0320)
12.000 (0.4720) REF
0-7°
0.230 (0.0090)
0.130 (0.0050)
0.950 (0.0370)
0.650 (0.0260)
1.950 (0.0770) REF
0.250 (0.010) MIN
SEE LEAD DETAIL
BASE PLANE
SEATING PLANE
0.450 (0.0180)
0.300 (0.0120)
18.400 (0.7240) REF
3.400 (0.134) MAX
Dimensions in mm (in.)

NOTES:

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DS-20032-3/96