Features

- **Fast Read Access Time - 45 ns**
- **Low-Power CMOS Operation**
  - **100 µA max. Standby**
  - **25 mA max. Active at 5 MHz (FT27C010L)**
  - **35 mA max. Active at 5 MHz (FT27C010)**
- **JEDEC Standard Packages**
  - **32-Lead CDIL/LCC/JLCC +Custom Ceramic packages**

- **5V ± 10% Supply**
- **High Reliability CMOS Technology**
  - **2000V ESD Protection**
  - **200 mA Latchup Immunity**
- **Programming Algorithm - 100 µs/byte (typical)**
- **CMOS and TTL Compatible Inputs and Outputs**
- **Integrated Product Identification Code**
- **Commercial, Industrial and Automotive Temperature Ranges. MILITARY-Contact sales**

1-Megabit (128K x 8) UVEPROM

FT27C010(L)

Description

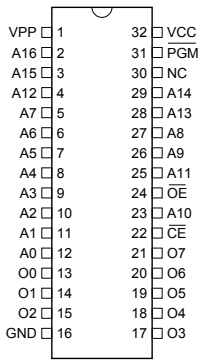
The FT27C010(L) is a low-power, high-performance 1,048,576-bit UV erase/programmable read only memory (UVEPROM) organised as 128K by 8 bits. They require only one 5V power supply in normal read mode operation. Any byte can be accessed in less than 45 ns, eliminating the need for speed reducing WAIT states on high-performance microprocessor systems.

Two power versions are offered. In read mode, the FT27C010 typically consumes 25 mA while the FT27C010L requires only 8 mA. Standby mode supply current for both parts is typically less than 10 µA.

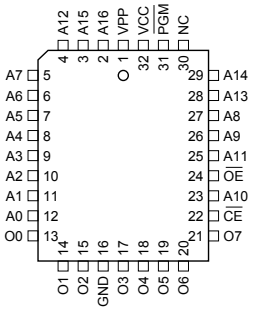
Pin Configurations

Pin Name	Function
A0 - A16	Addresses
O0 - O7	Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{PGM}$	Program Strobe
NC	No Connect

CDIL Top View



CLCC/JLCC Top View



The FT27C010(L) in available in a industry standard JEDEC-approved programmable (UVerasable) Ceramic DIl, LCC, packages. All devices feature two line control ($\overline{CE}$, $\overline{OE}$) to give designers the flexibility to prevent bus contention.

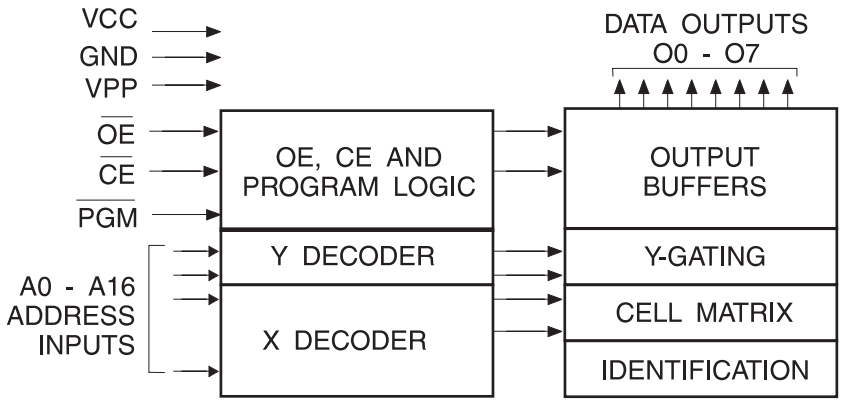
With 128K byte storage capability, the FT27C010(L) allows firmware to be stored reliably and to be accessed by the system without the delays of mass storage media.

Force FT27C010(L) have additional features to ensure high quality and efficient production use. The Programming Algorithm reduces the time required to program the part and guarantees reliable programming. Programming time is typically only 100 µs/byte. The Integrated Product Identification Code electronically identifies the device and manufacturer. This feature is used by industry standard programming equipment to select the proper programming algorithms and voltages.

System Considerations

Switching between active and standby conditions via the Chip Enable pin may produce transient voltage excursions. Unless accommodated by the system design, these transients may exceed data sheet limits, resulting in device non-conformance. At a minimum, a 0.1 µF high frequency, low inherent inductance, ceramic capacitor should be utilised for each device. This capacitor should be connected between the V_{CC} and Ground terminals of the device, as close to the device as possible. Additionally, to stabilise the supply voltage level on printed circuit boards with large EPROM arrays, a 4.7 µF bulk electrolytic capacitor should be utilised, again connected between the V_{CC} and Ground terminals. This capacitor should be positioned as close as possible to the point where the power supply is connected to the array.

Block Diagram



Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-2.0V to +7.0V(1)
Voltage on A9 with Respect to Ground	-2.0V to +14.0V(1)
V_{PP} Supply Voltage with Respect to Ground	-2.0V to +14.0V(1)

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: 1. Minimum voltage is -0.6V dc which may undershoot to -2.0V for pulses of less than 20 ns. Maximum output pin voltage is V_{CC} + 0.75V dc which may overshoot to +7.0 volts for pulses of less than 20 ns.

Operating Modes

Mode\Pin	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	Ai	V_{PP}	Outputs
Read	V_{IL}	V_{IL}	X(1)	Ai	X	D_{OUT}
Output Disable	X	V_{IH}	X	X	X	High Z
Standby	V_{IH}	X	X	X	X	High Z
Rapid Program(2)	V_{IL}	V_{IH}	V_{IL}	Ai	V_{PP}	D_{IN}
PGM Verify	V_{IL}	V_{IL}	V_{IH}	Ai	V_{PP}	D_{OUT}
PGM Inhibit	V_{IH}	X	X	X	V_{PP}	High Z
Product Identification(4)	V_{IL}	V_{IL}	X	A9 = V_H(3) A0 = V_{IH} or V_{IL} A1 - A16 = V_{IL}	X	Identification Code

Notes: 1. X can be V_{IL} or V_{IH}.
2. Refer to Programming Characteristics
3. V_H = 12.0 ± 0.5V.
4. Two identifier bytes may be selected. All Ai inputs are held low (V_{IL}), except A9 which is set to V_H and A0 which is toggled low (V_{IL}) to select the Manufacturer's Identification byte and high (V_{IH}) to select the Device Code byte.

DC and AC Operating Conditions for Read Operation

		FT27C010/FT27C010L					
		-45	-55	-70	-90	-12	-15
Operating Temp. (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
	Auto.				-40°C - 125°C	-40°C - 125°C	-40°C - 125°C
V_{CC} Power Supply		5V ± 10%	5V ± 10%	5V ± 10%	5V ± 10%	5V ± 10%	5V ± 10%

DC and Operating Characteristics for Read Operation

Symbol	Parameter	Condition		Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = 0V to V_{CC}	Com., Ind.		± 1	µA
			Auto.		± 5	µA
I_{LO}	Output Leakage Current	V_{OUT} = 0V to V_{CC}	Com., Ind.		± 5	µA
			Auto.		±10	µA
IPP1[2]	V_{PP}[1]) Read/Standby Current	V_{PP} = V_{CC}			10	µA
I_{SB}	V_{CC}[1] Standby Current	I_{SB1} (CMOS), $\overline{CE}$ = V_{CC} ± 0.3V			100	µA
		I_{SB2} (TTL), $\overline{CE}$ = 2.0 to V_{CC} + 0.5V			1	mA
I_{CC}	V_{CC} Active Current	f = 5 MHz, I_{OUT} = 0 mA, $\overline{CE}$ = V_{IL}	AT27C010(L)		25	mA
			AT27C010		35	mA
V_{IL}	Input Low Voltage			-0.6	0.8	V
V_{IH}	Input High Voltage			2.0	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA			0.4	V
V_{OH}	Output High Voltage	I_{OH} = -400 µA		2.4		V

Notes: 1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.

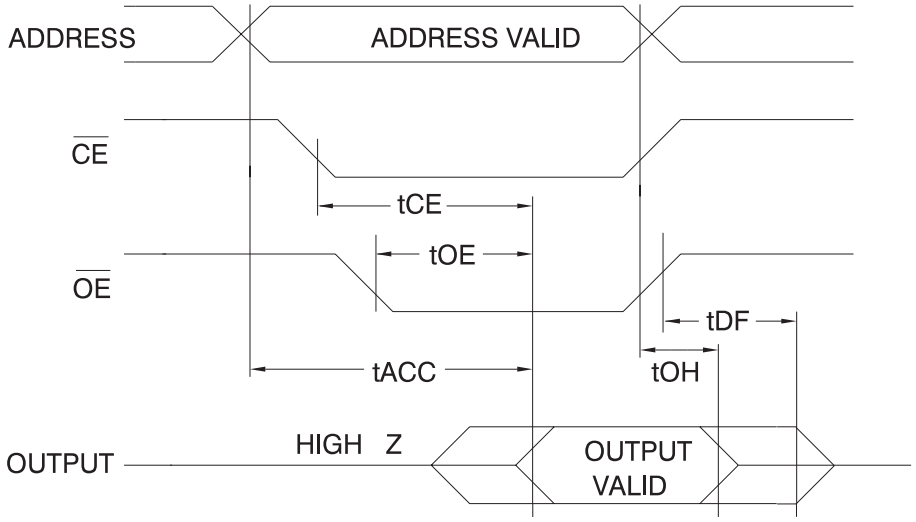
2. V_{PP} may be connected directly to V_{CC}, except during programming. The supply current would then be the sum of I_{CC} and I_{PP}.

AC Characteristics for Read Operation

			FT27C010/FT27C010L												
			-45		-55		-70		-90		-12		-15		
Symbol	Parameter	Condition	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Units
t_{ACC}[3]	Address to Output Delay	$\overline{CE}$ = $\overline{OE}$ = V_{IL}		45		55		70		90		120		150	ns
t_{CE}[2]	$\overline{CE}$ to Output Delay	$\overline{OE}$ = V_{IL}		45		55		70		90		120		150	ns
t_{OE}[2][3]	$\overline{OE}$ to Output Delay	$\overline{CE}$ = V_{IL}		20		25		30		35		35		40	ns
t_{DF}[4][5]	$\overline{OE}$ or $\overline{CE}$ High to Output Float, whichever occurred first			20		20		25		25		30		35	ns
t_{OH}	Output Hold from Address, $\overline{CE}$ or $\overline{OE}$, whichever occurred first		7		7		7		0		0		0		ns

Notes: 2,3,4,5. - see AC Waveforms for Read Operation.

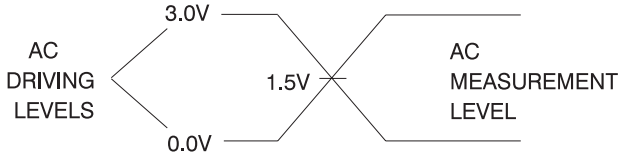
AC Waveforms for Read Operation(1)



Notes:
1. Timing measurement reference level is 1.5V for -45 and -55 devices. Input AC drive levels are V_{IL} = 0.0V and V_{IH} = 3.0V. Timing measurement reference levels for all other speed grades are V_{OL} = 0.8V and V_{OH} = 2.0V. Input AC drive levels are V_{IL} = 0.45V and V_{IH} = 2.4V.
2. $\overline{OE}$ may be delayed up to t_{CE} - t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE}.
3. $\overline{OE}$ may be delayed up to t_{ACC} - t_{OE} after the address is valid without impact on t_{ACC}.
4. This parameter is only sampled and is not 100% tested.
5. Output float is defined as the point when data is no longer driven.

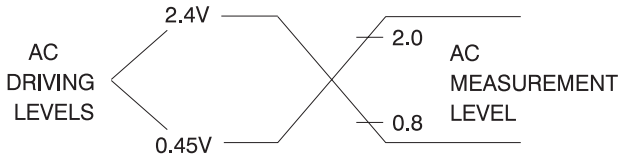
Input Test Waveforms and Measurement Levels

For -45 and -55 devices only:



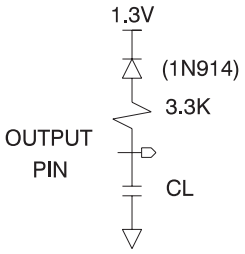
t_R, t_F < 5 ns (10% to 90%)

For -70, -90, -12, -15, and -20 devices:



t_R, t_F < 20 ns (10% to 90%)

Output Test Load



Note: C_L = 100 pF including jig capacitance, except for the -45 and -55 devices, where C_L = 30 pF.

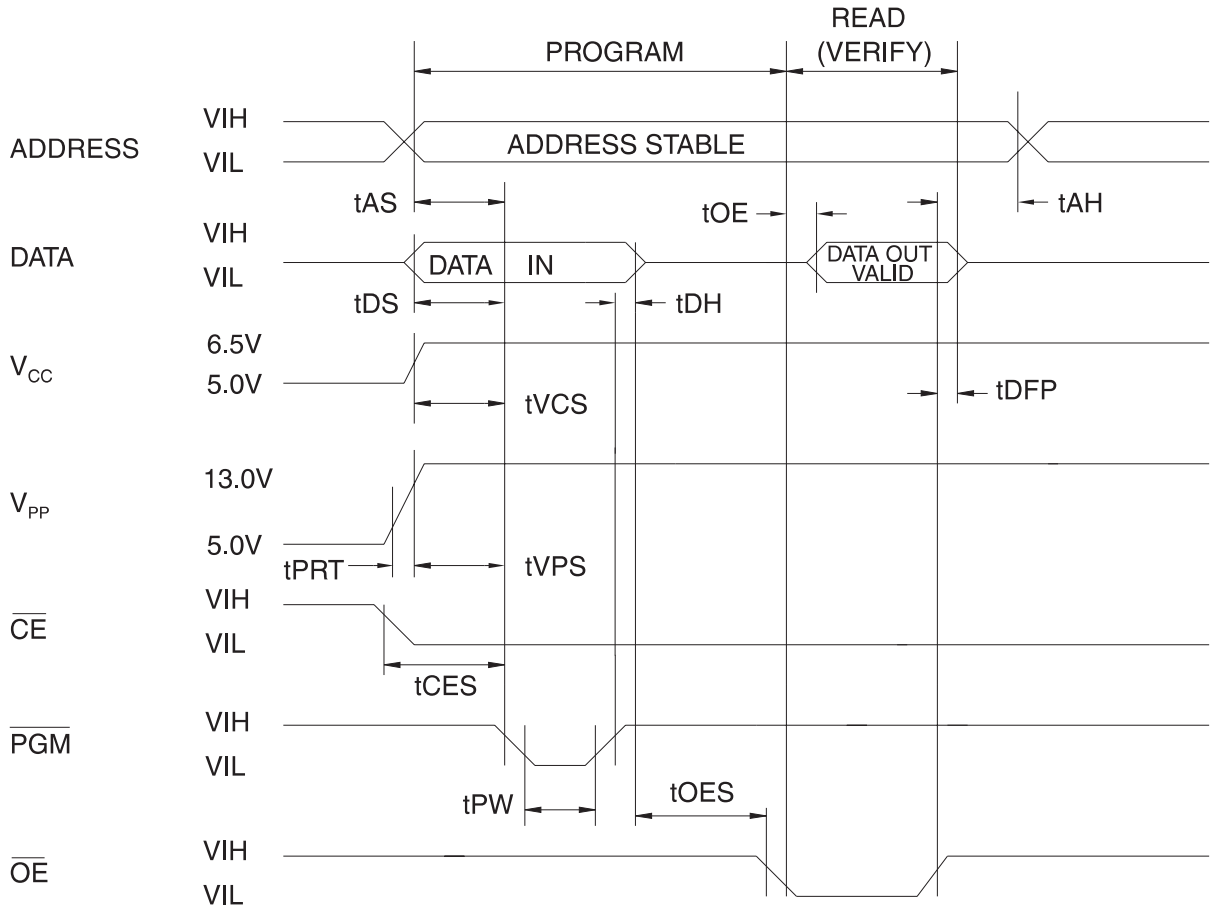
Pin Capacitance

f = 1 MHz, T = 25°C(1)

Symbol	Typ	Max	Units	Conditions
C_{IN}	4	8	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

Note: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

Programming Waveforms[1]



Notes:
1. The Input Timing Reference is 0.8V for V_{IL} and 2.0V for V_{IH}.
2. t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.
3. When programming the FT27C010(L) at 0.1 µF capacitor is required across V_{PP} and ground to suppress spurious voltage transients.

DC Programming Characteristics

T_A = 25 ± 5°C, V_{CC} = 6.5 ± 0.25V, V_{PP} = 13.0 ± 0.25V

Symbol	Parameter	Test Conditions	Limits		Units
			Min	Max	
I_{LI}	Input Load Current	$V_{IN} = V_{IL}, V_{IH}$		±10	µA
V_{IL}	Input Low Level		-0.6	0.8	V
V_{IH}	Input High Level		2.0	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = -400 µA	2.4		V
I_{CC2}	V_{CC} Supply Current (Program and Verify)			40	mA
I_{PP2}	V_{PP} Supply Current	$\overline{CE} = \overline{PGM} = V_{IL}$		20	mA
V_{ID}	A9 Product Identification Voltage		11.5	12.5	V

AC Programming Characteristics

T_A = 25 ± 5°C, V_{CC} = 6.5 ± 0.25 V, V_{PP} = 13.0 ± 0.25V

Symbol	Parameter	Test Conditions[1]	Limits		Units
			Min	Max	
t_{AS}	Address Setup Time	Input Rise and Fall Times (10% to 90%) 20ns Input Pulse Levels 0.45V to 2.4V Input Timing Reference Level 0.8V to 2.0V Output Timing Reference Level 0.8V to 2.0V	2		µs
t_{CES}	$\overline{CE}$ Setup Time		2		µs
t_{OES}	$\overline{OE}$ Setup Time		2		µs
t_{DS}	Data Setup Time		2		µs
t_{AH}	Address Hold Time		0		µs
t_{DH}	Data Hold Time		2		µs
t_{DFP}	$\overline{OE}$ High to Output Float Delay[2]		0	130	ns
t_{VPS}	V_{PP} Setup Time		2		µs
t_{VCS}	V_{CC} Setup Time		2		µs
t_{PW}	$\overline{PGM}$ Program Pulse Width[3]		95	105	µs
t_{OE}	Data Valid from $\overline{OE}$			150	ns
t_{PRT}	V_{PP} Pulse Rise TIme During Programming		50		ns

Notes: 1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.

2. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven—see timing diagram.

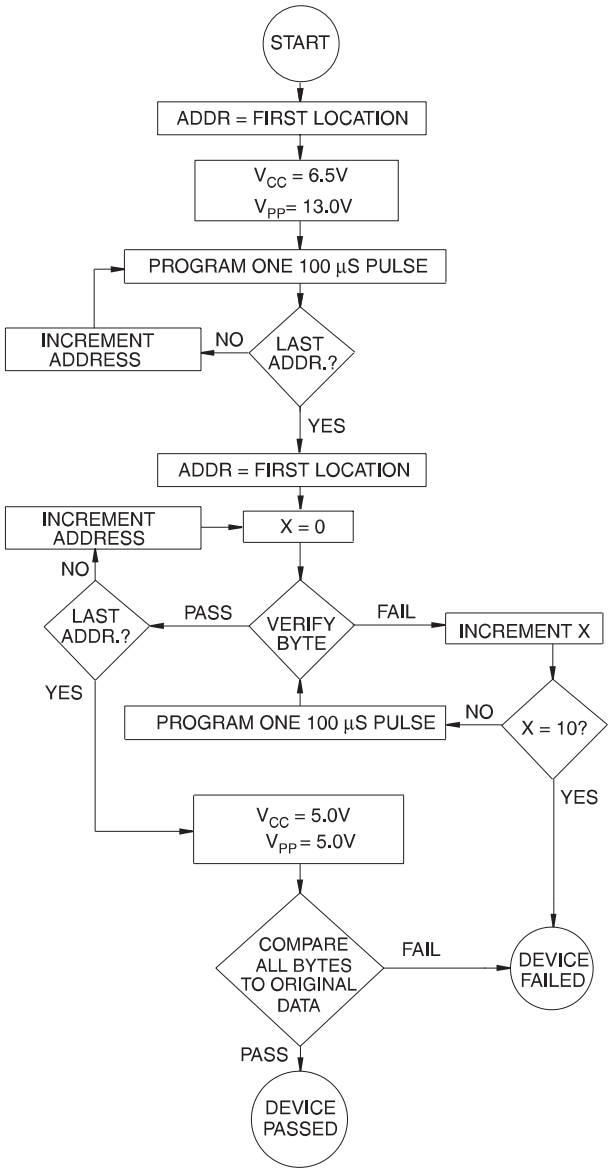
3. Program Pulse width tolerance is 100 µsec ± 5%.

Force 27C010(L) uses Integrated Product Identification Code

Codes	Pins									Hex Data
	A0	O7	O6	O5	O4	O3	O2	O1	O0	
Manufacturer	0	0	0	0	1	1	1	1	0	1E
Device ype T	1	0	0	0	0	0	1	0	1	05

Rapid Programming Algorithm

A 100 µs $\overline{PGM}$ pulse width is used to program. The address is set to the first location. V_{CC} is raised to 6.5V and V_{PP} is raised to 13.0V. Each address is first programmed with one 100 µs $\overline{PGM}$ pulse without verification. Then a verification / reprogramming loop is executed for each address. In the event a byte fails to pass verification, up to 10 successive 100 µs pulses are applied with a verification after each pulse. If the byte fails to verify after 10 pulses have been applied, the part is considered failed. After the byte verifies properly, the next address is selected until all have been checked. V_{PP} is then lowered to 5.0V and V_{CC} to 5.0V. All bytes are read again and compared with the original data to determine if the device passes or fails.



FT27C010 Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
45	35	0.1	FT27C010-45DC FT27C010-45LC	CDIL LCC	Commercial (0°C to 70°C)
	35	0.1	FT27C010-45DI FT27C010-45LI	CDIL LCC	Industrial (-40°C to 85°C)
55	35	0.1	FT27C010-55DC FT27C010-55LC	CDIL LCC	Commercial (0°C to 70°C)
	35	0.1	FT27C010-55DI FT27C010-55LI	CDIL LCC	Industrial (-40°C to 85°C)
70	35	0.1	FT27C010-70DC FT27C010-70LC	CDIL LCC	Commercial (0°C to 70°C)
	35	0.1	FT27C010-70DI FT27C010-70LI	CDIL LCC	Industrial (-40°C to 85°C)

(continued)

Package Type	
LCC	**32-pad, Windowed Leadless Chip Carrier (LCC)**
CDIL	**32-Lead, 0.600" Wide, Ceramic Windowed Dual Inline Package (CDIL)**

FT27C010 Ordering Information (Continued)

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
90	35	0.1	FT27C010-90DC FT27C010-90LC	CDIL LCC	Commercial (0°C to 70°C)
	35	0.1	FT27C010-90DI FT27C010-90LI	CDIL LCC	Industrial (-40°C to 85°C)
	35	0.1	FT27C010-90DA FT27C010-90LA/KA	CDIL/LCC/JLCC	Automotive (-40°C to 125°C)
120	35	0.1	FT27C010-12DC FT27C010-12LC	CDIL LCC	Commercial (0°C to 70°C)
	35	0.1	FT27C010-12DI FT27C010-12LI	LCC	Industrial (-40°C to 85°C)
	35	0.1	FT27C010-12DA FT27C010-12LA	CDIL LCC	Automotive (-40°C to 125°C)
150	35	0.1	FT27C010-15DC FT27C010-15LC	CDIL LCC	Commercial (0°C to 70°C)
	35	0.1	FT27C010-15DI FT27C010-15LI	CDIL LCC	Industrial (-40°C to 85°C)
	35	0.1	FT27C010-15JA FT27C010-15LA/KA	CDIL LCC/JLCC	Automotive (-40°C to 125°C)

Package Type	
LCC	**32-pad, Windowed Leadless Chip Carrier (LCC)**
CDIL	**32-Lead, 0.600" Wide, Ceramic Dual Inline Package (CDIL)**
JLCC	**32-Lead, Windowed J Leaded Chip Carrier (JLCC)**

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