GeneSiC SEMICONDUCTOR

2N7639-GA

Normally – OFF Silicon Carbide Junction Transistor

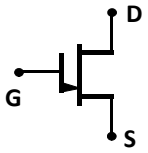
V_{DS}	=	600 V
$R_{DS(ON)}$	=	65 mΩ
$I_{D\ (Tc = 25°C)}$	=	32 A
$h_{FE\ (Tc = 25°C)}$	=	110

Features

- 225°C maximum operating temperature
- Electrically Isolated Base Plate
- Gate Oxide Free SiC Switch
- Exceptional Safe Operating Area
- Excellent Gain Linearity
- Temperature Independent Switching Performance
- Low Output Capacitance
- Positive Temperature Coefficient of $R_{DS,ON}$
- Suitable for Connecting an Anti-parallel Diode

Package

- RoHS Compliant



TO – 257 (Isolated Base-plate Hermetic Package)

Advantages

- Compatible with Si MOSFET/IGBT Gate Drive ICs
- > 20 µs Short-Circuit Withstand Capability
- Lowest-in-class Conduction Losses
- High Circuit Efficiency
- Minimal Input Signal Distortion
- High Amplifier Bandwidth

Applications

- Down Hole Oil Drilling, Geothermal Instrumentation
- Hybrid Electric Vehicles (HEV)
- Solar Inverters
- Switched-Mode Power Supply (SMPS)
- Power Factor Correction (PFC)
- Induction Heating
- Uninterruptible Power Supply (UPS)
- Motor Drives

Absolute Maximum Ratings

Parameter	Symbol	Conditions	Values	Unit
Drain – Source Voltage	V_{DS}	V_{GS} = 0 V	600	V
Continuous Drain Current	I_D	T_J = 225°C, T_C = 25°C	32	A
Gate Peak Current	I_{GM}		2	A
Turn-Off Safe Operating Area	RBSOA	T_{VJ} = 225°C, I_G = 1.5 A, Clamped Inductive Load	$I_{D,max}$ = 32 @ $V_{DS} \le V_{DSmax}$	A
Short Circuit Safe Operating Area	SCSOA	T_{VJ} = 225°C, I_G = 1.5 A, V_{DS} = 400 V, Non Repetitive	>20	µs
Reverse Gate – Source Voltage	V_{GS}		30	V
Reverse Drain – Source Voltage	V_{DS}		40	V
Power Dissipation	P_{tot}	T_J = 225°C, T_C = 25°C	172	W
Operating and Storage Temperature	T_j, T_{stg}		-55 to 225	°C

Electrical Characteristics

Parameter	Symbol	Conditions	Values min.	Values typ.	Values max.	Unit
On Characteristics						
Drain – Source On Resistance	$R_{DS(ON)}$	I_D = 20 A, I_G = 400 mA, T_j = 25 °C		65		mΩ
		I_D = 20 A, I_G = 500 mA, T_j = 125 °C		90		
		I_D = 20 A, I_G = 1000 mA, T_j = 175 °C		110		
		I_D = 20 A, I_G = 1000 mA, T_j = 250 °C		165		
Gate Forward Voltage	$V_{GS(FWD)}$	I_G = 1000 mA, T_j = 25 °C		3.0		V
		I_G = 1000 mA, T_j = 250 °C		2.7		
DC Current Gain	h_{FE}	V_{DS} = 5 V, I_D = 20 A, T_j = 25 °C		112		
		V_{DS} = 5 V, I_D = 20 A, T_j = 125 °C		78		
		V_{DS} = 5 V, I_D = 20 A, T_j = 175 °C		73		
		V_{DS} = 5 V, I_D = 20 A, T_j = 250 °C		69		
Off Characteristics						
Drain Leakage Current	I_{DSS}	V_R = 600 V, V_{GS} = 0 V, T_j = 25 °C		10		µA
		V_R = 600 V, V_{GS} = 0 V, T_j = 175 °C		50		
		V_R = 600 V, V_{GS} = 0 V, T_j = 250 °C		100		
Gate Leakage Current	I_{SG}	V_{SG} = 20 V, T_j = 25 °C		20		nA

Electrical Characteristics

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Capacitance Characteristics						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_D = 100 V, f = 1 MHz		2500		pF
Reverse Transfer/Output Capacitance	C_{rss}/C_{oss}	V_D = 100 V, f = 1 MHz		158		pF
Output Capacitance Stored Energy	E_{OSS}	V_{GS} = 0 V, V_D = 100 V, *f* = 1 MHz		0.8		µJ
Switching Characteristics						
Gate Resistance, Internal	$R_{G(INT)}$	*f* = 1 MHz, V_{AC} = 25 mV, T_j = 225 ºC		2.6		Ω
Turn On Delay Time	$t_{d(on)}$	T_j = 25 ºC, V_{DS} = 400 V, I_D = 20 A, Two-Level Gate Drive, R_G = 1.53 Ω, C_G = 25 nF, V_{GH} = 18 V, V_{GL} = 6 V, V_{EE} = -10 V, IXDD614 Gate Drive IC, L = 287 uH, FWD = GB20SLT12, Refer to Fig. 15 for gate current waveform		90		ns
Rise Time	t_r			40		ns
Turn Off Delay Time	$t_{d(off)}$			50		ns
Fall Time	t_f			30		ns
Turn-On Energy Per Pulse	E_{on}			810		µJ
Turn-Off Energy Per Pulse	E_{off}			95		µJ
Total Switching Energy	E_{ts}			905		µJ
Turn On Delay Time	$t_{d(on)}$	T_j = 250 ºC, V_{DS} = 400 V, I_D = 20 A, Two-Level Gate Drive, R_G = 1.53 Ω, C_G = 25 nF, V_{GH} = 18 V, V_{GL} = 6 V, V_{EE} = -10 V, IXDD614 Gate Drive IC, L = 287 uH, FWD = GB20SLT12, Refer to Fig. 15 for gate current waveform		90		ns
Rise Time	t_r			20		ns
Turn Off Delay Time	$t_{d(off)}$			50		ns
Fall Time	t_f			20		ns
Turn-On Energy Per Pulse	E_{on}			140		µJ
Turn-Off Energy Per Pulse	E_{off}			45		µJ
Total Switching Energy	E_{ts}			185		µJ

Thermal Characteristics

Thermal resistance, junction - case	R_{thJC}			1.16		°C/W

Figures

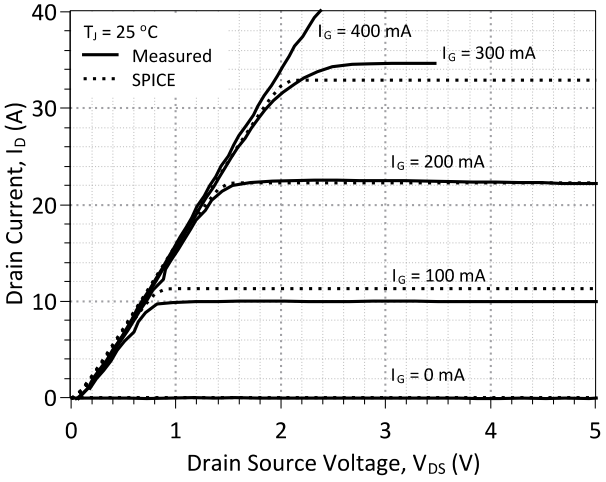


Figure 1: Typical Output Characteristics at 25 °C

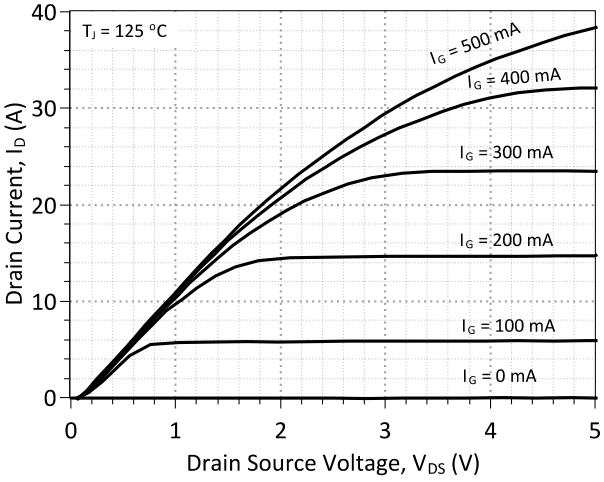


Figure 2: Typical Output Characteristics at 125 °C

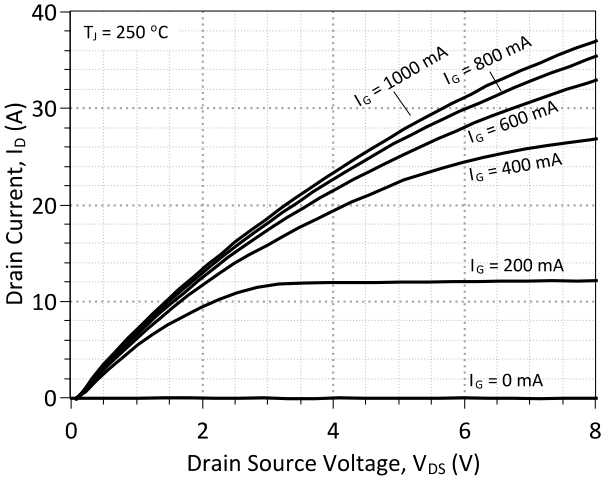


Figure 3: Typical Output Characteristics at 250 °C

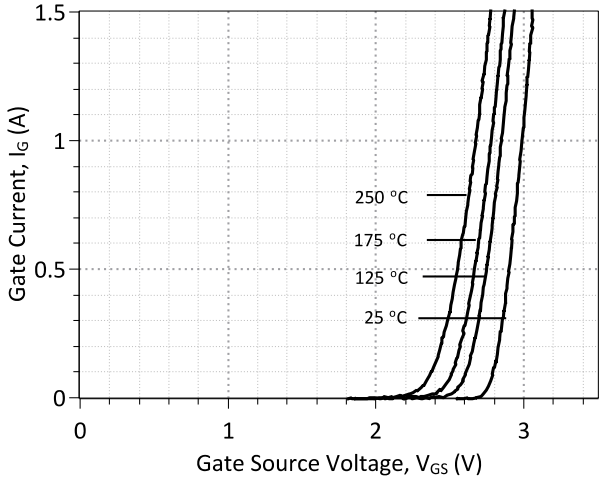


Figure 4: Typical Gate Source I-V Characteristics vs. Temperature

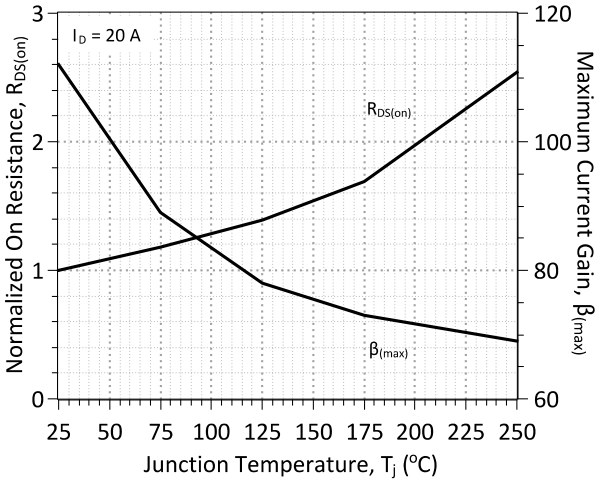


Figure 5: Normalized On-Resistance and Current Gain vs. Temperature

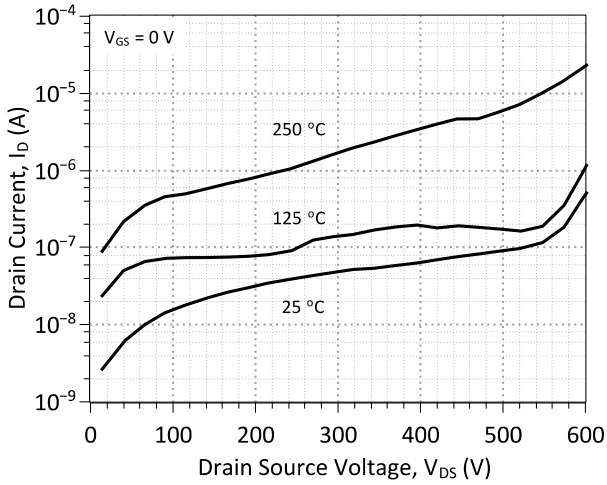


Figure 6: Typical Blocking Characteristics

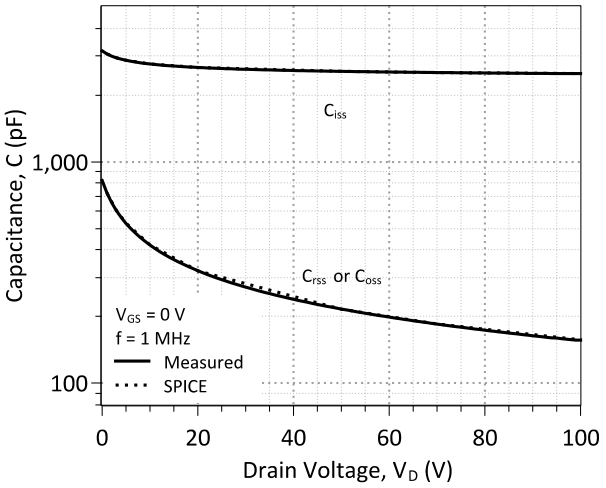


Figure 7: Capacitance Characteristics

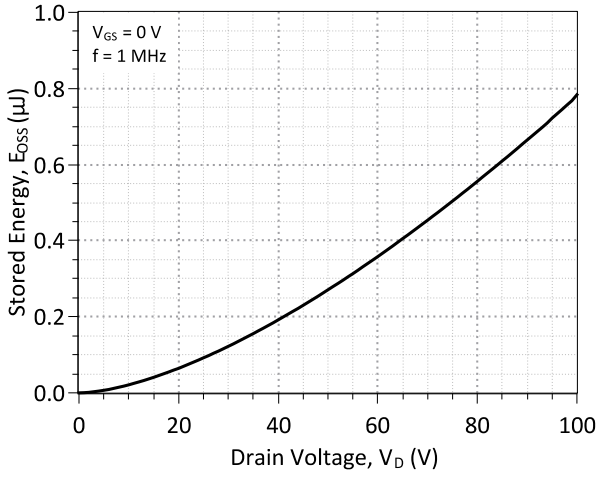


Figure 8: Output Capacitance Stored Energy

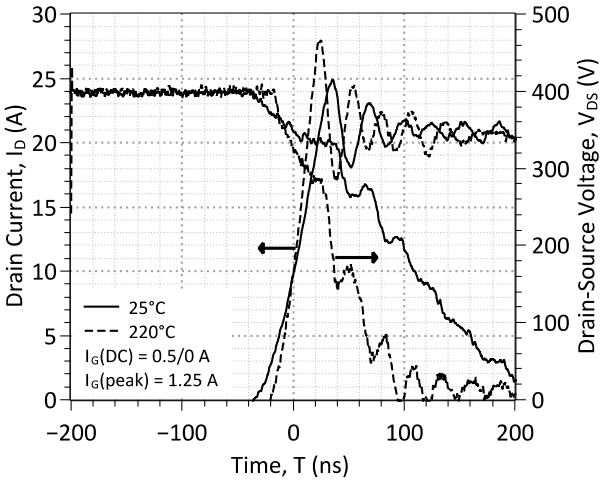


Figure 9: Typical Hard-switched Turn On Waveforms

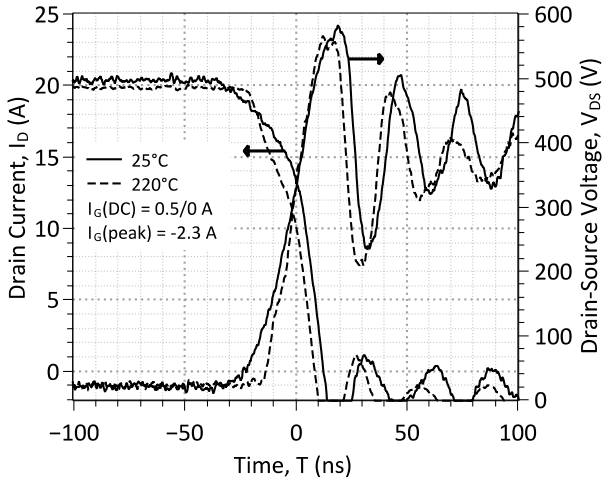


Figure 10: Typical Hard-switched Turn Off Waveforms

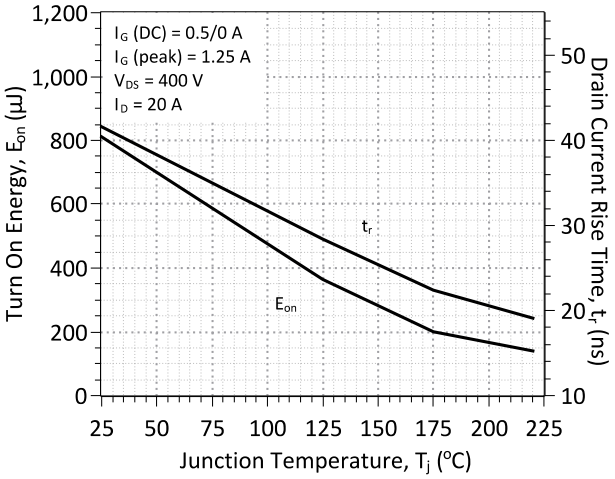


Figure 11: Typical Turn On Energy Losses and Switching Times vs. Temperature

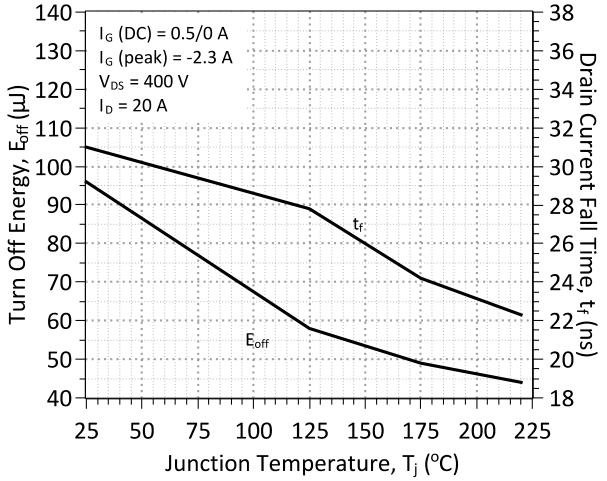


Figure 12: Typical Turn Off Energy Losses and Switching Times vs. Temperature

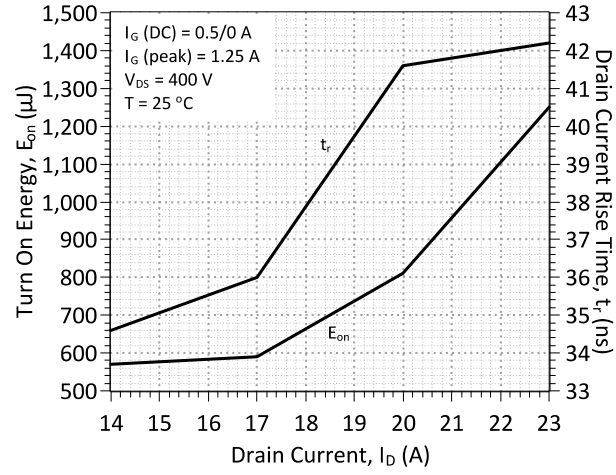


Figure 13: Typical Turn On Energy Losses and Switching Times vs. Drain Current

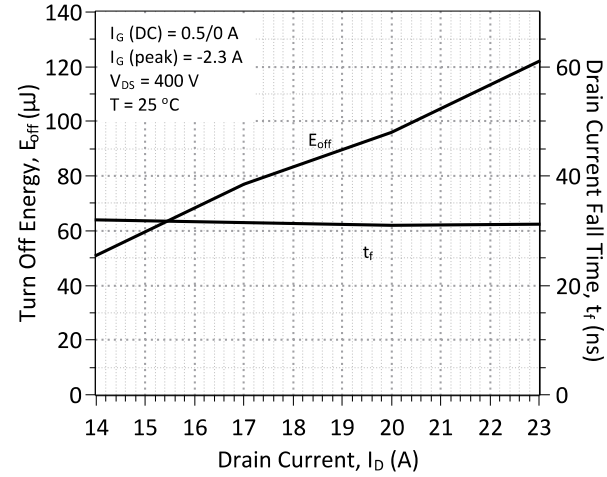


Figure 14: Typical Turn Off Energy Losses and Switching Times vs. Drain Current

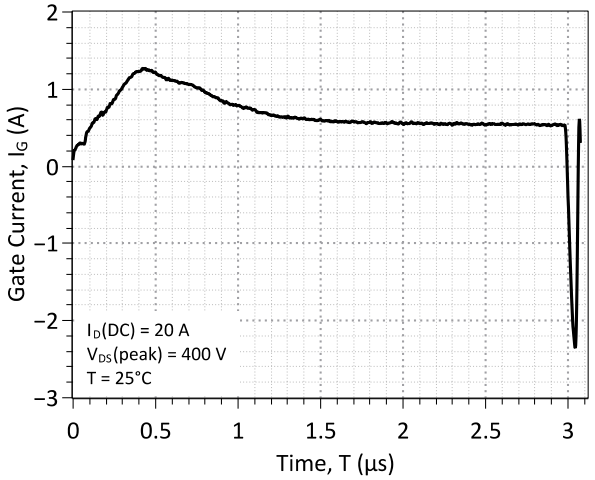


Figure 15: Typical Gate Current Waveform

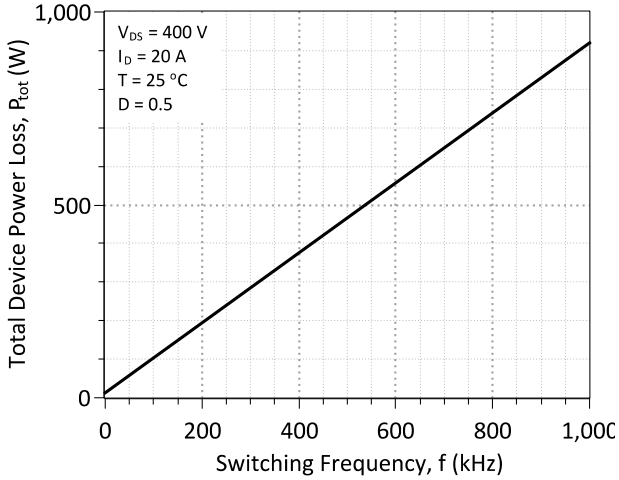


Figure 16: Typical Hard Switched Device Power Loss vs. Switching Frequency [1]

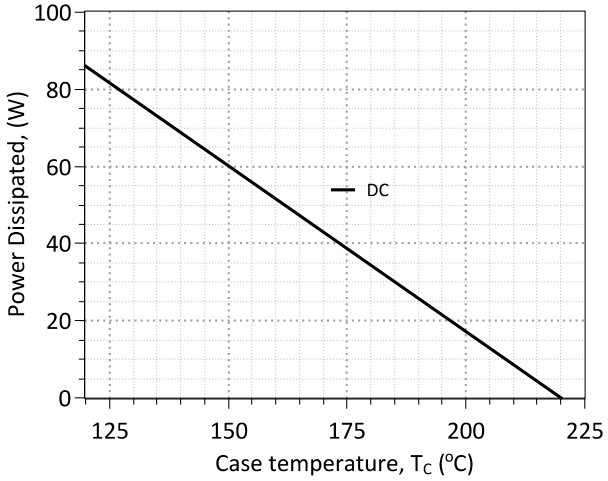


Figure 17: Power Derating Curve

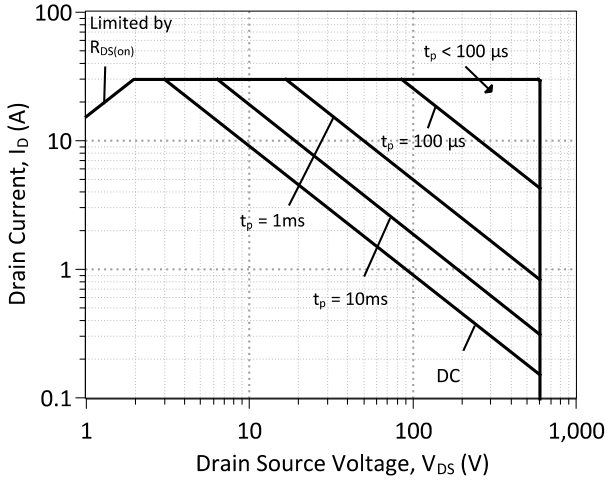


Figure 18: Forward Bias Safe Operating Area at T_c=120 °C

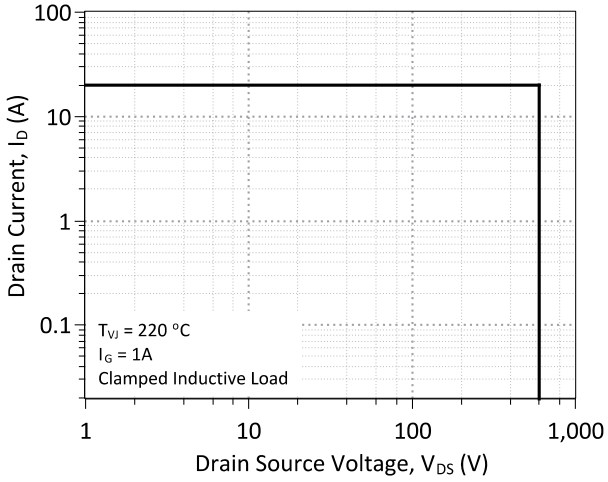


Figure 19: Turn-Off Safe Operating Area

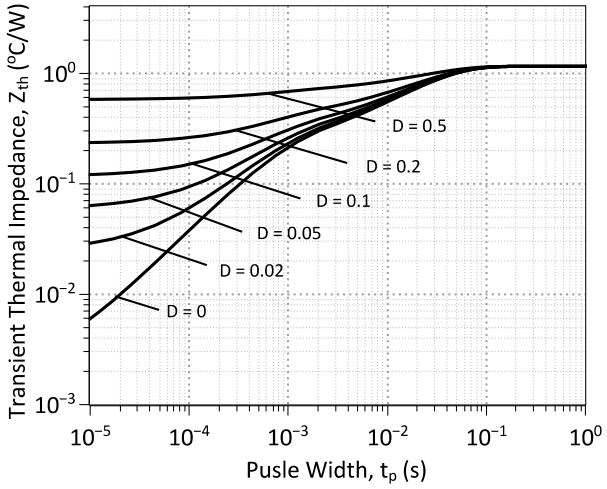


Figure 20: Transient Thermal Impedance

[1] – Representative values based on device switching energy loss. Actual losses will depend on gate drive conditions, device load, and circuit topology.

Gate Drive Theory of Operation

The SJT transistor is a current controlled transistor which requires a positive gate current for turn-on as well as to remain in on-state. An ideal gate current waveform for ultra-fast switching of the SJT, while maintaining low gate drive losses, is shown in Figure 21.

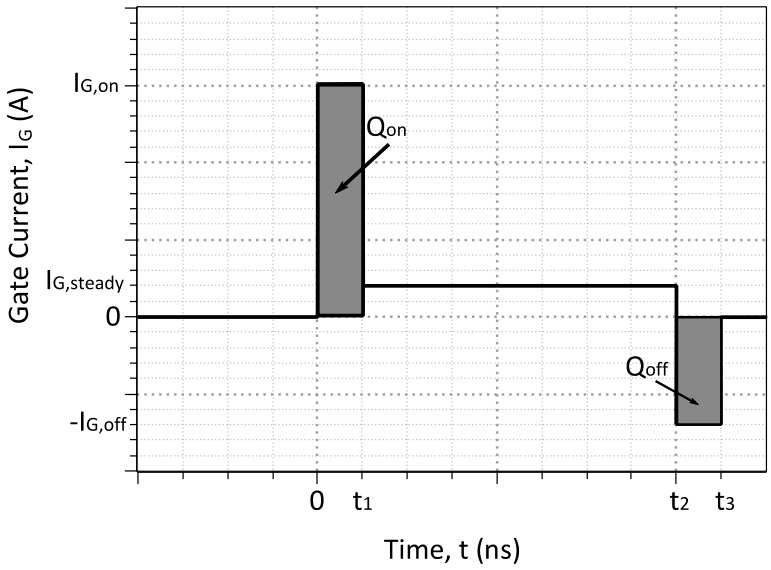


Figure 21: Idealized Gate Current Waveform

Gate Currents, $I_{G,pk}$/$-I_{G,pk}$ and Voltages during Turn-On and Turn-Off

An SJT is rapidly switched from its blocking state to on-state, when the necessary gate charge, Q_G, for turn-on is supplied by a burst of high gate current, $I_{G,on}$, until the gate-source capacitance, C_{GS}, and gate-drain capacitance, C_{GD}, are fully charged.

$$I_{G,on} * t_1 \geq Q_{gs} + Q_{gd}$$

The $I_{G,pon}$ pulse should ideally terminate, when the drain voltage falls to its on-state value, in order to avoid unnecessary drive losses during the steady on-state. In practice, the rise time of the $I_{G,on}$ pulse is affected by the parasitic inductances, L_{par} in the package and drive circuit. A voltage developed across the parasitic inductance in the source path, L_s, can de-bias the gate-source junction, when high drain currents begin to flow through the device. The applied gate voltage should be maintained high enough, above the $V_{GS,ON}$ level to counter these effects.

A high negative peak current, $-I_{G,off}$ is recommended at the start of the turn-off transition, in order to rapidly sweep out the injected carriers from the gate, and achieve rapid turn-off. While satisfactory turn off can be achieved with V_{GS} = 0 V, a negative gate voltage V_{GS} may be used in order to speed up the turn-off transition.

Steady On-State

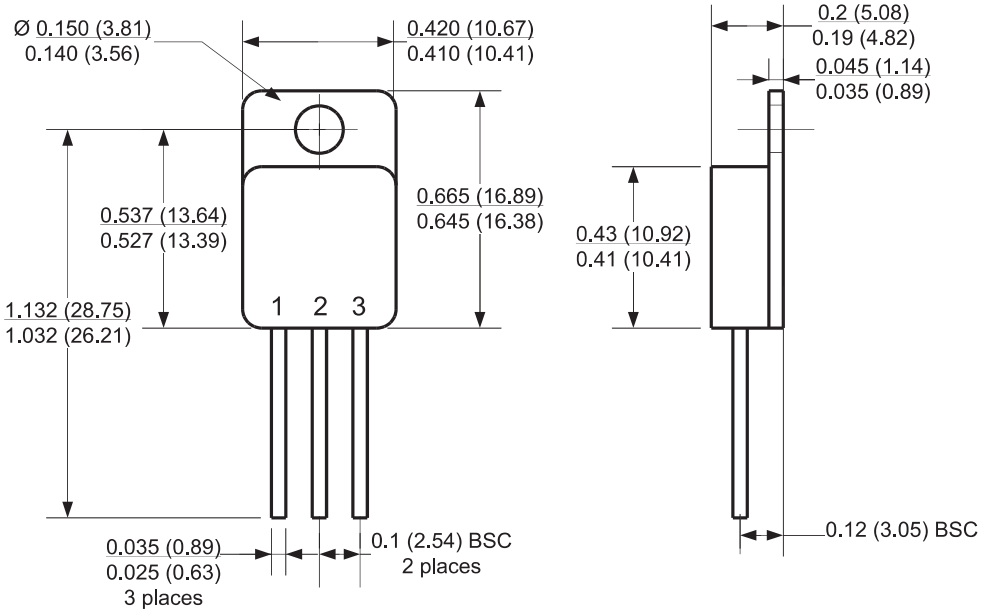
After the device is turned on, I_G may be advantageously lowered to $I_{G,steady}$ for reducing unnecessary gate drive losses. The $I_{G,steady}$ is determined by noting the DC current gain, h_{FE}, of the device.

The desired $I_{G,steady}$ is determined by the peak device junction temperature T_J during operation, drain current I_D, DC current gain h_{FE}, and a 50 % safety margin to ensure operating the device in the saturation region with low on-state voltage drop by the equation:

$$I_{G,steady} \approx \frac{I_D}{h_{FE}(T, I_D)} * 1.5$$

Package Dimensions:

TO-257 **PACKAGE OUTLINE**



NOTE
1. CONTROLLED DIMENSION IS INCH. DIMENSION IN BRACKET IS MILLIMETER.
2. DIMENSIONS DO NOT INCLUDE END FLASH, MOLD FLASH, MATERIAL PROTRUSIONS

Revision History			
Date	Revision	Comments	Supersedes
2014/08/25	6	Updated Electrical Characteristics	
2014/03/18	5	Updated Gate Drive Section	
2014/02/10	4	Updated Electrical Characteristics	
2013/12/19	3	Updated Gate Drive Section	
2013/12/09	2	Updated Electrical Characteristics	
2013/11/18	1	Updated Electrical Characteristics	
2012/08/24	0	Initial release	

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SPICE Model Parameters

This is a secure document. Please copy this code from the SPICE model PDF file on our website (http://www.genesicsemi.com/images/hit_sic/sjt/2N7639-GA_SPICE.pdf) into LTSPICE (version 4) software for simulation of the 2N7639-GA.

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*     MODEL OF GeneSiC Semiconductor Inc.
*
*     $Revision:   1.2           $
*     $Date:   23-JUN-2014       $
*
*     GeneSiC Semiconductor Inc.
*     43670 Trade Center Place Ste. 155
*     Dulles, VA 20166
*
*     COPYRIGHT (C) 2014 GeneSiC Semiconductor Inc.
*     ALL RIGHTS RESERVED
*
* These models are provided "AS IS, WHERE IS, AND WITH NO WARRANTY
* OF ANY KIND EITHER EXPRESSED OR IMPLIED, INCLUDING BUT NOT LIMITED
* TO ANY IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A
* PARTICULAR PURPOSE."
* Models accurate up to 2 times rated drain current.
*
.model 2N7639-GA NPN
+ IS       5.00E-47
+ ISE      1.26E-28
+ EG       3.23
+ BF       114
+ BR       0.55
+ IKF      700
+ NF       1
+ NE       2
+ RB       2.60
+ RE       0.01
+ RC       0.045
+ CJC      8.2281E-10
+ VJC      3.31126
+ MJC      0.48117
+ CJE      2.33957E-9
+ VJE      2.91486
+ MJE      0.48211
+ XTI      3
+ XTB      -1.2
+ TRC1     6.20E-03
+ VCEO     600
+ ICRATING 32
+ MFG      GeneSiC_Semiconductor
*
* End of 2N7639-GA SPICE Model
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