

Normally – OFF Silicon Carbide Junction Transistor

| | | |
|---------------------------------------|---|--------|
| V_{DS} | = | 600 V |
| $R_{DS(ON)}$ | = | 425 mΩ |
| I_D ($T_C = 25^\circ\text{C}$) | = | 10 A |
| h_{FE} ($T_C = 25^\circ\text{C}$) | = | 110 |

Features

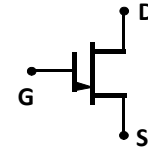
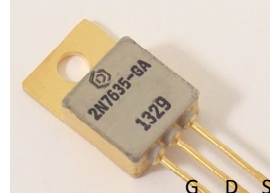
- 225°C maximum operating temperature
- Electrically Isolated Base Plate
- Gate Oxide Free SiC Switch
- Exceptional Safe Operating Area
- Excellent Gain Linearity
- Temperature Independent Switching Performance
- Low Output Capacitance
- Positive Temperature Coefficient of $R_{DS,ON}$
- Suitable for Connecting an Anti-parallel Diode

Advantages

- Compatible with Si MOSFET/IGBT Gate Drive ICs
- > 20 μs Short-Circuit Withstand Capability
- Lowest-in-class Conduction Losses
- High Circuit Efficiency
- Minimal Input Signal Distortion
- High Amplifier Bandwidth

Package

- RoHS Compliant



TO – 257 (Isolated Base-plate Hermetic Package)

Applications

- Down Hole Oil Drilling, Geothermal Instrumentation
- Hybrid Electric Vehicles (HEV)
- Solar Inverters
- Switched-Mode Power Supply (SMPS)
- Power Factor Correction (PFC)
- Induction Heating
- Uninterruptible Power Supply (UPS)
- Motor Drives

Absolute Maximum Ratings

| Parameter | Symbol | Conditions | Values | Unit |
|-----------------------------------|----------------|--|---|------|
| Drain – Source Voltage | V_{DS} | $V_{GS} = 0\text{ V}$ | 600 | V |
| Continuous Drain Current | I_D | $T_J = 225^\circ\text{C}, T_C = 25^\circ\text{C}$ | 10 | A |
| Continuous Gate Current | I_{GM} | | 0.5 | A |
| Turn-Off Safe Operating Area | RBSOA | $T_{VJ} = 225^\circ\text{C}, I_G = 0.5\text{ A},$ Clamped Inductive Load | $I_{D,max} = 10$ @ $V_{DS} \leq V_{DSmax}$ | A |
| Short Circuit Safe Operating Area | SCSOA | $T_{VJ} = 225^\circ\text{C}, I_G = 0.5\text{ A}, V_{DS} = 400\text{ V},$ Non Repetitive | 20 | μs |
| Reverse Gate – Source Voltage | V_{GS} | | 30 | V |
| Reverse Drain – Source Voltage | V_{DS} | | 40 | V |
| Power Dissipation | P_{tot} | $T_J = 225^\circ\text{C}, T_C = 25^\circ\text{C}$ | 47 | W |
| Operating and Storage Temperature | T_J, T_{stg} | | -55 to 225 | °C |

Electrical Characteristics

| Parameter | Symbol | Conditions | Values | | | Unit |
|------------------------------|---------------|--|--------|------|------|------|
| | | | min. | typ. | max. | |
| On Characteristics | | | | | | |
| Drain – Source On Resistance | $R_{DS(ON)}$ | $I_D = 4\text{ A}, I_G = 100\text{ mA}, T_J = 25^\circ\text{C}$ | | 425 | | mΩ |
| | | $I_D = 4\text{ A}, I_G = 250\text{ mA}, T_J = 175^\circ\text{C}$ | | 800 | | |
| | | $I_D = 4\text{ A}, I_G = 250\text{ mA}, T_J = 220^\circ\text{C}$ | | 1180 | | |
| Gate Forward Voltage | $V_{GS(FWD)}$ | $I_G = 500\text{ mA}, T_J = 25^\circ\text{C}$ | | 3.3 | | V |
| | | $I_G = 500\text{ mA}, T_J = 220^\circ\text{C}$ | | 3.2 | | |
| DC Current Gain | h_{FE} | $V_{DS} = 5\text{ V}, I_D = 5\text{ A}, T_J = 25^\circ\text{C}$ | 90 | 110 | | |
| | | $V_{DS} = 5\text{ V}, I_D = 5\text{ A}, T_J = 220^\circ\text{C}$ | 60 | 80 | | |
| Off Characteristics | | | | | | |
| Drain Leakage Current | I_{DSS} | $V_R = 600\text{ V}, V_{GS} = 0\text{ V}, T_J = 25^\circ\text{C}$ | | 0.1 | 10 | μA |
| | | $V_R = 600\text{ V}, V_{GS} = 0\text{ V}, T_J = 175^\circ\text{C}$ | | 1 | 50 | |
| | | $V_R = 600\text{ V}, V_{GS} = 0\text{ V}, T_J = 220^\circ\text{C}$ | | 10 | 100 | |

Electrical Characteristics

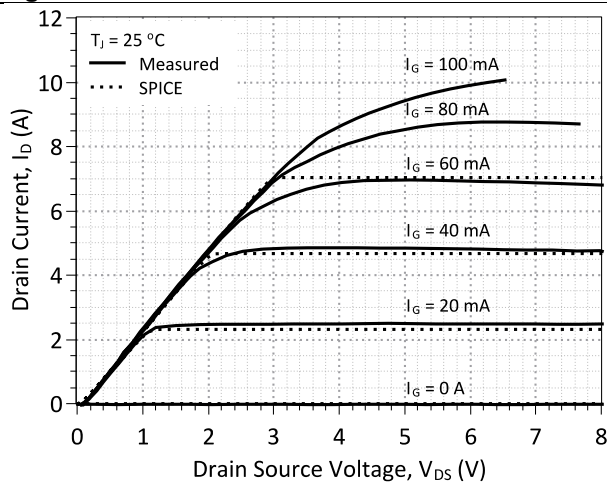
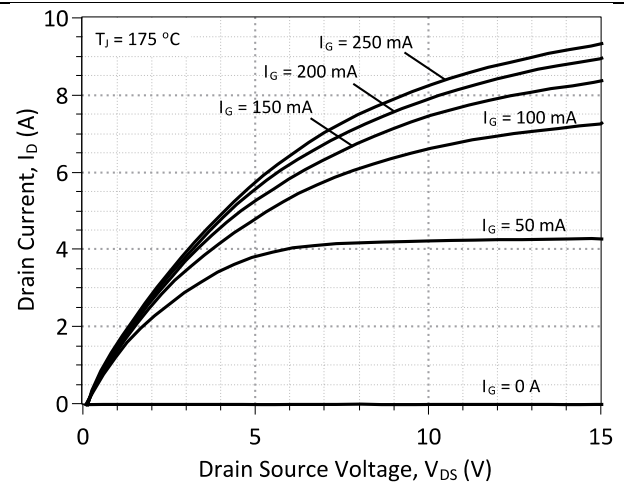
| Parameter | Symbol | Conditions | Values | | | Unit |
|-------------------------------------|-------------------|---|--------|------|------|---------------|
| | | | min. | typ. | max. | |
| Capacitance Characteristics | | | | | | |
| Input Capacitance | C_{iss} | $V_{GS} = 0\text{ V}, V_D = 600\text{ V}, f = 1\text{ MHz}$ | | 310 | | pF |
| Reverse Transfer/Output Capacitance | C_{rss}/C_{oss} | $V_D = 600\text{ V}, f = 1\text{ MHz}$ | | 17 | | pF |
| Output Capacitance Stored Energy | E_{oss} | $V_{GS} = 0\text{ V}, V_D = 600\text{ V}, f = 1\text{ MHz}$ | | 2.8 | | μJ |

Switching Characteristics

| | | | | | | |
|---------------------------|--------------|---|----|-----|---------------|---------------|
| Turn On Delay Time | $t_{d(on)}$ | $V_{DD} = 400\text{ V}, I_D = 4\text{ A},$ $R_G = 44\ \Omega, C_G = 9\text{ nF}$ Single-Level Gate Drive $V_{GS} = -8/15\text{ V}, T_J = 175\text{ }^\circ\text{C}$ Refer to Figure 11 for gate drive current waveforms | | 5 | | ns |
| Rise Time | t_r | | | 15 | | ns |
| Turn Off Delay Time | $t_{d(off)}$ | | | 75 | | ns |
| Fall Time | t_f | | | 15 | | ns |
| Turn-On Energy Per Pulse | E_{on} | | | 25 | | μJ |
| Turn-Off Energy Per Pulse | E_{off} | | 10 | | μJ | |
| Total Switching Energy | E_{ts} | | 35 | | μJ | |
| Turn On Delay Time | $t_{d(on)}$ | $V_{DD} = 400\text{ V}, I_D = 4\text{ A},$ $R_G = 44\ \Omega, C_G = 9\text{ nF}$ Single-Level Gate Drive $V_{GS} = -8/15\text{ V}, T_J = 220\text{ }^\circ\text{C}$ Refer to Figure 11 for gate drive current waveforms | | 10 | | ns |
| Rise Time | t_r | | | 20 | | ns |
| Turn Off Delay Time | $t_{d(off)}$ | | | 115 | | ns |
| Fall Time | t_f | | | 15 | | ns |
| Turn-On Energy Per Pulse | E_{on} | | | 40 | | μJ |
| Turn-Off Energy Per Pulse | E_{off} | | 10 | | μJ | |
| Total Switching Energy | E_{ts} | | 50 | | μJ | |

Thermal Characteristics

| | | | |
|-------------------------------------|--------------|-----|--------------------|
| Thermal resistance, junction - case | $R_{th(jc)}$ | 4.2 | $^\circ\text{C/W}$ |
|-------------------------------------|--------------|-----|--------------------|

Figures

Figure 1: Typical Output Characteristics at 25 °C

Figure 2: Typical Output Characteristics at 175 °C

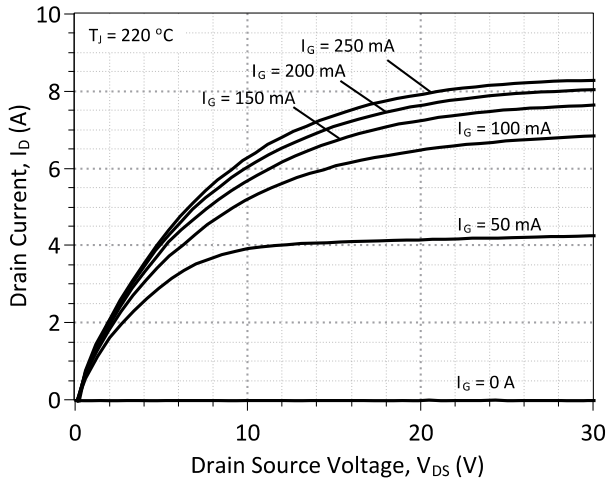


Figure 3: Typical Output Characteristics at 220 °C

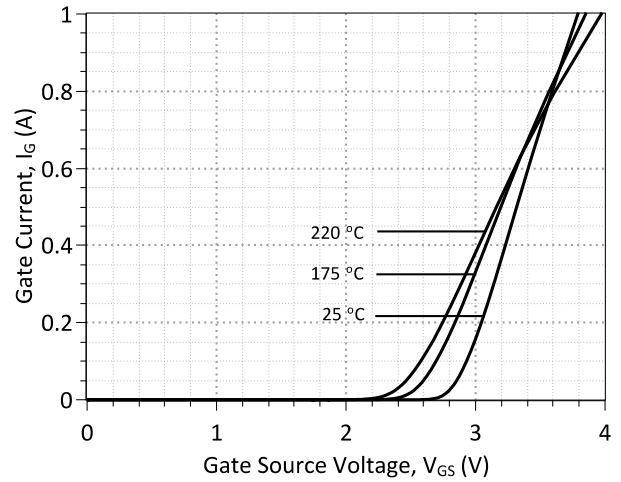


Figure 4: Typical Gate Source I-V Characteristics vs. Temperature

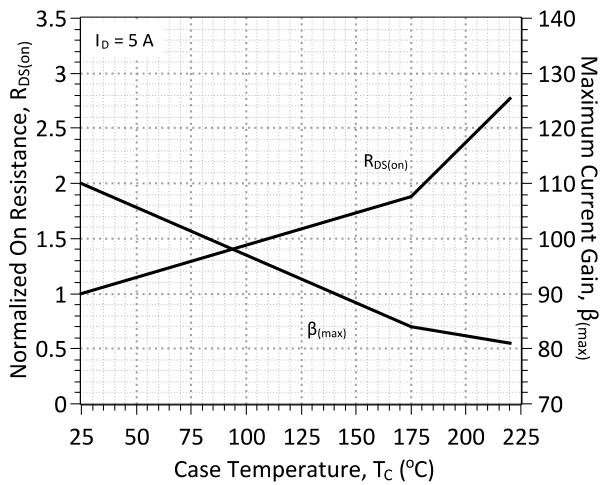


Figure 5: Normalized On-Resistance and Current Gain vs. Temperature

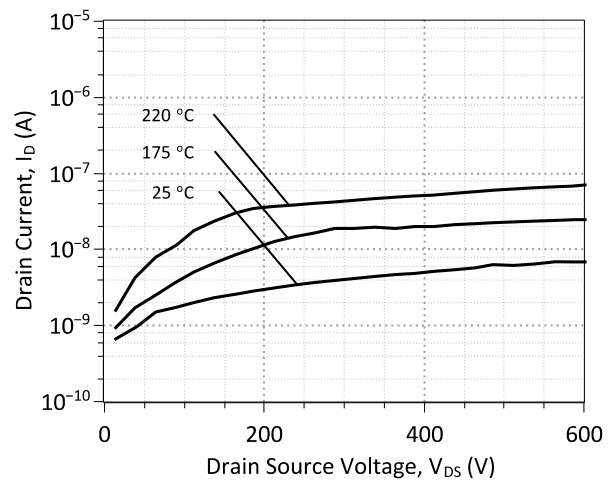


Figure 6: Typical Blocking Characteristics

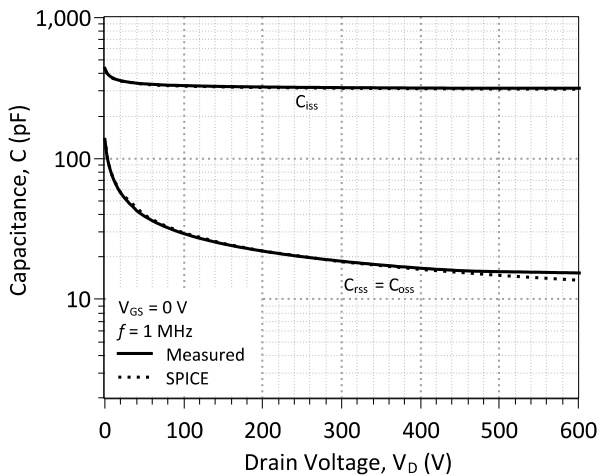


Figure 7: Capacitance Characteristics

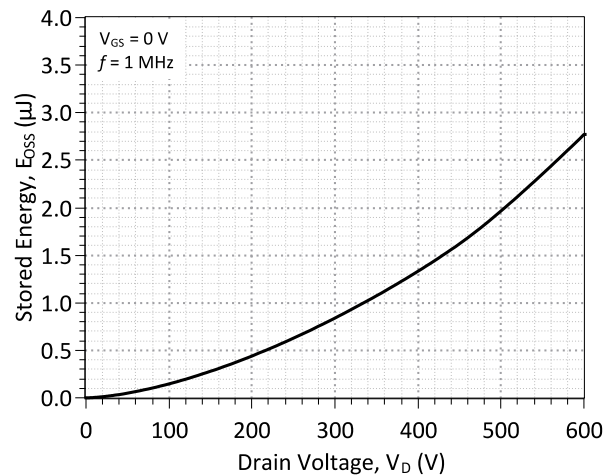


Figure 8: Output Capacitance Stored Energy

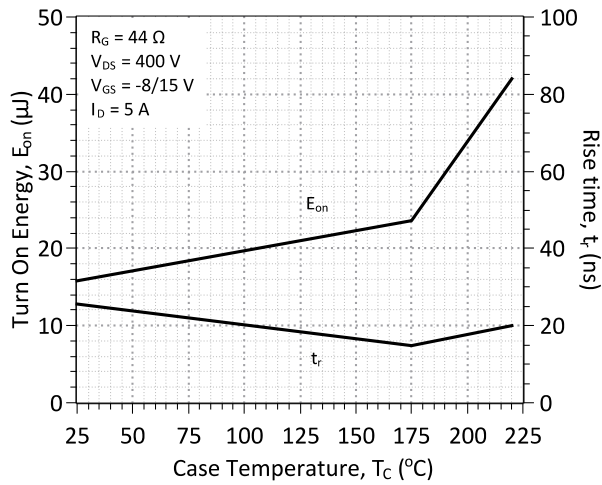


Figure 9: Typical Turn On Energy Losses and Switching Times vs. Temperature

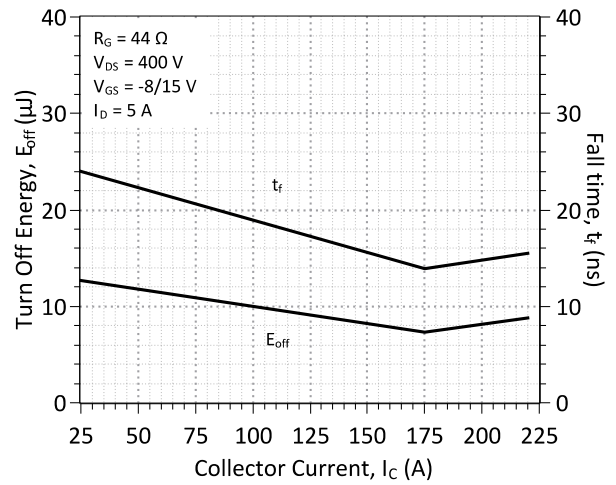


Figure 10: Typical Turn Off Energy Losses and Switching Times vs. Temperature

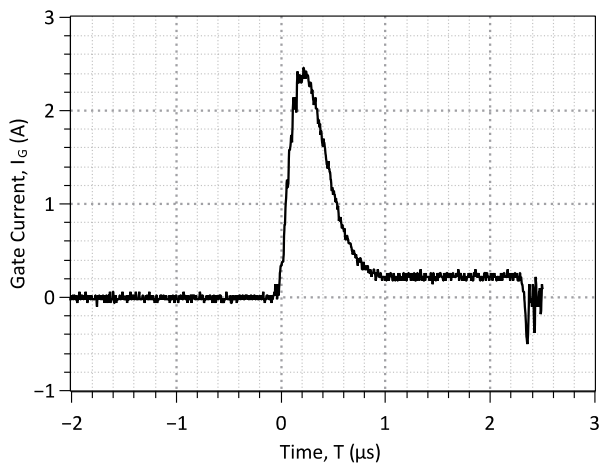


Figure 11: Typical Gate Current Waveform

Gate Drive Theory of Operation

The SJT transistor is a current controlled transistor which requires a positive gate current for turn-on as well as to remain in on-state. An ideal gate current waveform for ultra-fast switching of the SJT, while maintaining low gate drive losses, is shown in Figure 12.

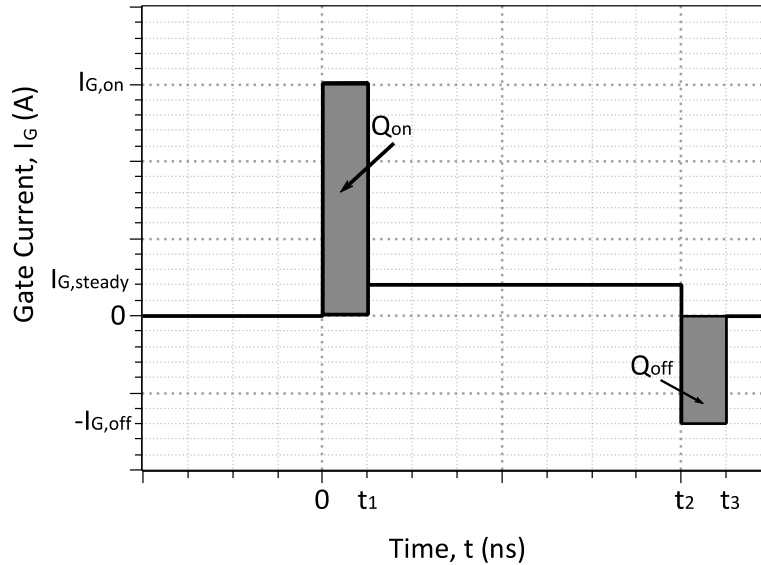


Figure 12: Idealized Gate Current Waveform

Gate Currents, $I_{G,pk}/-I_{G,pk}$ and Voltages during Turn-On and Turn-Off

An SJT is rapidly switched from its blocking state to on-state, when the necessary gate charge, Q_G , for turn-on is supplied by a burst of high gate current, $I_{G,on}$, until the gate-source capacitance, C_{GS} , and gate-drain capacitance, C_{GD} , are fully charged.

$$I_{G,on} * t_1 \geq Q_{gs} + Q_{gd}$$

The $I_{G,on}$ pulse should ideally terminate, when the drain voltage falls to its on-state value, in order to avoid unnecessary drive losses during the steady on-state. In practice, the rise time of the $I_{G,on}$ pulse is affected by the parasitic inductances, L_{par} in the package and drive circuit. A voltage developed across the parasitic inductance in the source path, L_s , can de-bias the gate-source junction, when high drain currents begin to flow through the device. The applied gate voltage should be maintained high enough, above the $V_{GS,ON}$ level to counter these effects.

A high negative peak current, $-I_{G,off}$ is recommended at the start of the turn-off transition, in order to rapidly sweep out the injected carriers from the gate, and achieve rapid turn-off. While satisfactory turn off can be achieved with $V_{GS} = 0$ V, a negative gate voltage V_{GS} may be used in order to speed up the turn-off transition.

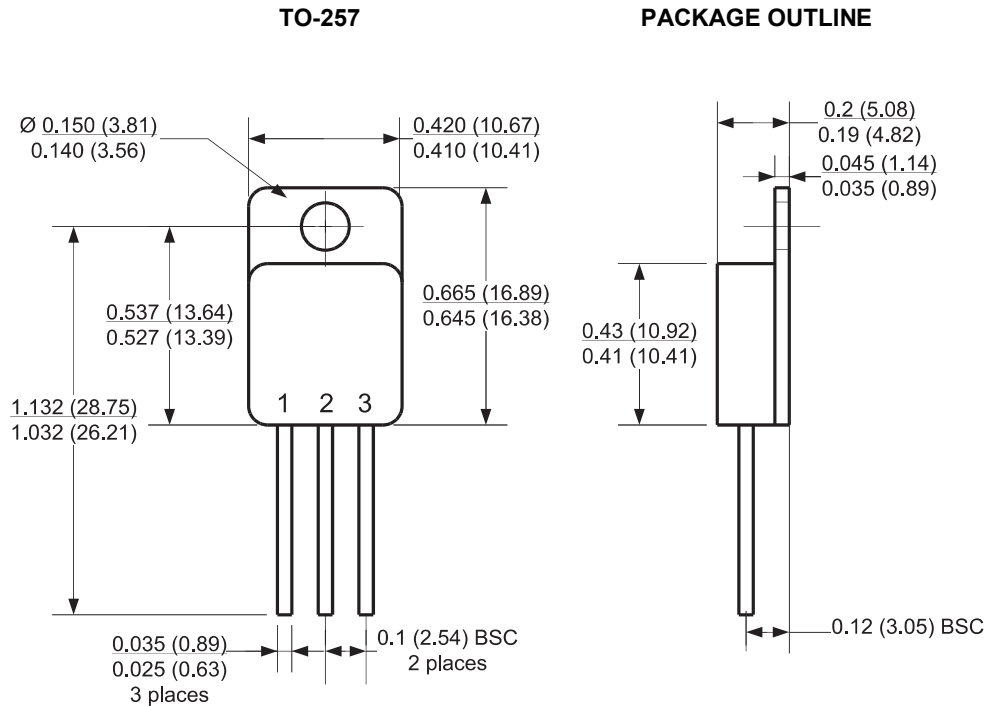
Steady On-State

After the device is turned on, I_G may be advantageously lowered to $I_{G,steady}$ for reducing unnecessary gate drive losses. The $I_{G,steady}$ is determined by noting the DC current gain, h_{FE} , of the device.

The desired $I_{G,steady}$ is determined by the peak device junction temperature T_J during operation, drain current I_D , DC current gain h_{FE} , and a 50 % safety margin to ensure operating the device in the saturation region with low on-state voltage drop by the equation:

$$I_{G,steady} \approx \frac{I_D}{h_{FE}(T, I_D)} * 1.5$$

Package Dimensions:



NOTE
 1. CONTROLLED DIMENSION IS INCH. DIMENSION IN BRACKET IS MILLIMETER.
 2. DIMENSIONS DO NOT INCLUDE END FLASH, MOLD FLASH, MATERIAL PROTRUSIONS

| Revision History | | | |
|------------------|----------|------------------------------------|------------|
| Date | Revision | Comments | Supersedes |
| 2014/08/23 | 5 | Updated Electrical Characteristics | |
| 2014/03/20 | 4 | Updated Gate Drive Section | |
| 2014/02/11 | 3 | Updated Electrical Characteristics | |
| 2013/12/19 | 2 | Updated Gate Drive Section | |
| 2013/11/18 | 1 | Updated Electrical Characteristics | |
| 2012/08/24 | 0 | Initial release | |

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SPICE Model Parameters

This is a secure document. Please copy this code from the SPICE model PDF file on our website (http://www.genesicsemi.com/images/hit_sic/sjt/2N7635-GA_SPICE.pdf) into LTSPICE (version 4) software for simulation of the 2N7635-GA.

```
*      MODEL OF GeneSiC Semiconductor Inc.
*
*      $Revision:   1.2           $
*      $Date:      23-JUN-2014   $
*
*      GeneSiC Semiconductor Inc.
*      43670 Trade Center Place Ste. 155
*      Dulles, VA 20166
*
*      COPYRIGHT (C) 2014 GeneSiC Semiconductor Inc.
*      ALL RIGHTS RESERVED
*
*      These models are provided "AS IS, WHERE IS, AND WITH NO WARRANTY
*      OF ANY KIND EITHER EXPRESSED OR IMPLIED, INCLUDING BUT NOT LIMITED
*      TO ANY IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A
*      PARTICULAR PURPOSE."
*      Models accurate up to 2 times rated drain current.
*
.model 2N7635 NPN
+ IS      1.22E-47
+ ISE     3.908E-27
+ EG      3.23
+ BF      121
+ BR      0.55
+ IKF     999
+ NF      1
+ NE      2.022
+ RB      10.0
+ RE      0.231
+ RC      0.16
+ CJC     1.37E-10
+ VJC     3.150960833
+ MJC     0.43821105
+ CJE     2.97E-10
+ VJE     2.901930244
+ MJE     0.475141754
+ XTI     3
+ XTB     -0.45
+ TRC1    1.50E-02
+ VCEO    600
+ ICRATING 10
+ MFG     GeneSiC_Semiconductor
*
* End of 2N7635-GA SPICE Model
```