Giantec Semiconductor Inc.

ADVANCED

GT25C01

SPI

1K bits

Serial EEPROM

Table of Content

1 FEATURES

- Serial Peripheral Interface (SPI) Compatible
  - Supports Mode 0 (0,0) and Mode 3 (1,1)
- Wide-voltage Operation
  - Vcc = 1.8V to 5.5V
- Low power CMOS
  - Standby current: ≤ 1 μA (1.8V)
  - Operating current: ≤ 1 mA (1.8V)
- Operating frequency: 20 MHz (5.5V)
- Memory organization: 1Kb (128 x 8)
- Byte and Page write (up to 8 bytes)
  - Partial page write allowed
- Block Write Protection
  - Protect 1/4, 1/2, or Entire Array
- Self timed write cycle: 5 ms (max.)
- High-reliability
  - Endurance: 1 million cycles
  - Data retention: 100 years
- Industrial temperature grade
- Packages (8-pin): SOIC/SOP, TSSOP and UDFN
- Lead-free, RoHS, Halogen free, Green

2 DESCRIPTION

The GT25C01 is an industrial standard electrically erasable programmable read only memory (EEPROM) product that utilizes standard Serial Peripheral Interface (SPI) for communications. The GT25C01 contains a memory array of 1K bits (128x 8), which is organized in 8 bytes per page.

This EEPROM operates in a wide voltage range from 1.8V to 5.5V, which fits most application. The device provides low-power operations and low standby current. The product is offered in Lead-free, RoHS, halogen free or Green package. The available package types are 8-pin SOIC/SOP, TSSOP and UDFN.

The functionalities of the GT25C01 are optimized for most applications, such as consumer electronics, wireless, telecommunication, industrial, medical, instrumentation, commercial and others, where low-power and low-voltage are vital. This product has a compatible SPI interface: Chip-Select ($\overline{CS}$), Serial Data In (SI), Serial Data Out (SO) and Serial Clock (SCK) for high-speed communication. Furthermore, a Hold feature via $\overline{HOLD}$ pin allows the device entering into a suspended state whenever necessary and resuming the communication without re-initializing the serial sequence. A Status Register facilitates a flexible write protection mechanism and device status monitoring.

In order to refrain the state machine from entering into a wrong state during power-up sequence or a power toggle off-on condition, a power on reset circuit is implemented. During power-up, the device does not respond to any instructions until the supply voltage (V_{CC}) has reached an acceptable stable level above the reset threshold voltage. Once V_{CC} passes the power on reset threshold, the device is reset and enters into Standby mode. This should also avoid any inadvertent Write operations during power-up stage. During power-down process, the device will enter into standby mode, once V_{CC} drops below the power on reset threshold voltage. In addition, the device will be in standby mode after receiving the Stop command, provided that no internal write operation is in progress. Nevertheless, it is illegal to send a command unless the Vcc is within its operating level.

3 PIN CONFIGURATION

Fig. 3.1: 8-Pin SOIC/SOP and TSSOP

Fig. 3.2: 8-Lead UDFN

(Top View)
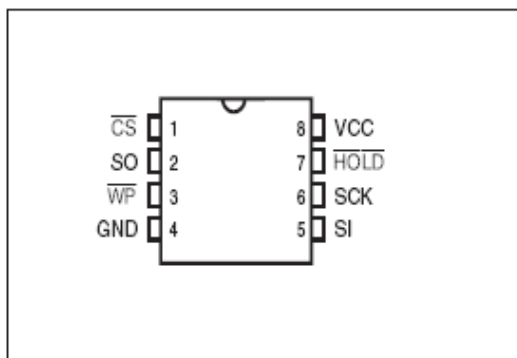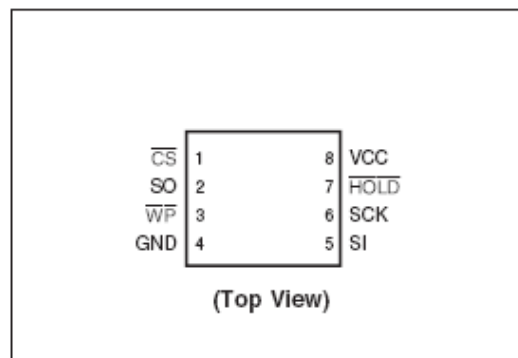
Table 3.1: Pin Descriptions

Pin Name	Descriptions
$\overline{\text{CS}}$	Chip Select
SO	Serial Data Output
$\overline{\text{WP}}$	Write Protect Input
GND	Ground
SI	Serial Data Input
SCK	Serial Clock
$\overline{\text{HOLD}}$	Hold function
V_{CC}	Supply Voltage

Chip Select ($\overline{\text{CS}}$): The $\overline{\text{CS}}$ pin is used to enable or disable the device. Upon power-up, $\overline{\text{CS}}$ must follow the supply voltage. When the device is ready for instruction input, this signal requires a High-to-Low transition. Once $\overline{\text{CS}}$ is stable at Low, the device is enabled. Then the master (usually microcontroller) and slave (EEPROM) can communicate among each other through SCK, SI and SO pins. Upon completion of transmission, $\overline{\text{CS}}$ must be driven to High in order to start the operation. After $\overline{\text{CS}}$ is driven to High, the device will enter into standby mode, unless an operation is in progress. During this mode, SO becomes high impedance.

Serial Clock (SCK): Under the SPI modes (0, 0) and (1, 1), this clock signal provides synchronization between the microcontroller and GT25C01. Typically, Op-Codes, addresses and data are latched from SI at the rising edge of SCK, while data from SO are clocked out at the falling edge of SCK.

Serial Data Input (SI): Data Input pin.

Serial Data Output (SO): Data output pin.

Write Protect ($\overline{\text{WP}}$): This active Low input signal is utilized to initiate Hardware Write Protection mode. This mode prevents the Block Protection bits and the WPEN bit in the Status Register from being modified. To activate the Hardware Write Protection, $\overline{\text{WP}}$ must be Low simultaneously when WPEN is set to 1.

HOLD ($\overline{\text{HOLD}}$): This feature is used to suspend the device in the middle of a serial sequence and temporarily ignore further communication on the bus (SI, SO, SCK). The $\overline{\text{HOLD}}$ signal transitions must occur only when SCK is Low and be held stable during SCK transitions. Connecting $\overline{\text{HOLD}}$ to High disables this feature. Fig. 8 shows Hold timing.

4 BLOCK DIAGRAM

Fig. 4.1: Functional block diagram
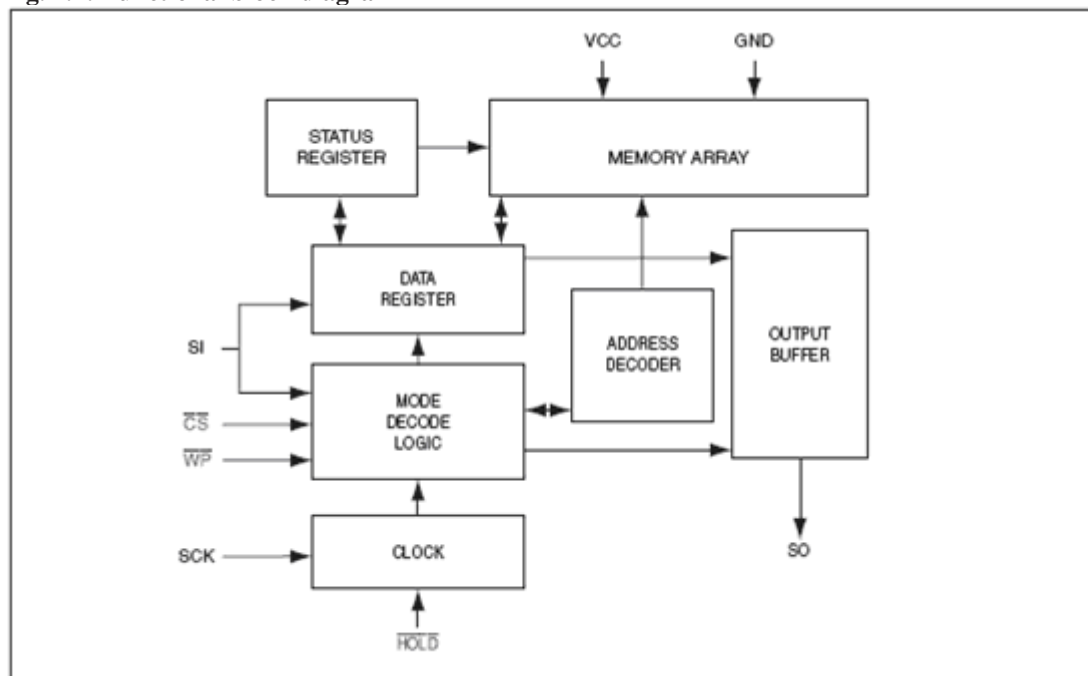
SERIAL INTERFACE DESCRIPTION

MASTER: The device that provides a clock signal.

SLAVE: GT25C01.

TRANSMITTER / RECEIVER: The GT25C01 has both data input (SI) and data output (SO).

MSB (Most **S**ignificant **B**it) is the first bit being transmitted or received.

Op-Code: Operational instruction code typically sent to the GT25C01 is the first byte of information transmitted after $\overline{\text{CS}}$ is Low. If the Op-Code is a valid instruction as listed in Table 5.3, then it will be decoded appropriately. It is prohibited to send an invalid Op-Code.

5 FUNCTIONAL OPERATIONS

STATUS REGISTER

The Status Register accessible by the user consists of 8-bits data for write protection control and write status. It becomes Read-Only under any of the following conditions: Hardware Write Protection is enabled or WEN is set to 0. If neither is true, it can be modified by a valid instruction.

Table 5.1: Status Register

Bit	Symbol	Name	Description
0	$\overline{\text{RDY}}$	Ready	When $\overline{\text{RDY}}$ = 0, device is ready for an instruction. When $\overline{\text{RDY}}$ = 1, device is busy. As busy, device only accepts Read Status Register command.
1	WEN	Write Enable	This represents the write protection status of the device. When WEN = 0, Status Register and entire array cannot be modified, regardless the setting of WPEN, $\overline{\text{WP}}$ pin or block protection. Write Enable command (WREN) can be used to set WEN to 1. Upon power-up stage, WEN is reset to 0.
2	BP0	Block Protect Bit	Despite of the status on WPEN, $\overline{\text{WP}}$ or WEN, BP0 and BP1 configure any combinations of the four blocks being protected (Table 5.2). They are non-volatile memory and programmed to 0 by factory.
3	BP1	Block Protect Bit	
4	X	Don't Care	Values can be either 0 or 1, but are not retained. Mostly always 0, except during write operation.
5	X	Don't Care	
6	X	Don't Care	
7	WPEN	Write Protect Enable	This bit can be utilized to enable Hardware Write Protection, together with $\overline{\text{WP}}$ pin. If enabled, Status Register becomes read-only. However, the memory array is not protected by this mode. Hardware Write Protection requires the setting of $\overline{\text{WP}}$ = 0 and WPEN = 1. Otherwise, it is disabled. WPEN cannot be altered from 1 to 0 if $\overline{\text{WP}}$ is already set to Low. (Table 5.4 for write protection)

Note: During internal write cycles, bits 0 to 7 are temporarily 1's.

Table 5.2: Block Protection by BP0 and BP1

Level	Status Register Bits		Array Addresses Protected
	BP1	BP0	
0	0	0	None
1 (1/4)	0	1	060h-07Fh
2 (1/2)	1	0	040h-07Fh
3 (All)	1	1	000h-07Fh

Op-Code INSTRUCTIONS

The operations of the GT25C01 are controlled by a set of instruction Op-Codes (Table 5.3) that are clocked-in serially via SI pin. To initiate an instruction, the chip select ($\overline{\text{CS}}$) must be Low. Subsequently, each Low-to-High transition of the clock (SCK) will latch a stable level from SI. After the 8-bit Op-Code, it may continue to latch-in an address and/or data from SI accordingly, or to output data from SO. During

data output, data are latched out at the falling edge of SCK. All communications start with MSB first. Upon the transmission of the last bit but prior to any following Low-to-High transition on SCK, $\overline{CS}$ must be brought to High in order to end the transaction and start the operation. The device will enter into Standby Mode after the operation is completed.

Table 5.3: Instruction Op-Codes[1,2,3]

Name	Op-Code	Operation	Address	Data (SI)	Data (SO)
WREN	0000 X110	Set Write Enable Latch	-	-	-
WRDI	0000 X100	Reset Write Enable Latch	-	-	-
RDSR	0000 X101	Read Status Register	-	-	D_7-D_0 -
WRSR	0000 X001	Write Status Register	-	D_7-D_0	-
READ	0000 X011	Read Data from Array	A_7-A_0	-	D_7-D_0, ...
WRITE	0000 X010	Write Data to Array	A_7-A_0	D_7-D_0, ...	-

Notes: [1] X = Don't care bit. However, it is recommended to be "0".

[2] Some address bits may be don't care (Table 5.5).

[3] It is strongly recommended that an appropriate format of Op-Code must be entered. Otherwise, it may cause unexpected phenomenon to be occurred. Nevertheless, it is illegal to input invalid any Op-Code.

WRITE ENABLE (WREN)

When Vcc is initially applied, the device powers up with both status register and entire array in a write-disabled state. Upon completion of Write Disable (WRDI), Write Status Register (WRSR) or Write Data to Array (WRITE), the device resets the WEN bit in the Status Register to 0. Prior to any data modification, a WREN instruction is necessary to set WEN to 1 (Fig. 2).

WRITE DISABLE (WRDI)

The device can be completely protected from modification by resetting WEN to 0 through the WRDI instruction (Fig. 3).

READ STATUS REGISTER (RDSR)

The Read Status instruction reviews the status of Write Protect Enable, Block Protection setting (Table 5.2), Write Enable state and $\overline{RDY}$ status. RDSR is the only instruction accepted when a write cycle is underway. It is recommended that the status of Write Enable and $\overline{RDY}$ be checked, especially prior to an attempted modification of data. These 8 bits information can be repeatedly output on SO after the initial Op-Code (Fig. 4).

WRITE STATUS REGISTER (WRSR)

The WRSR instruction allows the user to choose a Block Protection setting and set or reset the WPEN bit. The values of the other data bits incorporated into WRSR can be 0 or 1 and are not stored in the Status Register. WRSR will be ignored unless both following conditions are true: a) WEN = 1, due to a prior WREN instruction; and b) Hardware Write Protection is not enabled (Table 5.4). Except for $\overline{RDY}$ status, the values in the Status Register remain unchanged until the moment when the write cycle is completed and the register is updated. Note that WPEN can be changed from 1 to 0 only if $\overline{WP}$ is already set High. Once completed, WEN is reset for complete chip write protection (Fig. 5).

READ DATA (READ)

This instruction includes an Op-Code and 8-bit address, then results the selected data to be shifted out from SO. Following the first data byte, additional sequential data can be output. If the data byte of the last address is initially output, then address will rollover to the first address in the array, and the output could loop indefinitely. At any time, a rising $\overline{CS}$ signal ceases the operation (Fig. 6).

WRITE DATA (WRITE)

The WRITE instruction contains an Op-Code, a 8-bit address and the first data byte. Additional data bytes may be supplied sequentially after the first byte. Each WRITE instruction can affect up to 8 bytes of data in

a page. Each page has a starting address XXXXXXXX XXXXX000 and an ending address XXXXXXXX XXXXX111. After the last byte of data in a page is input, the address rolls over to the beginning of the same page. If more than 8 bytes of data is input during a single instruction, then only the last 8 bytes will be retained, but the initial data will be overwritten.

The contents of the array defined by Block Protection cannot be modified as long as that block configuration is selected. The contents of the array outside the Block Protection can only be modified if Write Enable (WEN) is set to 1. Therefore, it may be necessary that a WREN instruction is initiated prior to WRITE. Once Write operation is completed, WEN is reset for complete chip write protection (Fig. 7). Besides, Hardware Write Protection has no affect on the memory array.

Table 5.4: Write Protection

WPEN	$\overline{WP}$	Hardware Write Protection	WEN	Inside Block	Outside Block	Status Register (WPEN, BP1, BP0)
0	X	Not Enabled	0	Read-only	Read-only	Read-only
0	X	Not Enabled	1	Read-only	Unprotected	Unprotected
1	0	Enabled	0	Read-only	Read-only	Read-only
1	0	Enabled	1	Read-only	Unprotected	Read-only
X	1	Not Enabled	0	Read-only	Read-only	Read-only
X	1	Not Enabled	1	Read-only	Unprotected	Unprotected

Note: X = Don't care bit.

Table 5.5: Address Key

Name	GT25C01
A_N	A_6-A_0
Don't Care Bits	A_7

6 ABSOLUTE MAXIMUM RATINGS

Table 6.1: Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
V_{DD}	Supply voltage	-0.5 to + 6.5	V
V_P	Voltage on any other pin	-0.5 to Vcc + 0.5	V
T_{BIAS}	Temperature Under Bias	-55 to +125	°C
T_{STG}	Storage Temperature	-65 to +150	°C
I_{OUT}	Output Current	5	mA

Notes: Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operational sections of this specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING RANGE

Table 6.2: Operating Range

Supply Voltage	Ambient Temperature (T_A)	Grade
1.8V to 5.5V	–40°C to +85°C	Industrial

Note: Giantec offers Industrial grade for Commercial applications (0°C to +70°C).

CAPACITANCE

Table 6.3: Capacitance

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}	Input Capacitance	$V_{IN} = 0V$	6	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$	8	pF

Notes:
1. Tested initially and after any design or process changes that may affect these parameters and not 100% tested.
2. Test conditions: $T_A = 25°C$, f = 1 MHz, Vcc = 5.0V.

7 DC ELECTRICAL CHARACTERISTICS

Table 7.1: Industrial: T_A = –40°C to +85°C, Supply voltage = 1.8V to 5.5V

Symbol	Parameter	Vcc	Test Conditions	Min.	Max.	Unit
V_{CC}	Supply Voltage			1.8	5.5	V
V_{IH}	Input High Voltage			0.7* V_{CC}	V_{CC}+1	V
V_{IL}	Input Low Voltage			-0.3	0.3* V_{CC}	V
I_{LI}	Input Leakage Current		V_{IN} = 0V To V_{CC}	-2	2	μA
I_{LO}	Output Leakage Current		V_{OUT} = 0V To V_{CC}, $\overline{CS}$ = V_{CC}	-2	2	μA
V_{OH1}	Output High Voltage	1.8	I_{OH} = -0.1mA	0.8*V_{CC}	—	V
		2.5	I_{OH} = -0.4mA	0.8*V_{CC}	—	V
		5	I_{OH} = -2 mA	0.8*V_{CC}	—	V
V_{OL1}	Output Low Voltage	1.8	I_{OL} = 0.15 mA	—	0.2	V
		2.5	I_{OL} = 1.5 mA	—	0.4	V
		5	I_{OL} = 2 mA	—	0.4	V
I_{CC1}	Operating Current	1.8	Read/Write at 5 MHz, SO=Open, SCK=0.2*V_{CC}/0.8*V_{CC}	—	1	mA
		2.5	Read/Write at 10 MHz, SO=Open, SCK=0.2*V_{CC}/0.8*V_{CC}	—	3	mA
		5	Read/Write at 20 MHz, SO=Open, SCK=0.2*V_{CC}/0.8*V_{CC}	—	8	mA
I_{SB1}	Standby Current	1.8	V_{IN}= V_{CC} or GND , $\overline{CS}$ = V_{CC}	—	1	μA
		2.5	V_{IN}= V_{CC} or GND , $\overline{CS}$ = V_{CC}	—	2	μA
		5	V_{IN}= V_{CC} or GND , $\overline{CS}$ = V_{CC}	—	3	μA

8 AC ELECTRICAL CHARACTERISTICS

Table 8.1: Industrial: $T_A = -40°C$ to $+85°C$, Supply voltage = 1.8V to 5.5V

Symbol	Parameter	1.8V≤Vcc<2.5V		2.5V≤Vcc<4.5V		4.5V≤Vcc≤5.5V		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
fSCK	SCK Clock Frequency	0	5	0	10	0	20	MHz
tRI	Input Rise Time	—	1	—	1	—	1	μs
tFI	Input Fall Time	—	1	—	1	—	1	μs
tWH	SCK High Time	80	—	40	—	20	—	ns
tWL	SCK Low Time	80	—	40	—	20	—	ns
tCS	$\overline{CS}$ High Time	100	—	50	—	25	—	ns
tCSS	$\overline{CS}$ Setup Time	100	—	50	—	25	—	ns
tCSH	$\overline{CS}$ Hold Time	100	—	50	—	25	—	ns
tSU	Data In Setup Time	20	—	10	—	5	—	ns
tH	Data In Hold Time	20	—	10	—	5	—	ns
tHD	$\overline{HOLD}$ Setup Time	20	—	10	—	5	—	ns
tCD	$\overline{HOLD}$ Hold Time	20	—	10	—	5	—	ns
tV	Output Valid	0	80	0	40	0	20	ns
tHO	Output Hold Time	0	—	0	—	0	—	ns
tLZ	$\overline{HOLD}$ to Output Low Z	0	100	0	50	0	25	ns
tHZ (ori)	$\overline{HOLD}$ to Output High Z	—	200	—	80	—	40	ns
tDIS	Output Disable Time	—	200	—	80	—	40	ns
tWC	Write Cycle Time	—	5	—	5	—	5	ms

Notes: C_L = 30pF (typical)

9 TIMING DIAGRAMS

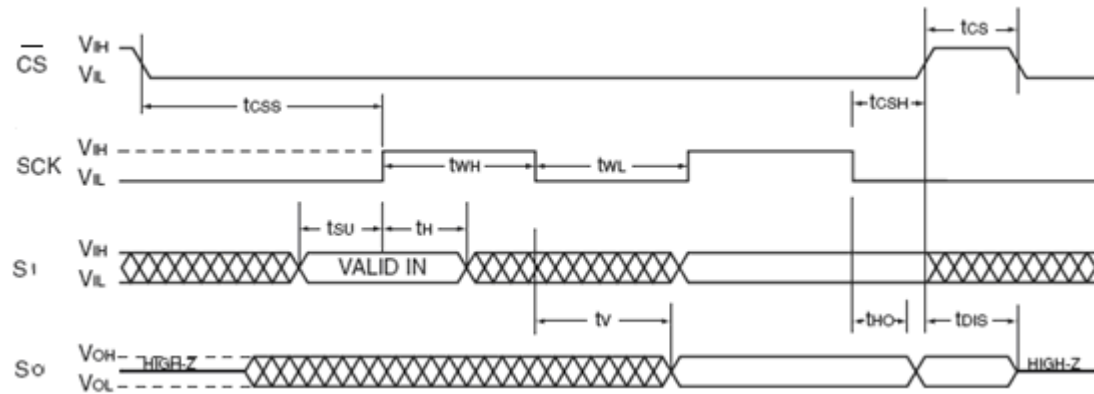**Figure 9.1: Synchronous Data Timing**

Figure 9.2: WREN Timing
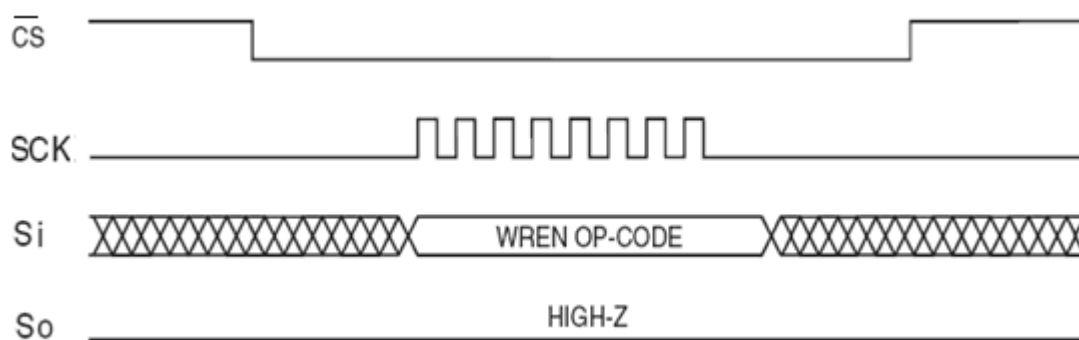
Figure 9.3: WRDI Timing
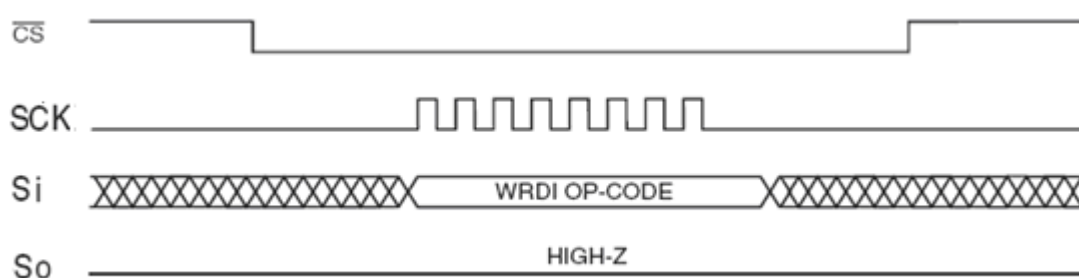
Figure 9.4: RDSR Timing
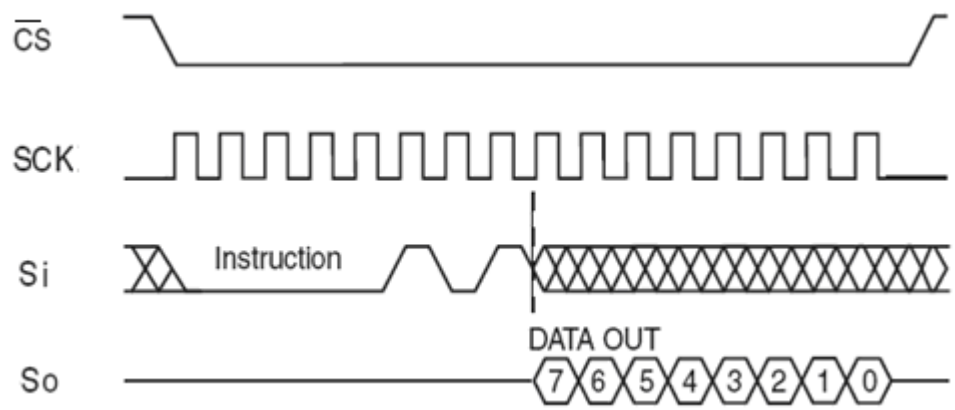
Figure 9.5: WRSR Timing
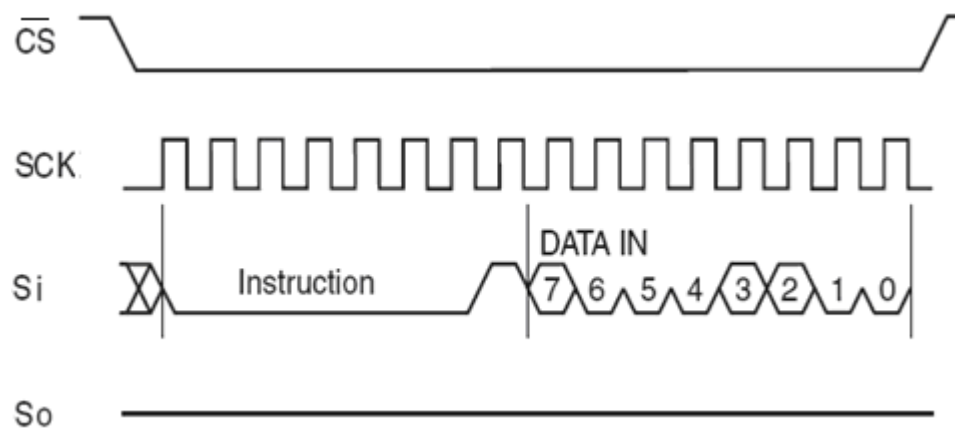
Figure 9.6: READ Timing
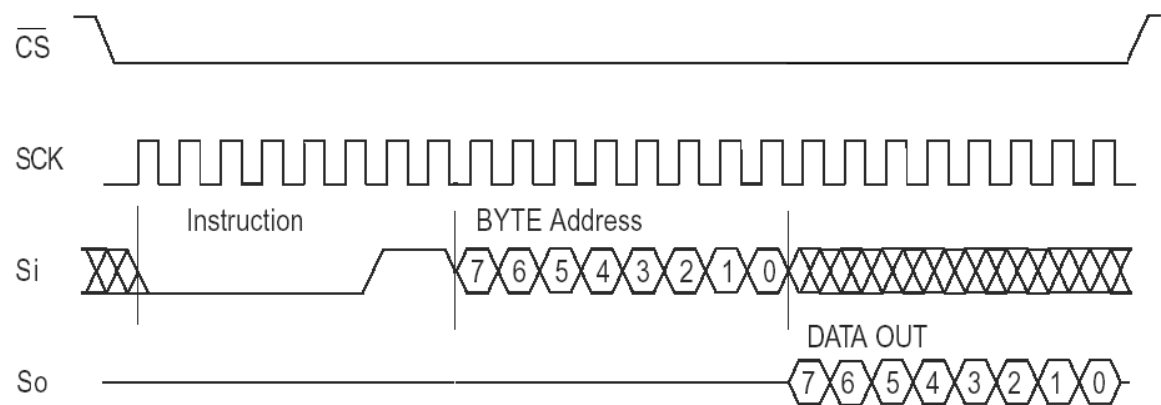
Figure 9.7: WRITE Timing
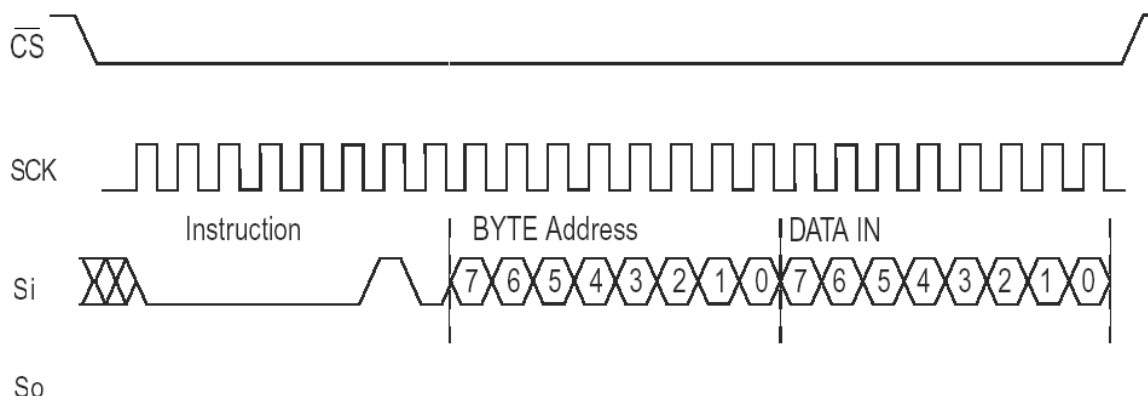
Figure 9.8: HOLD Timing
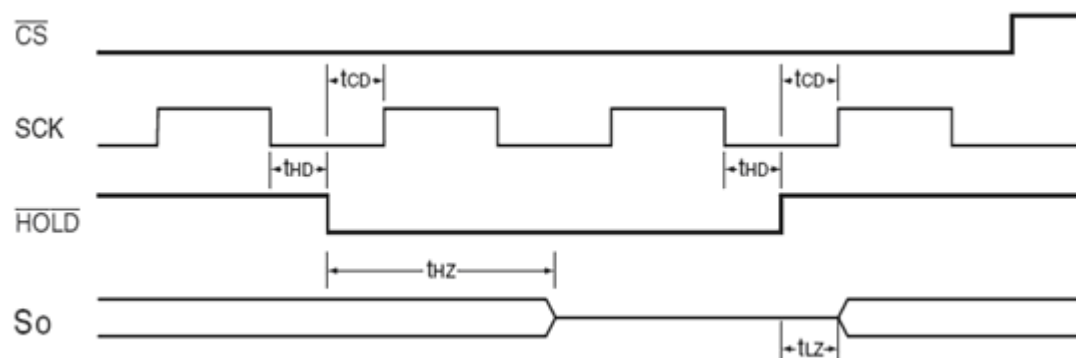
10 ORDERING INFORMATION

Industrial Grade: -40°C to +85°C, Lead-free

Voltage Range	Part Number*	Package (8-pin)*
1.8V to 5.5V	GT25C01-2GLI-TR	150-mil SOIC/SOP (JEDEC)
	GT25C01-2ZLI-TR	3 x 4.4 mm TSSOP
	GT25C01-2UDLI-TR	2 x 3 x 0.55 mm UDFN

*

1. Contact Giantec Sales Representatives for availability and other package information.
2. The listed part numbers are packed in tape and reel "-TR" (4K per reel). UDFN is 5K per reel.
3. Refer to Giantec website for related declaration document on lead free, RoHS, halogen free or Green, whichever is applicable.
4. Giantec offers Industrial grade for Commercial applications (0°C to +70°C).

11 PACKAGE INFORMATION

Fig. 11.1: SOIC/SOP (JEDEC)

SYMBOL	DIMENSION IN MM MIN.	DIMENSION IN MM NOM.	DIMENSION IN MM MAX.	DIMENSION IN INCH MIN.	DIMENSION IN INCH NOM.	DIMENSION IN INCH MAX.
A	1.35	—	1.75	0.053	—	0.069
A1	0.10	—	0.25	0.004	—	0.010
b	0.33	—	0.51	0.013	—	0.020
D	4.80	—	5.00	0.189	—	0.197
E	5.80	—	6.20	0.228	—	0.244
E1	3.80	—	4.00	0.150	—	0.157
e		1.27 BSC.			0.050 BSC.	
L	0.38	—	1.27	0.015	—	0.050
L1		0.25 BSC.			0.010 BSC.	
ZD		0.545 REF.			0.021 REF.	
θ	0	—	8°	0	—	8°

NOTE :

1. CONTROLLING DIMENSION : MM
2. DIMENSION D AND E1 DO NOT INCLUDE MOLD PROTRUSION.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION/INTRUSION.

| TITLE | 8L 150mil SOP Package Outline | REV. A | DATE 01/13/2010 |

DETAIL A

GAUGE PLANE

SAETING PLANE

Fig. 11.2: TSSOP

SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	—	—	1.20	—	—	0.047
A1	0.05	—	0.15	0.002	—	0.006
A2	0.80	1.00	1.05	0.031	0.039	0.041
b	0.19	—	0.30	0.007	—	0.012
c	0.09	—	0.20	0.004	—	0.008
D	2.90	3.00	3.10	0.114	0.118	0.122
E1		6.40 BSC			0.252 BSC	
E	4.30	4.40	4.50	0.169	0.173	0.177
e		0.65 BSC			0.026 BSC	
L	0.45	0.60	0.75	0.018	0.024	0.030
θ	0°		8°	0°		8°

NOTE
1. CONTROLLING DIMENSION IS MILLIMETER.
2. REFER TO JEDEC STANDARD MO-153 AA.
3. PACKAGE MAY HAVE EXPOSED TIE BAR.
4. DIMENSION "D" AND "E1" DOES NOT INCLUDE MOLD PROTRUSION.
5. DIMENSION "b" DOES NOT INCLUDE DAM BAR PROTRUSION.

TITLE	8L 3x4.4mm TSSOP Package Outline	REV.	A	DATE	01/13/2010

GIANTEC Semiconductor Inc.

Fig. 11.3: UDFN: Ultra-thin DFN

RECOMMENDED LAND PATTERN

0.500 0.300 0.550

1.400 2.300 1.500

TOP VIEW

BOTTOM VIEW

SIDE VIEW

PIN#1 DOT BY MARKING

PIN#1 IDENTIFICATION CHAMFER

SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.50	0.55	0.60	0.020	0.022	0.024
A1	0.00	—	0.05	0.000	—	0.002
b	0.18	0.25	0.30	0.007	0.010	0.012
A3		0.152 REF.			0.006 REF	
D		2.00 BSC			0.079 BSC	
D2	1.25	1.40	1.50	0.049	0.055	0.059
E		3.00 BSC			0.118 BSC	
E2	1.15	1.30	1.40	0.045	0.051	0.055
e		0.50 BSC			0.020 BSC	
K	0.40		—	0.016		—
L	0.20	0.30	0.40	0.008	0.012	0.016

TITLE	8L 2x3mm UDFN Package Outline	REV.	A	DATE	01/13/2010

NOTE
1. CONTROLLING DIMENSION IS MILLIMETER.

12 REVISION HISTORY

Revision	Date	Descriptions
a0	Mar 2010	Initial version