

G3R20MT17K

1700 V 20 mΩ SiC MOSFET



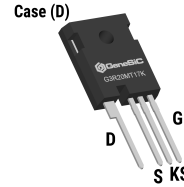
Silicon Carbide MOSFET
N-Channel Enhancement Mode

V _{DS}	=	1700 V
R _{DS(ON)(Typ.)}	=	20 mΩ
I _D (T _C = 100°C)	=	88 A

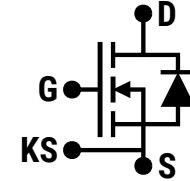
Features

- G3R™ Technology - +15 V / -5 V Gate Drive
- Superior Q_G x R_{DS(ON)} Figure of Merit
- Low Capacitances and Low Gate Charge
- High V_{th} for Increased System Stability
- Fast and Reliable Body Diode
- High Avalanche and Short Circuit Ruggedness
- Low Conduction Losses at High Temperatures
- Optimized Package with Separate Driver Source Pin

Package



TO-247-4



D = Drain
G = Gate
S = Source
KS = Kelvin Source



Advantages

- Increased Power Density for Compact System
- High Frequency Switching
- Reduced Losses for Higher System Efficiency
- Minimized Gate Ringing
- Improved Thermal Capability
- Superior Cost-Performance Index
- Ease of Paralleling without Thermal Runaway
- Simple to Drive

Applications

- Electric Vehicle Fast Charging
- Solar Inverters
- Traction Inverters
- Smart Grid and HVDC
- High Voltage DC-DC Converters
- Switched Mode Power Supply
- Wind Energy Converters
- Pulsed Power

Absolute Maximum Ratings (At T_C = 25°C Unless Otherwise Stated)

Parameter	Symbol	Conditions	Values	Unit	Note
Drain-Source Voltage	V _{DS(max)}	V _{GS} = 0 V, I _D = 100 μA	1700	V	
Gate-Source Voltage (Dynamic)	V _{GS(max)}		-10 / +20	V	
Gate-Source Voltage (Static)	V _{GS(op)}	Recommended Operation	-5 / +15	V	
Continuous Forward Current	I _D	T _C = 25°C, V _{GS} = -5 / +15 V	124	A	Fig. 15
		T _C = 100°C, V _{GS} = -5 / +15 V	88		
		T _C = 135°C, V _{GS} = -5 / +15 V	64		
Pulsed Drain Current	I _{D(pulse)}	t _p ≤ 10 μs, D ≤ 1%, Note 1	300	A	Fig. 14
Power Dissipation	P _D	T _C = 25°C	809	W	Fig. 16
Operating and Storage Temperature	T _J , T _{stg}		-55 to 175	°C	

Thermal/Package Characteristics

Parameter	Symbol	Conditions	Values			Unit	Note
			Min.	Typ.	Max.		
Thermal Resistance, Junction - Case	R _{thJC}			0.13	0.19	°C/W	Fig. 13
Weight	W _T			6.1		g	
Mounting Torque	T _M	Screws to Heatsink			1.1	Nm	

Note 1: Pulse Width t_p Limited by T_{J(max)}

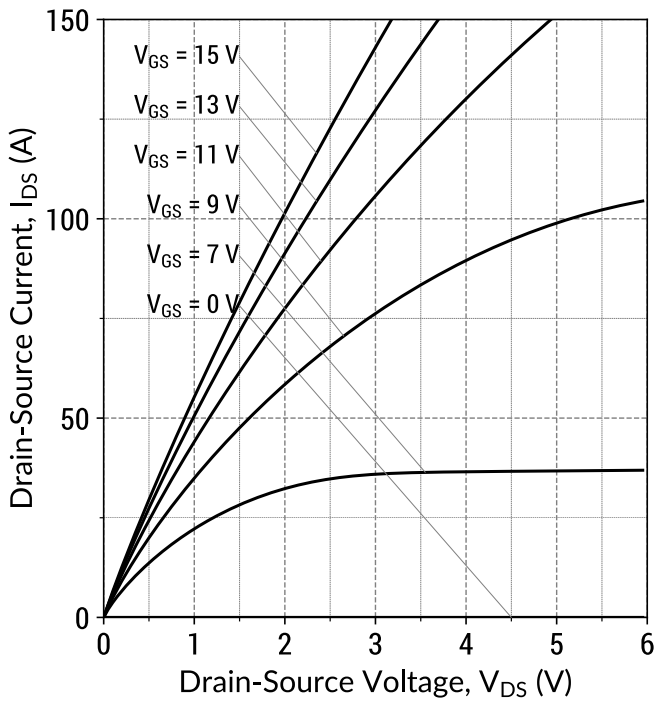
Electrical Characteristics (At $T_c = 25^\circ\text{C}$ Unless Otherwise Stated)

Parameter	Symbol	Conditions	Values			Unit	Note
			Min.	Typ.	Max.		
Drain-Source Breakdown Voltage	V_{DSS}	$V_{GS} = 0\text{ V}, I_D = 100\ \mu\text{A}$	1700			V	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 1700\text{ V}, V_{GS} = 0\text{ V}$		1		μA	
Gate Source Leakage Current	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = 20\text{ V}$			100	nA	
		$V_{DS} = 0\text{ V}, V_{GS} = -10\text{ V}$			-100		
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 15.0\text{ mA}$		2.7		V	Fig. 9
		$V_{DS} = V_{GS}, I_D = 15.0\text{ mA}, T_j = 175^\circ\text{C}$		2.05			
Transconductance	g_{fs}	$V_{DS} = 10\text{ V}, I_D = 75\text{ A}$		37.3		S	Fig. 4
		$V_{DS} = 10\text{ V}, I_D = 75\text{ A}, T_j = 175^\circ\text{C}$		41.6			
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 15\text{ V}, I_D = 75\text{ A}$		20	26	mΩ	Fig. 5-8
		$V_{GS} = 15\text{ V}, I_D = 75\text{ A}, T_j = 175^\circ\text{C}$		40			
Input Capacitance	C_{iss}			10187		pF	Fig. 11
Output Capacitance	C_{oss}			261			
Reverse Transfer Capacitance	C_{rss}	$V_{DS} = 1000\text{ V}, V_{GS} = 0\text{ V}$ $f = 1\text{ MHz}, V_{AC} = 25\text{ mV}$		38.7			
C_{oss} Stored Energy	E_{oss}			168		μJ	Fig. 12
C_{oss} Stored Charge	Q_{oss}			481		nC	
Gate-Source Charge	Q_{gs}	$V_{DS} = 1000\text{ V}, V_{GS} = -5 / +15\text{ V}$		101		nC	Fig. 10
Gate-Drain Charge	Q_{gd}	$I_D = 75\text{ A}$		191			
Total Gate Charge	Q_g	Per IEC607478-4		400			
Internal Gate Resistance	$R_{G(int)}$	$f = 1\text{ MHz}, V_{AC} = 25\text{ mV}$		1.2		Ω	

Reverse Diode Characteristics

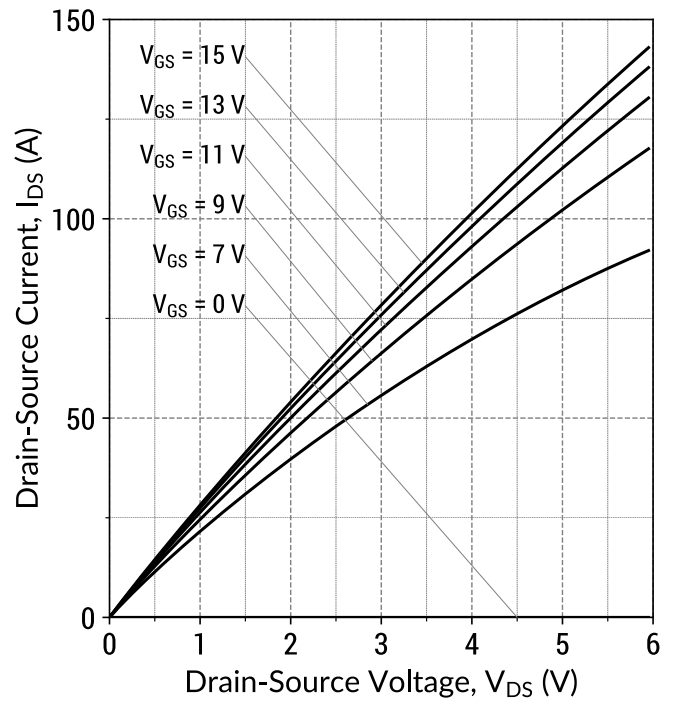
Parameter	Symbol	Conditions	Values			Unit	Note
			Min.	Typ.	Max.		
Diode Forward Voltage	V_{SD}	$V_{GS} = -5\text{ V}, I_{SD} = 37\text{ A}$		3.9		V	Fig. 17-18
		$V_{GS} = -5\text{ V}, I_{SD} = 37\text{ A}, T_j = 175^\circ\text{C}$		3.5			
Continuous Diode Forward Current	I_S	$V_{GS} = -5\text{ V}, T_c = 100^\circ\text{C}$	85			A	
Diode Pulse Current	$I_{S(pulse)}$	$V_{GS} = -5\text{ V}, \text{Note 1}$		340		A	

Figure 1: Output Characteristics ($T_j = 25^\circ\text{C}$)



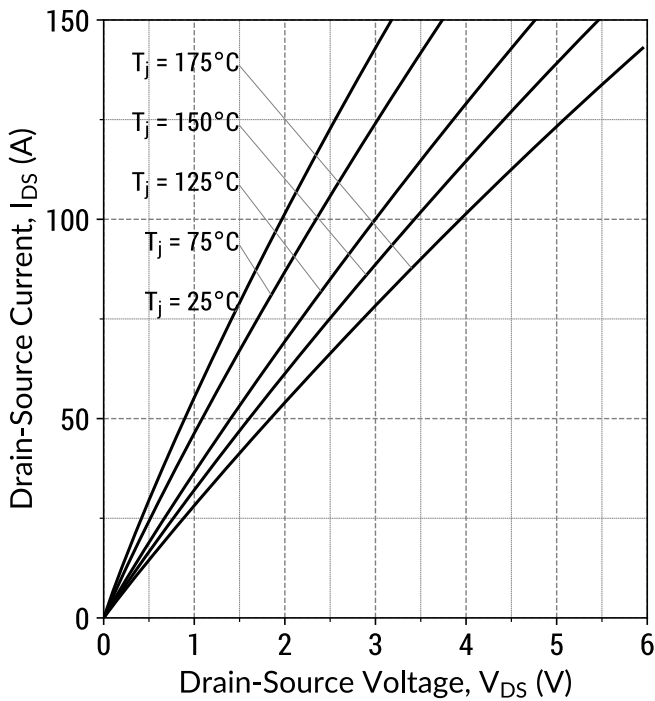
$I_D = f(V_{DS}, V_{GS}); t_P = 250 \mu\text{s}$

Figure 2: Output Characteristics ($T_j = 175^\circ\text{C}$)



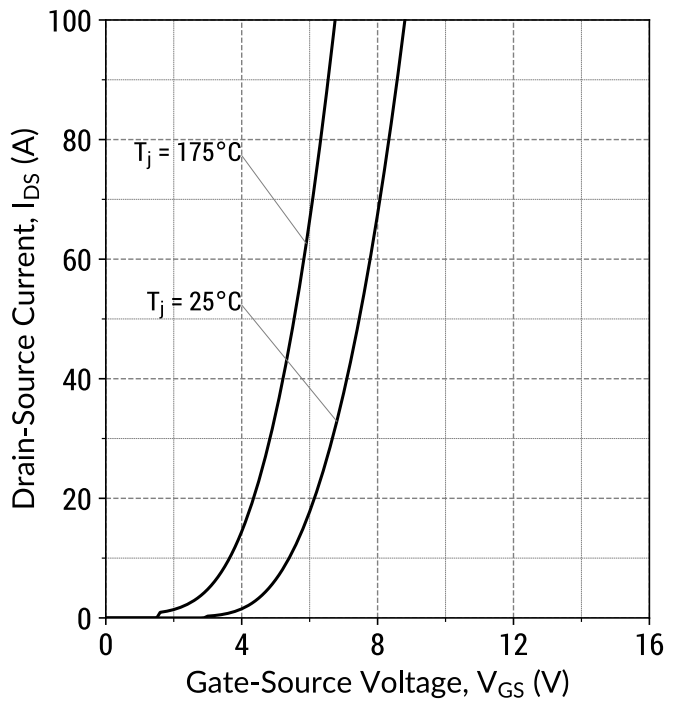
$I_D = f(V_{DS}, V_{GS}); t_P = 250 \mu\text{s}$

Figure 3: Output Characteristics ($V_{GS} = 15$ V)



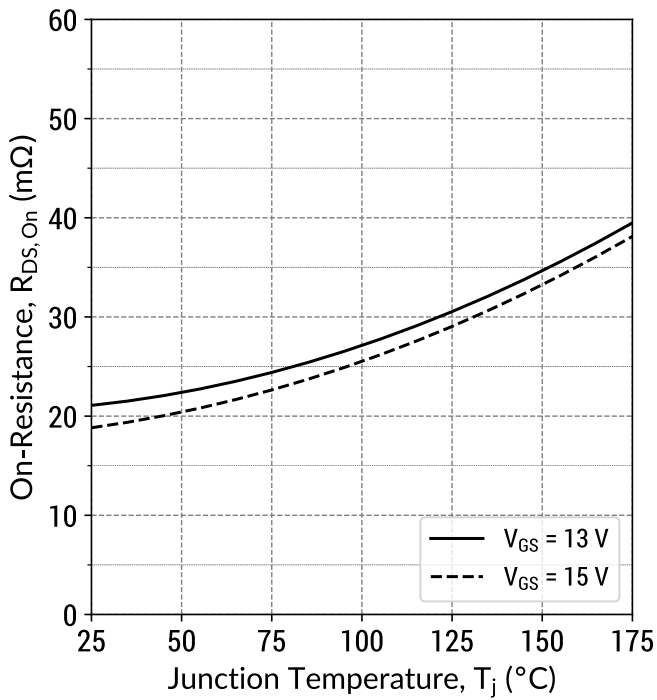
$I_D = f(V_{DS}, T_j); t_P = 250 \mu\text{s}$

Figure 4: Transfer Characteristics ($V_{DS} = 10$ V)



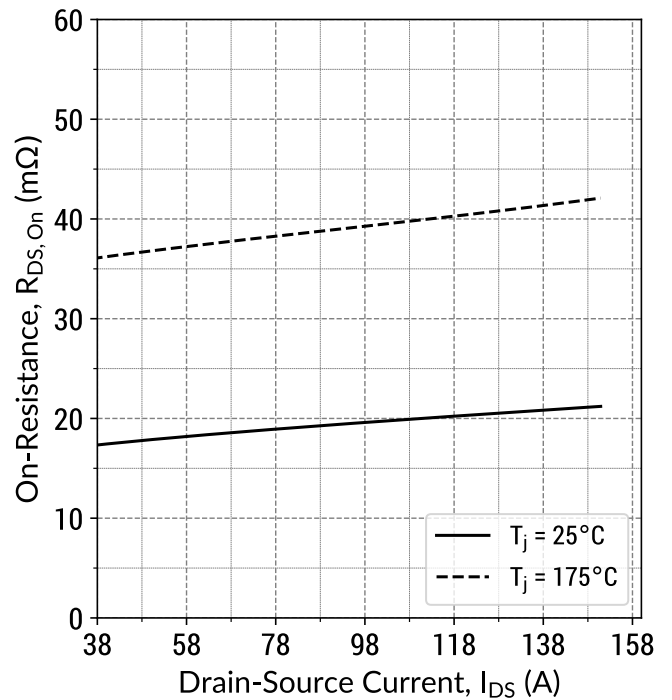
$I_D = f(V_{GS}, T_j); t_P = 100 \mu\text{s}$

Figure 5: On-State Resistance v/s Temperature



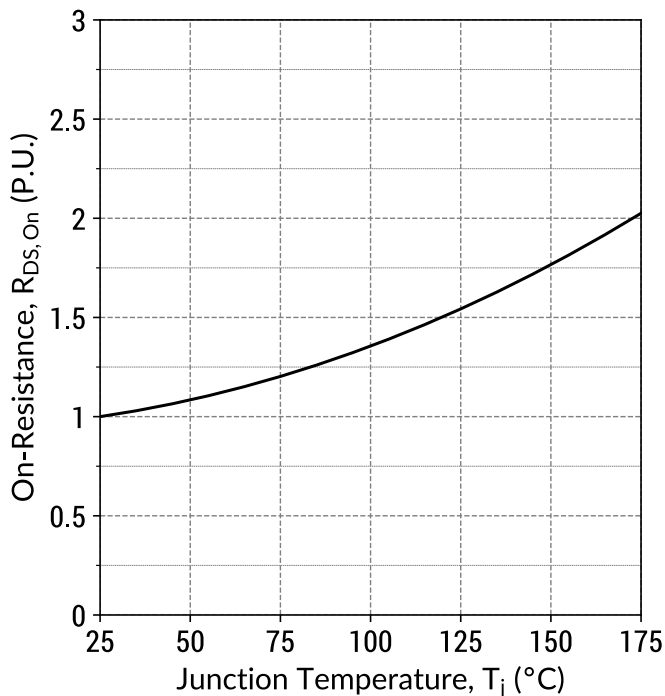
$R_{DS(ON)} = f(T_j, V_{GS}); t_P = 250 \mu s; I_D = 75 A$

Figure 6: On-State Resistance v/s Drain Current



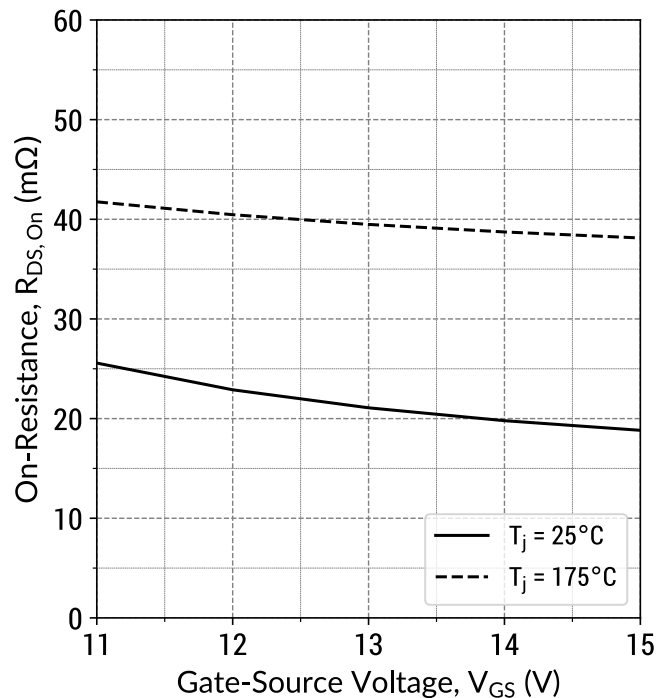
$R_{DS(ON)} = f(T_j, I_D); t_P = 250 \mu s; V_{GS} = 15 V$

Figure 7: Normalized On-State Resistance v/s Temperature



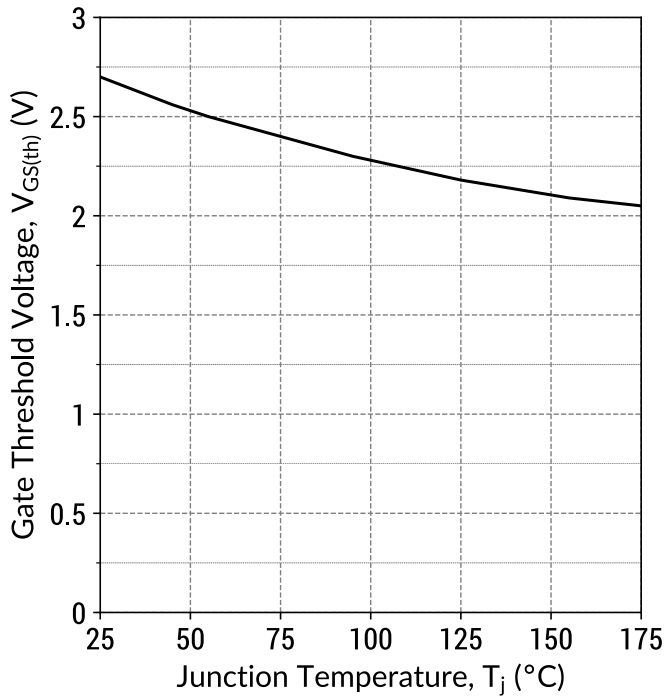
$R_{DS(ON)} = f(T_j); t_P = 250 \mu s; I_D = 75 A; V_{GS} = 15 V$

Figure 8: On-State Resistance v/s Gate Voltage



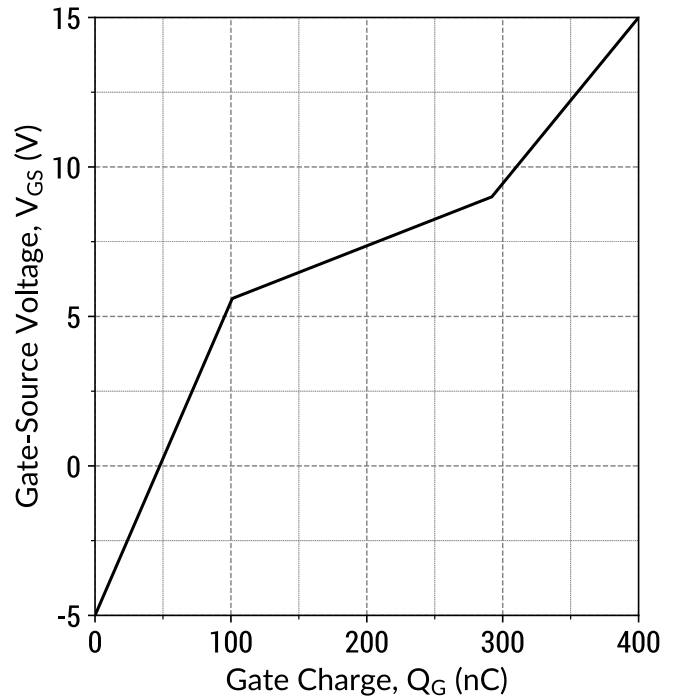
$R_{DS(ON)} = f(T_j, V_{GS}); t_P = 250 \mu s; I_D = 75 A$

Figure 9: Threshold Voltage Characteristics



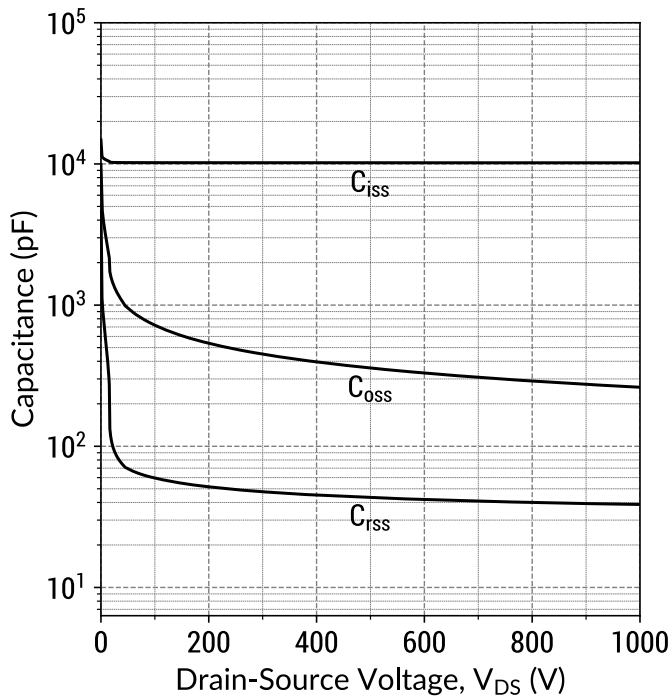
$V_{GS(th)} = f(T_j); V_{DS} = V_{GS}; I_D = 15.0 \text{ mA}$

Figure 10: Gate Charge Characteristics



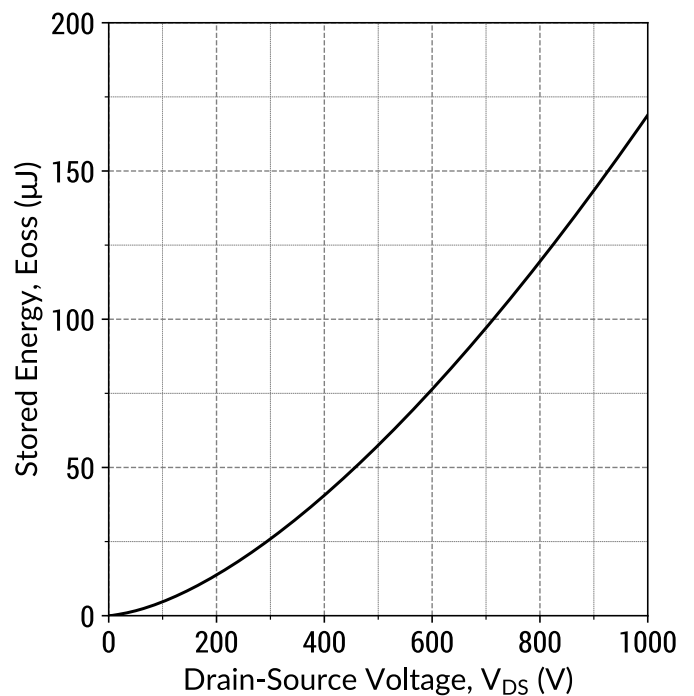
$I_D = 75 \text{ A}; V_{DS} = 1000 \text{ V}; T_C = 25^\circ\text{C}$

Figure 11: Capacitance v/s Drain-Source Voltage



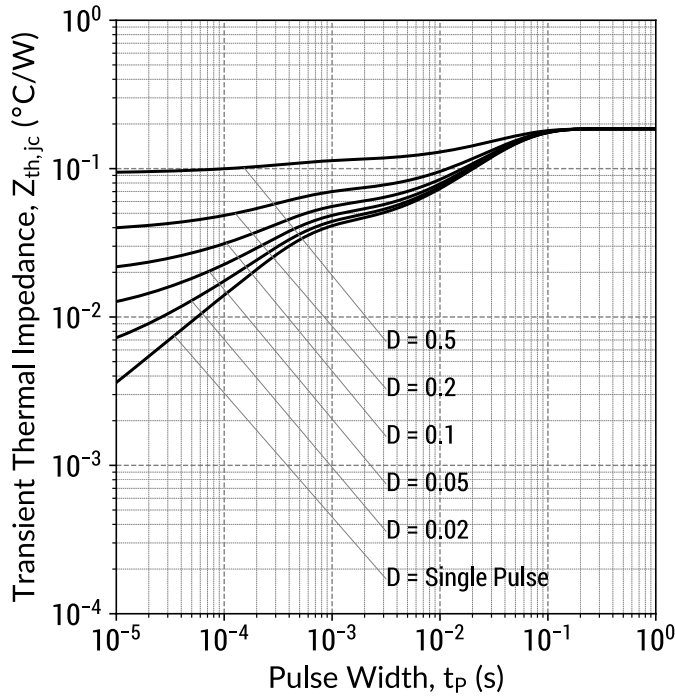
$f = 1 \text{ MHz}; V_{AC} = 25 \text{ mV}$

Figure 12: Output Capacitor Stored Energy



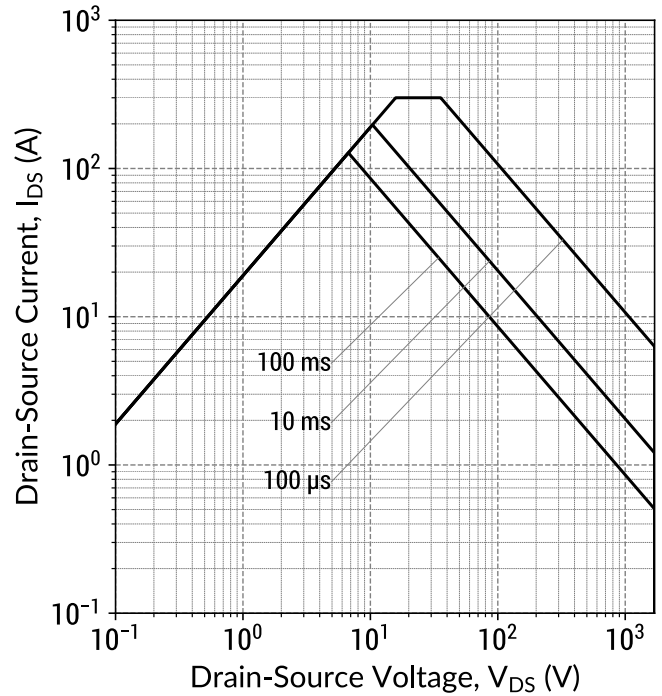
$E_{oss} = f(V_{DS})$

Figure 13: Transient Thermal Impedance



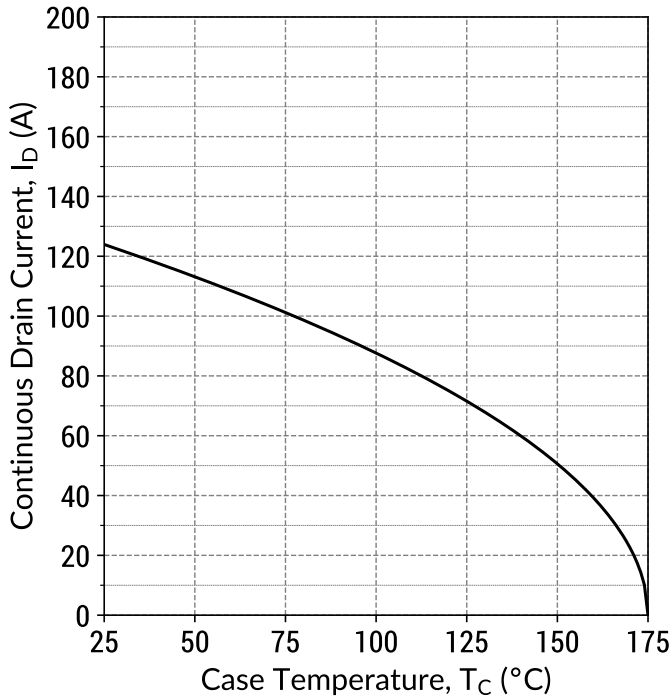
$$Z_{th,jc} = f(t_p, D); D = t_p/T$$

Figure 14: Safe Operating Area ($T_c = 25^\circ\text{C}$)



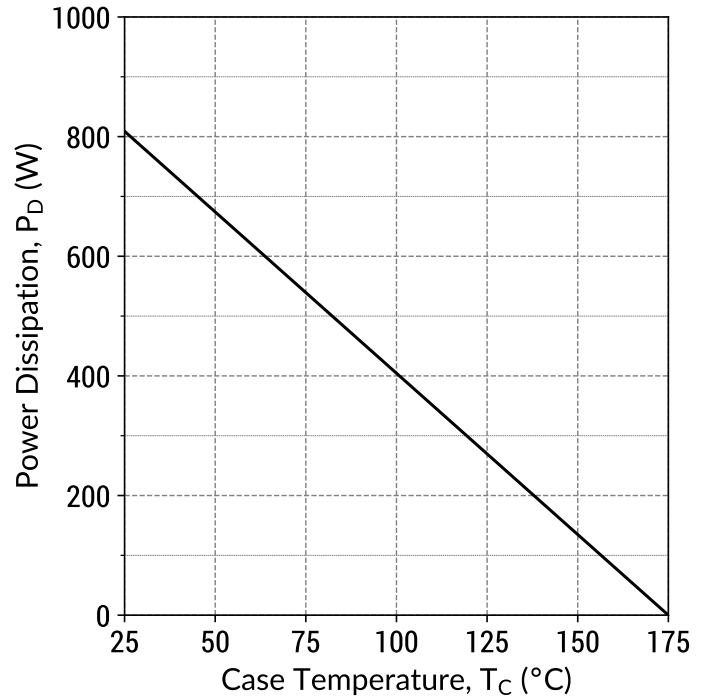
$$I_D = f(V_{DS}, t_p); T_j \leq 175^\circ\text{C}; D = 0$$

Figure 15: Current De-rating Curve



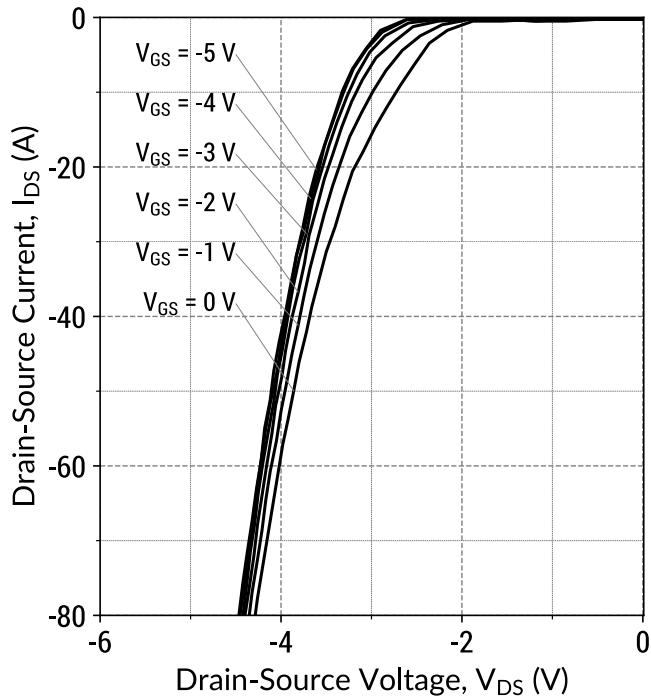
$$I_D = f(T_c); T_j \leq 175^\circ\text{C}$$

Figure 16: Power De-rating Curve



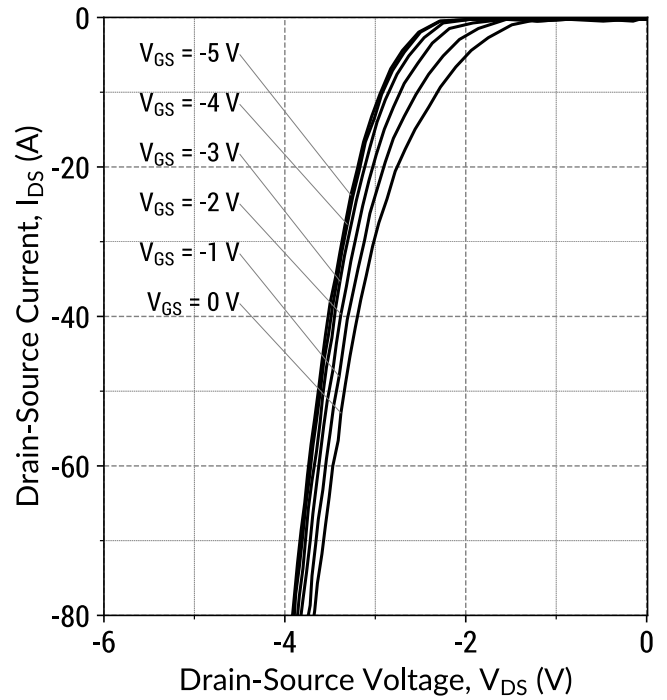
$$P_D = f(T_c); T_j \leq 175^\circ\text{C}$$

Figure 17: Body Diode Characteristics ($T_j = 25^\circ\text{C}$)



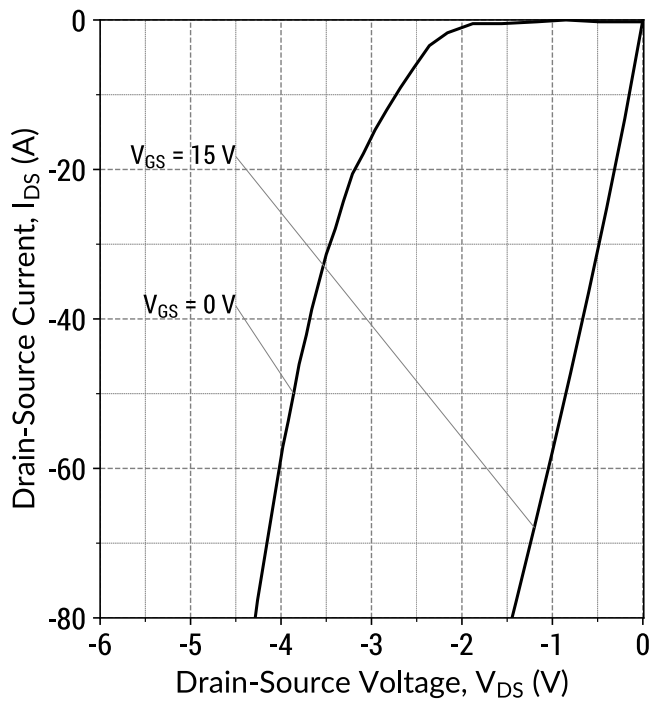
$I_D = f(V_{DS}, V_{GS}); t_P = 250 \mu\text{s}$

Figure 18: Body Diode Characteristics ($T_j = 175^\circ\text{C}$)



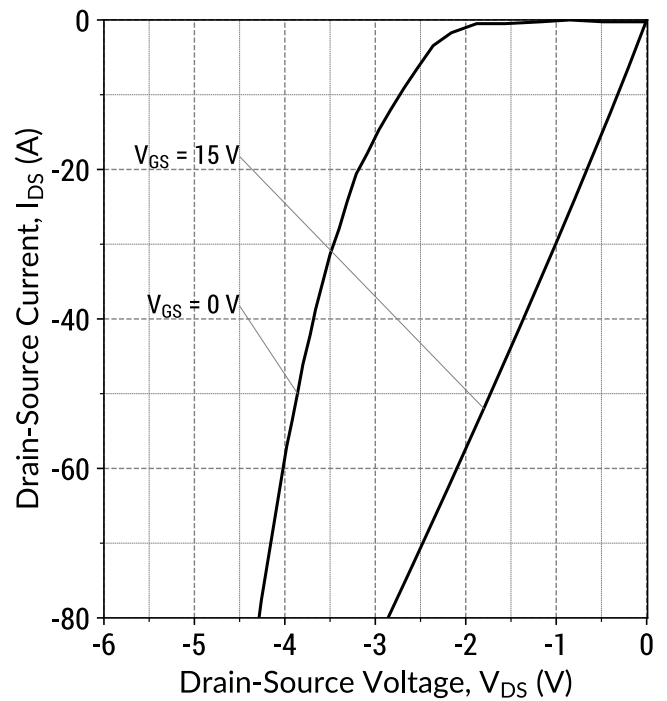
$I_D = f(V_{DS}, V_{GS}); t_P = 250 \mu\text{s}$

Figure 19: Third Quadrant Characteristics ($T_j = 25^\circ\text{C}$)



$I_D = f(V_{DS}, V_{GS}); t_P = 250 \mu\text{s}$

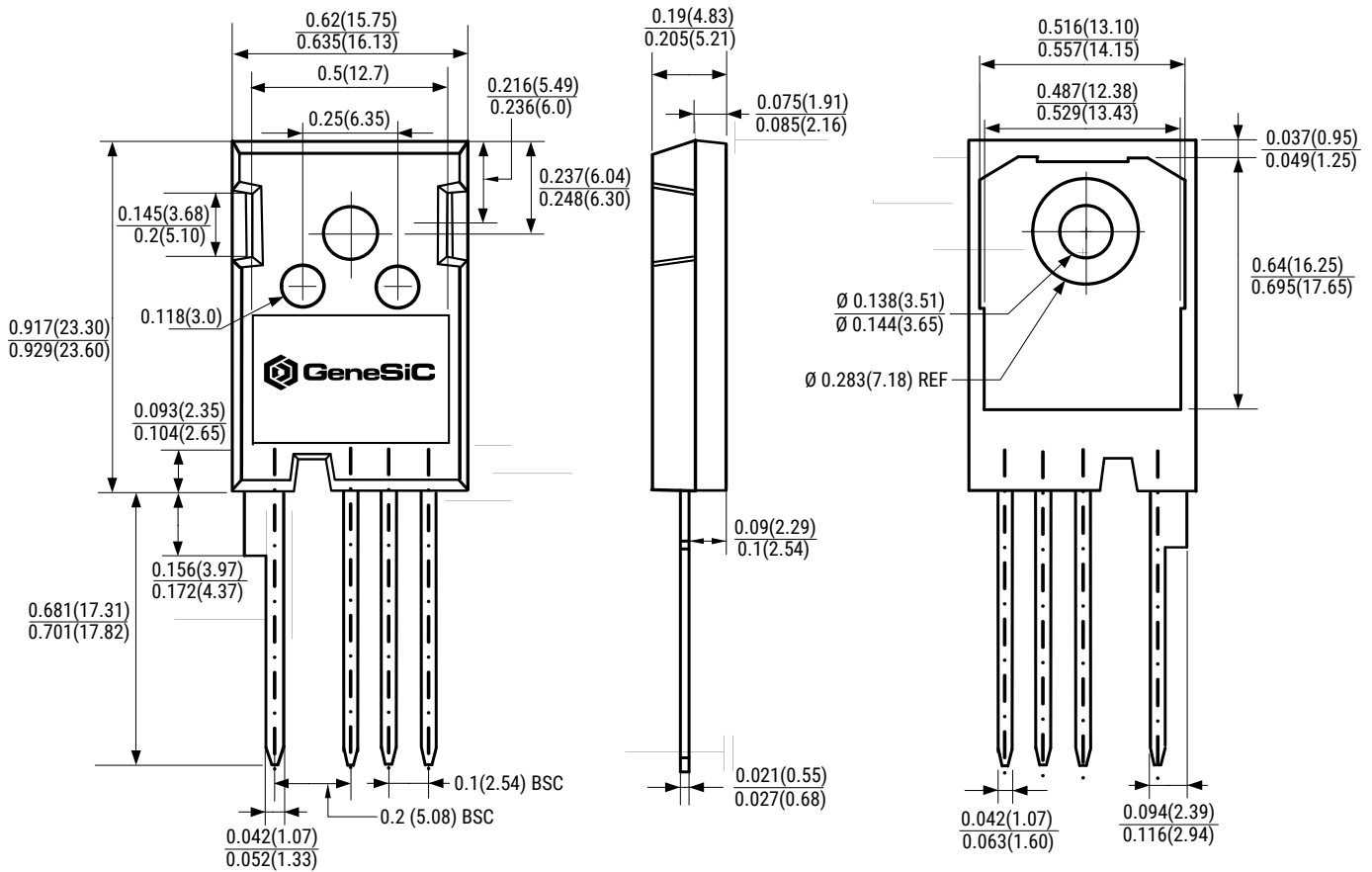
Figure 20: Third Quadrant Characteristics ($T_j = 175^\circ\text{C}$)



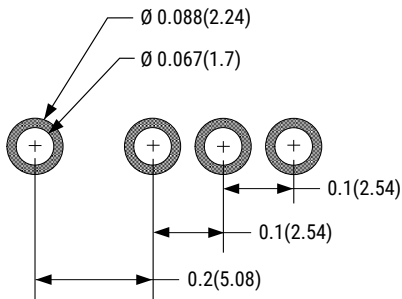
$I_D = f(V_{DS}, V_{GS}); t_P = 250 \mu\text{s}$

Package Dimensions

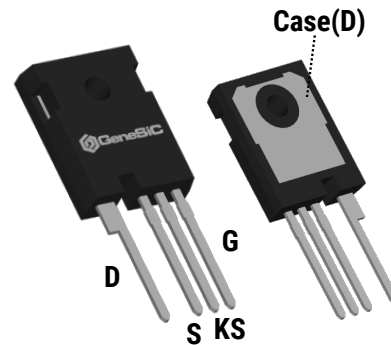
TO-247-4 Package Outline



Recommended Solder Pad Layout



Package View



NOTE

1. CONTROLLED DIMENSION IS INCH. DIMENSION IN BRACKET IS MILLIMETER.
2. DIMENSIONS DO NOT INCLUDE END FLASH, MOLD FLASH, MATERIAL PROTRUSIONS.

Compliance

RoHS Compliance

The levels of RoHS restricted materials in this product are below the maximum concentration values (also referred to as the threshold limits) permitted for such substances, or are used in an exempted application, in accordance with EU Directive 2011/65/EC (RoHS 2), as adopted by EU member states on January 2, 2013 and amended on March 31, 2015 by EU Directive 2015/863. RoHS Declarations for this product can be obtained from your GeneSiC representative.

REACH Compliance

REACH substances of high concern (SVHCs) information is available for this product. Since the European Chemical Agency (ECHA) has published notice of their intent to frequently revise the SVHC listing for the foreseeable future, please contact a GeneSiC representative to insure you get the most up-to-date REACH SVHC Declaration. REACH banned substance information (REACH Article 67) is also available upon request.

Disclaimer

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Unless otherwise expressly indicated, GeneSiC products are not designed, tested or authorized for use in life-saving, medical, aircraft navigation, communication, air traffic control and weapons systems, nor in applications where their failure may result in death, personal injury and/or property damage.

Related Links

- SPICE Models: https://www.genesicsemi.com/sic-mosfet/G3R20MT17K/G3R20MT17K_SPICE.zip
- PLECS Models: https://www.genesicsemi.com/sic-mosfet/G3R20MT17K/G3R20MT17K_PLECS.zip
- CAD Models: https://www.genesicsemi.com/sic-mosfet/G3R20MT17K/G3R20MT17K_3D.zip
- Gate Driver Reference: <https://www.genesicsemi.com/technical-support>
- Evaluation Boards: <https://www.genesicsemi.com/technical-support>
- Reliability: <https://www.genesicsemi.com/reliability>
- Compliance: <https://www.genesicsemi.com/compliance>
- Quality Manual: <https://www.genesicsemi.com/quality>

Revision History

Date	Revision	Comments	Supersedes
Sep. 28, 2020	Rev 2	Recommended Gate Voltage Changed from +20 V/-5 V to +15 V/-5 V, Rev 1	Rev 1
Jun. 2, 2020	Rev 1	Initial Release	



www.genesicsemi.com/sic-mosfet/