1K bytes EEPROM Contactless Smart Card
Conform to ISO/IEC 14443A Standard

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1. Features

- Contactless transmission of data and supply energy
- Up to 100mm operation distance
- 13.56MHz operating frequency
- 106k bit/s date rate
- High level security data communication
- True anti-collision
- 1k bytes EEPROM, organized in 16 sectors with 4 blocks of 16 bytes each
- User definable access condition for each memory block
- Data retention > 10 years
- Write endurance > 100,000 cycle
- Typical ticketing transaction < 100ms
- Three pass authentication (ISO/IEC DIS9798-2)
- Data encryption on RF-channel with replay attack protection
- Two keys per sector (per application) to support multi-application with key hierarchy
- Unique serial number for each device
- Transport key protects access to EEPROM on chip delivery
- Conform to ISO/IEC14443A standard
- Operation temperature range -25 to +70C

2. General Description

GT23SC4439A is contactless smart card IC compliant to ISO/IEC 14443A standard with 0.18um CMOS EEPROM process technology. GT23SC4439A has 1k bytes EEPROM. It has high performance security functions and contactless communication functions. GT23SC4439A can be used in payment card, public transportation card and many other applications.

3. Typical Transaction Time

- Identification of a card: 2.5ms (incl. Answer to Request, Anticollision and Select)
- Authentication: 2ms
- Read block (16 bytes): 2.5ms (excl. Authentication)
- Write block + Control Read: 4ms (excl. Authentication)
- Typical ticketing transaction: < 100ms

4. Functional Description

4.1 Block Description

The GT23SC4439A chip consists of 1k bytes EEPROM, RF Interface and Digital Control Unit. Energy and data are transferred via an antenna, which consists of a coil with a few turns directly connected to the GT23SC4439A. No further external components are necessary.

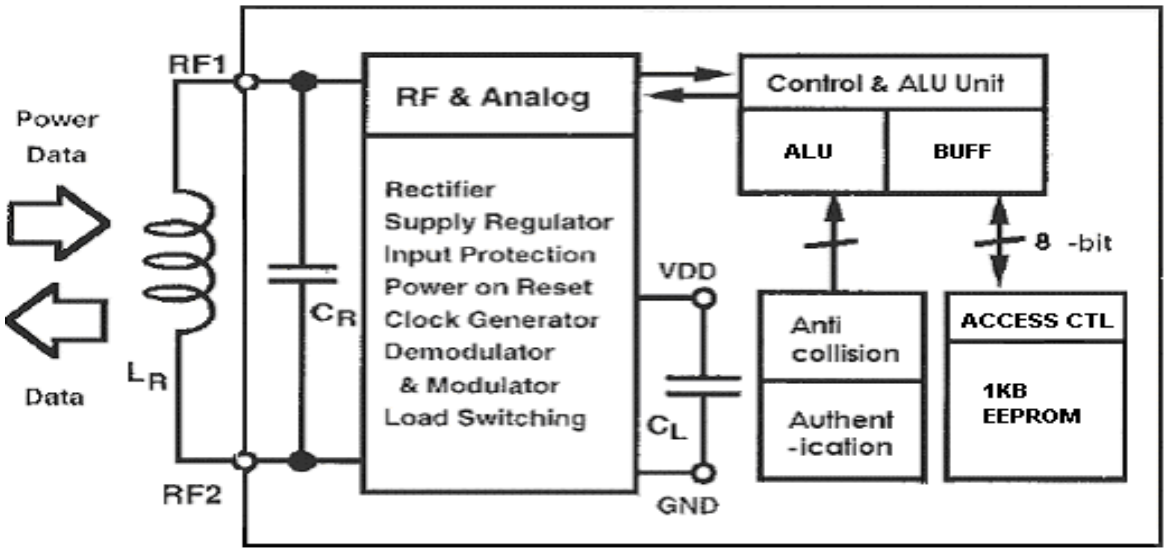

Fig. 1 Block Diagram

4.2 Communication Principle

The commands are initiated by PCD (Proximity Coupling Device) and controlled by the Digital Control Unit of GT23SC4439A according to the access conditions valid for the corresponding sector.

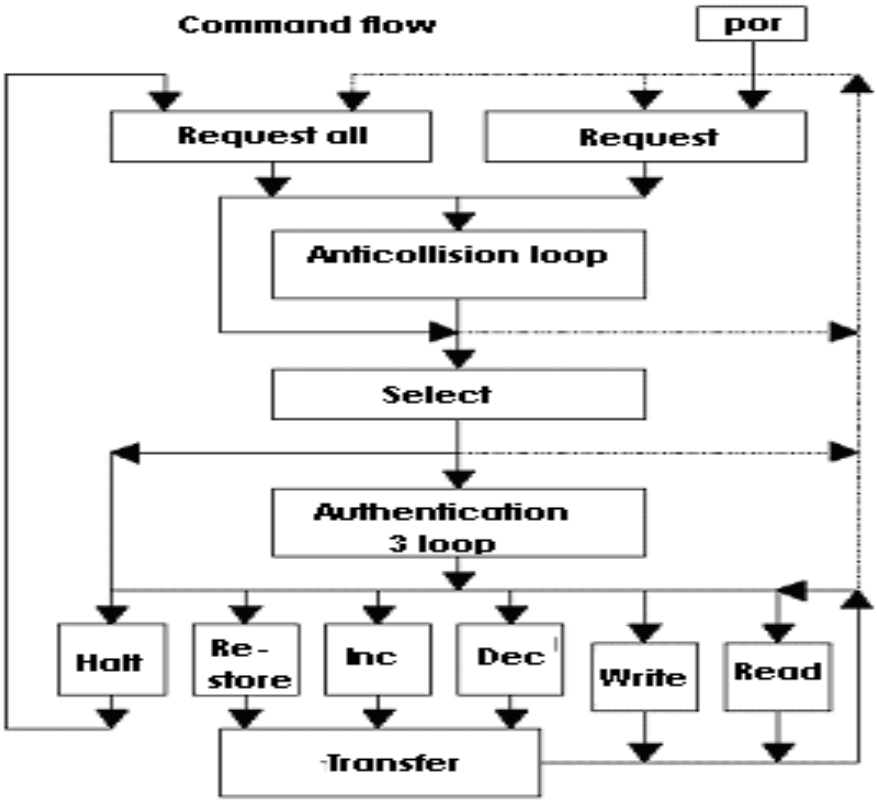

Fig. 2 Communication Flow

4.3 Data Integrity

To ensure reliable data transmission, following mechanisms are implemented in the contactless communication link between PCD and PICC:

- 16 bits CRC per block
- Parity bits for each byte
- Bit count checking
- Bit coding to distinguish between "1", "0", and no information
- Channel monitoring

4.4 Security

To provide high secure level, the triple pass authentication according to ISO 9798-2 is used in the following sequence:

a. PCD specifies the sector to be accessed and chooses key A or B.
b. PICC reads the secret key and access conditions from the sector trailer, then PICC sends a random number as the challenge to PCD (**pass one**).
c. PCD calculates the Response using the secret key and additional input. The response, together with a random challenge from PCD, is then transmitted to PICC (**pass two**).
d. PICC verifies the response of PCD by comparing it with its own challenge and then calculates the response to the challenge and transmits it (**pass three**).
e. PCD verifies the response of PICC by comparing it to its own challenge.

Note: After transmission of the first random challenge the communication between PICC and PCD is encrypted.

4.5 RF Interface

The RF interface is according to the standard for contactless ISO/IEC 14443A compatible smart card. The carrier field from PCD is always present (with short pauses when transmitting). For both directions of data communication there is only one start bit at the beginning of each frame. Each byte is transmitted with a parity bit at the end. The LSB of the byte with the lowest address of the selected block is transmitted first. The maximum frame length is 163 bits.

4.6 Memory Organization

The 1024 x 8 bit EEPROM memory is organized in 16 sectors with 4 blocks of 16 bytes each. In the erased state the EEPROM cells are read logical "1", in the written state as a logical "0".

Sector	Block	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
F	3 Trailer	KeyA						Access bits				KeyB					
	2 Data																

	1 Data																
	0 Data																
E	3 Trailer	KeyA						Access bits				KeyB					
	2 Data																
	1 Data																
	0 Data																
. . . . . .	. . . . . .																
1	3 Trailer	KeyA						Access bits				KeyB					
	2 Data																
	1 Data																
	0 Data																
0	3 Trailer	KeyA						Access bits				KeyB					
	2 Data																
	1 Data																
	0 Data	Manufacture Block															

Table 1: Memory Organizations

4.7 Memory Access

Before any memory operation can be carried out, PICC has to be selected and authenticated as described previously. The possible memory operations for an addressed block depend on the key used and the access conditions stored in the associated sector trailer.

Memory Operations		
Operation	**Description**	**Valid for Block Type**
Read	Reads one memory block	Value & Sector Trailer
Write	Writes one memory block	Value & Sector Trailer
Increment	Increments the contents of a block and stores the result in the internal data register	Value
Decrement	Decrements the contents of a block and stores the result in the internal data register	Value
Transfer	Writes the contents of the internal data register to a block	Value

Restore	Reads the contents of a block into the internal data register	Value

Table 2: Memory Operations

5. Characteristics

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.
Operating frequency			13.56MHz	
Input capacitance	25C, VCC = 3 V		16.5 pF	

6. Ordering Information

Part Number	Package
GT23SC4439A-MCxxxWBD	Sorted Wafer
GT23SC4439A-X10MCxxx-TR	Tape & Reel Module
GT23SC4439A-X20MCxxx-TR	Tape & Reel Module

7. Revision History

REV	*History*	*Page*	*Date*
1.0	Initial Version	--	3/31/2011