

# **GT24C64**

## **2-Wire**

### **64Kb Serial EEPROM (Smart Card application)**

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## 1 FEATURES

- Two-Wire Serial Interface, I<sup>2</sup>C™ Compatible
  - Bi-directional data transfer protocol
- Wide-voltage Operation
  - V<sub>cc</sub> = 1.8V to 5.5V
- Speed: 400 KHz (1.8V) and 1 MHz (2.5V~5.5V)
- Standby current: 1 μA (max.)
- Operating current: 3 mA (max.)
- Hardware Data Protection
  - Write Protect the entire array
- Sequential & Random Read Features
- Memory organization: 8k x 8
- Page Size: 32 bytes
- Page write mode
  - Up to 32 bytes per page write
- Self timed write cycle with auto clear: 5 ms (max.)
- Filtered inputs for noise suppression
- High-reliability
  - Endurance: 1 million cycles
  - Data retention: 10 years
- Wide operating temperature range
  - -30°C to +75°C

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## **2 DESCRIPTION**

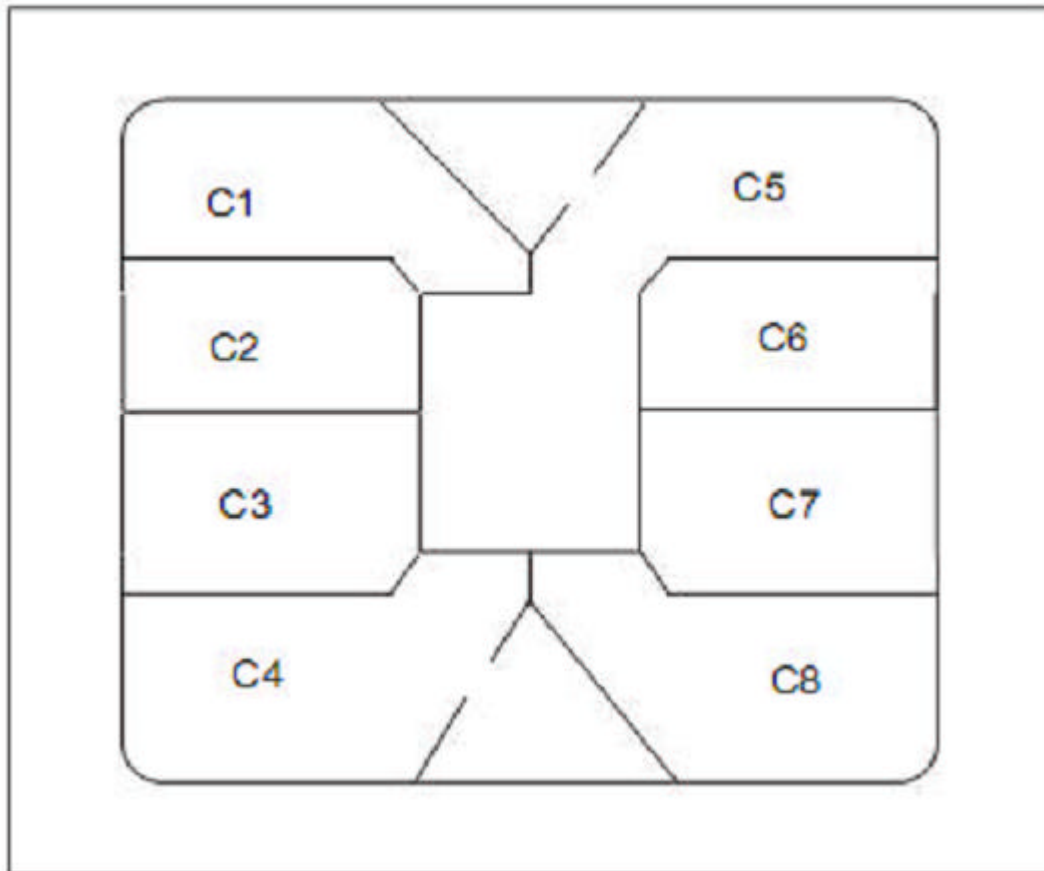
The GT24C64 are EEPROM device that uses the industrial standard 2-wire interface for communications. This EEPROM contains an embedded memory array of 64K-bits (8,192x8), which is organized in 32-byte per page.

The GT24C64 operates in a wide voltage range from 1.8V to 5.5V which fits most application. This device utilizes the CMOS technology to provide low-power operations.

The GT24C64 is fully compatible with the industrial standard 2-wire bus protocol. If in case the bus is not responded, a new sent Opcode command will reset the bus and the device will respond correctly. The simple bus consists of the Serial Clock wire (SCL) and the Serial Data wire (SDA). Utilizing such bus protocol, a Master device, such as a microcontroller, can usually control one or more Slave devices, alike this GT24C64. The bit stream over the SDA line includes a series of bytes, which identifies a particular Slave device, an instruction, an address within that Slave device, and a series of data, if appropriate.

In order to refrain the state machine entering into a wrong state during power-up sequence or a power toggle off-on condition, a power on reset circuit is embedded. During power-up, the device does not respond to any instructions until the supply voltage ( $V_{CC}$ ) has reached an acceptable stable level above the reset threshold voltage. Once  $V_{CC}$  passes the power on reset threshold, the device is reset and enters into the Standby mode. This would also avoid any inadvertent Write operations during power-up stage. During power-down process, the device will enter into standby mode, once  $V_{CC}$  drops below the power on reset threshold voltage. In addition, the device will be in standby mode after receiving the Stop command, provided that no internal write operation is in progress. Nevertheless, it is not recommended to send any command until the  $V_{cc}$  reaches its operating level.

**3 PIN CONFIGURATION**



## **4 PIN DESCRIPTIONS**

### **SCL (C3)**

This input clock pin is used to synchronize the data transfer to and from the device.

### **SDA (C7)**

The SDA is a bi-directional pin used to transfer addresses and data into and out of the device. The SDA pin is an open drain output and can be wired with other open drain or open collector outputs. However, the SDA pin requires a pull-up resistor connected to the power supply.

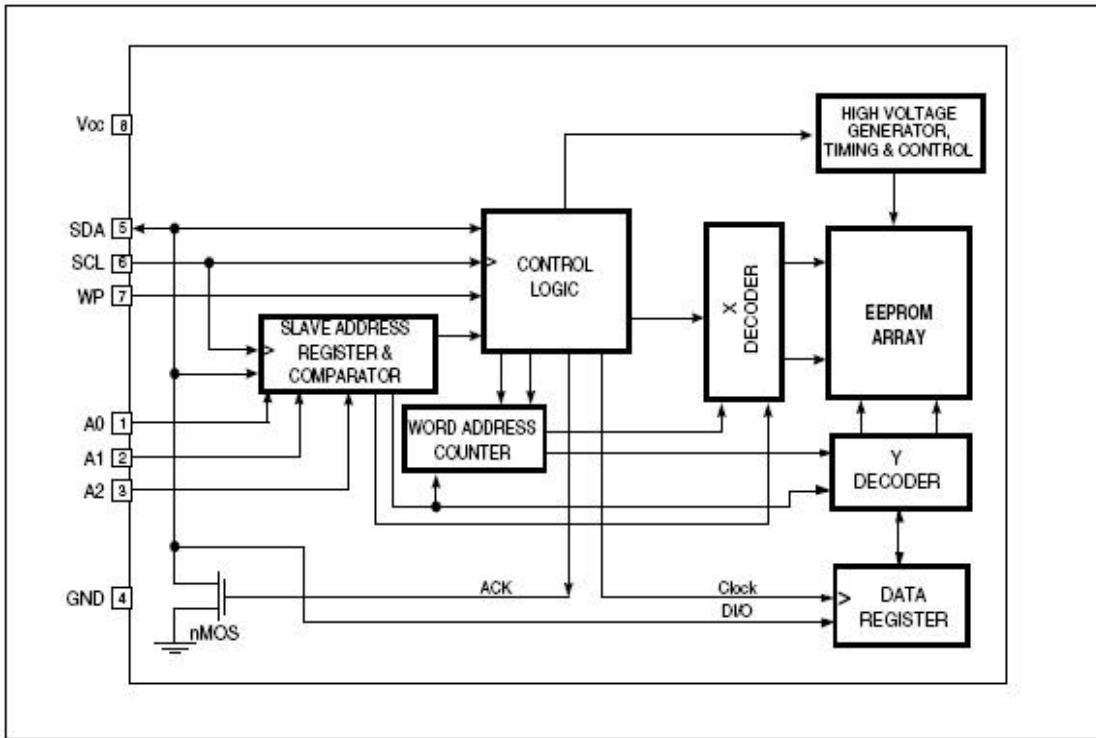
### **Vcc (C1)**

Supply voltage

### **GND (C5)**

Ground of supply voltage

### 5 BLOCK DIAGRAM



## 6 DEVICE OPERATION

The GT24C64 serial interface supports communications using industrial standard 2-wire bus protocol, namely I<sup>2</sup>C.

### 2-WIRE BUS

The two-wire bus is defined as a Serial Data line (SDA), and a Serial Clock line (SCL). The protocol defines any device that sends data onto the SDA bus as a transmitter, and the receiving devices as receivers. The bus is controlled by Master device that generates the SCL, controls the bus access, and generates the Stop and Start conditions. The GT24C64 is the Slave device on the bus.

#### The Bus Protocol:

- Data transfer may be initiated only when the bus is not busy
- During a data transfer, the SDA line must remain stable whenever the SCL line is high. Any changes in the SDA line while the SCL line is high will be interpreted as a Start or Stop condition.

The state of the SDA line represents valid data after a Start condition. The SDA line must be stable for the duration of the High period of the clock signal. The data on the SDA line may be changed during the Low period of the clock signal. There is one clock pulse per bit of data. Each data transfer is initiated with a Start condition and terminated with a Stop condition.

#### Start Condition

The Start condition precedes all commands to the device and is defined as a High to Low transition of SDA when SCL is High. The EEPROM monitors the SDA and SCL lines and will not respond until the Start condition is met.

#### Stop Condition

The Stop condition is defined as a Low to High transition of SDA when SCL is High. All operations must end with a Stop condition.

#### Acknowledge (ACK)

After a successful data transfer, each receiving device is required to generate an ACK. The Acknowledging device pulls down the SDA line.

#### Reset

The GT24C64 contains a reset function in case the 2-wire bus transmission is accidentally interrupted (e.g. a power loss), or needs to be terminated mid-stream. The reset is caused when the Master device creates a Start condition. To do this, it may be necessary for the Master device to monitor the SDA line while cycling the SCL up to nine times. (For each clock signal transition to High, the Master checks for a High level on SDA.)

#### Standby Mode

The standby mode permits the minimal power consumption. The GT24C64 enters the standby state in either one of the following conditions: a) At Power-up, and remain in it until SCL or SDA toggles; b) Following the Stop signal if a no write operation is initiated; or c) After the completion of an internal write operation.



## **DEVICE ADDRESSING**

The Master begins a transmission by sending a Start condition. The Master then sends the address of the particular Slave devices it is requesting. The Slave device (Fig. 5) address is 8 bits.

The four most significant bits of the Slave address are fixed as 1010 for the GT24C64.

The next three bits of the Slave address are specific for each of the EEPROM. The bit values enable access to multiple memory blocks or multiple devices.

The GT24C64 uses the bits A0, A1, and A2 to address internal memory in the device.

The last bit of the Slave address specifies whether a Read or Write operation is to be performed. When this bit is set to 1, a Read operation is selected, and when set to 0, a Write operation is selected.

After the Master transmits the Start condition and Slave address byte (Fig. 5), the appropriate 2-wire Slave (e.g. GT24C64) will respond with ACK on the SDA line. The Slave will pull down the SDA on the ninth clock cycle, signaling that it received the eight bits of data. Then the selected EEPROM prepares for a Read or Write operation by monitoring the bus.

## **WRITE OPERATION**

### **Byte Write**

In the Byte Write mode, the Master device sends the Start condition and the Slave address information (with the R/W set to Zero) to the Slave device. After the Slave generates an ACK, the Master sends the byte address that is to be written into the address pointer of the GT24C64. After receiving another ACK from the Slave, the Master device transmits the data byte to be written into the address memory location. The GT24C64 acknowledges once more and the Master generates the Stop condition, at which time the device begins its internal programming cycle. While this internal cycle is in progress, the device will not respond to any request from the Master device.

### **Page Write**

The GT24C64 is capable of 32 bytes Page-Write operation. A Page-Write is initiated in the same manner as a Byte Write, but instead of terminating the internal Write cycle after the first data word is transferred, the Master device can transmit up to 31 more bytes. After the receipt of each data word, the EEPROM responds immediately with an ACK on SDA line, and the five lower order data word address bits are internally incremented by one, while the higher order bits of the data word address remain constant. If a byte address is incremented from the last byte of a page, it returns to the first byte of that page. If the Master device should transmit more than 32 bytes prior to issuing the Stop condition, the address counter will “roll over,” and the previously written data will be overwritten. Once all 32 bytes are received and the Stop condition has been sent by the Master, the internal programming cycle begins. At this point, all received data is written to the GT24C64 in a single Write cycle. All inputs are disabled until completion of the internal Write cycle.

### **Acknowledge (ACK) Polling**

The disabling of the inputs can be used to take advantage of the typical Write cycle time. Once the Stop condition is issued to indicate the end of the host's Write operation, the GT24C64 initiates the internal Write cycle. ACK polling can be initiated immediately. This involves issuing the Start condition followed by the Slave address for a Write operation. If the EEPROM is still busy with the Write operation, no ACK will be returned. If the GT24C64 has completed the Write operation, an ACK will be returned and the host can then proceed with the next Read or Write operation.

## **READ OPERATION**

Read operations are initiated in the same manner as Write operations, except that the (R/W) bit of the Slave address is set to “1”. There are three Read operation options: current address read, random address read and sequential read.

### Current Address Read

The GT24C64 contains an internal address counter which maintains the address of the last byte accessed, incremented by one. For example, if the previous operation is either a Read or Write operation addressed to the address location  $n$ , the internal address counter would increment to address location  $n+1$ . When the EEPROM receives the Slave Addressing Byte with a Read operation (R/W bit set to “1”), it will respond an ACK and transmit the 8-bit data byte stored at address location  $n+1$ . The Master should not acknowledge the transfer but should generate a Stop condition so the GT24C64 discontinues transmission. If 'n' is the last byte of the memory, the data from location '0' will be transmitted. (Refer to Figure 8. Current Address Read Diagram.)

### Random Address Read

Selective Read operations allow the Master device to select at random any memory location for a Read operation. The Master device first performs a 'dummy' Write operation by sending the Start condition, Slave address and byte address of the location it wishes to read. After the GT24C64 acknowledges the byte address, the Master device resends the Start condition and the Slave address, this time with the R/W bit set to one. The EEPROM then responds with its ACK and sends the data requested. The Master device does not send an ACK but will generate a Stop condition. (Refer to Figure 9. Random Address Read Diagram.)

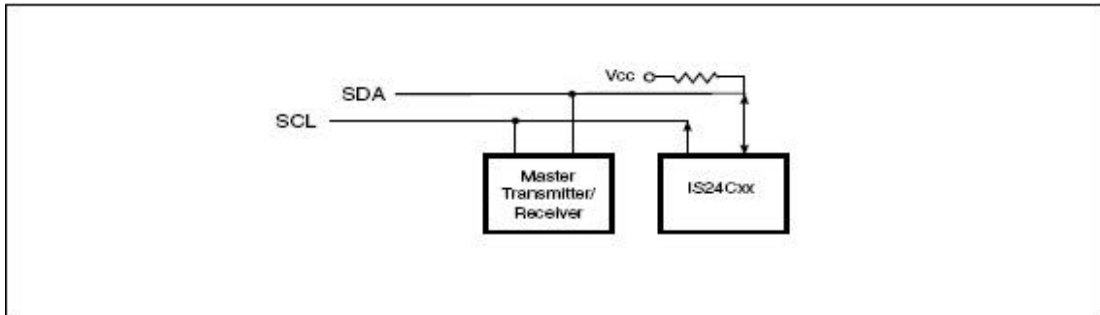
### Sequential Read

Sequential Reads can be initiated as either a Current Address Read or Random Address Read. After the GT24C64 sends the initial byte sequence, the Master device now responds with an ACK indicating it requires additional data from the GT24C64. The EEPROM continues to output data for each ACK received. The Master device terminates the sequential Read operation by pulling SDA High (no ACK) indicating the last data word to be read, followed by a Stop condition.

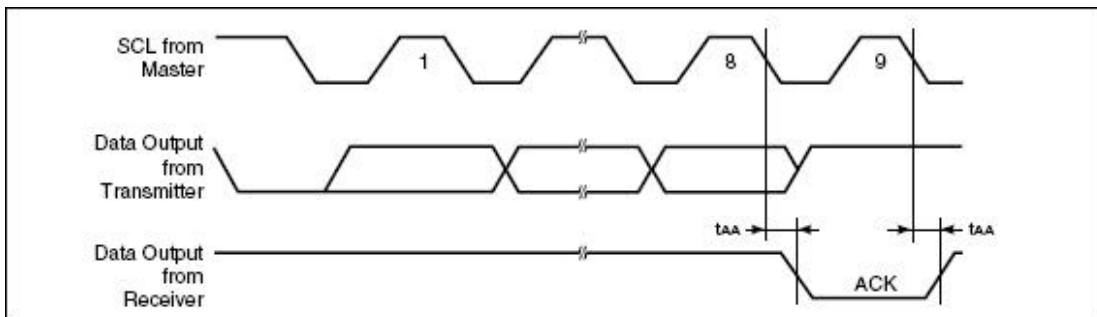
The data output is sequential, with the data from address  $n$  followed by the data from address  $n+1, n+2 \dots$  etc. The address counter automatically increments by one, allowing the entire memory contents to be serially read during sequential Read operation. When the memory address boundary of the array is reached, the address counter “rolls over” to address 0, and the device continues to output data. (Refer to Figure 10. Sequential Read Diagram).

## 7 TIMING DIAGRAMS

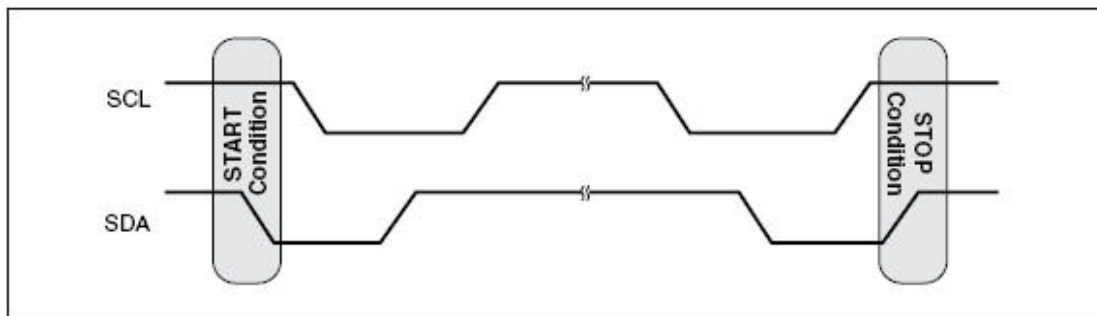
**Figure 1: Typical System Bus Configuration**



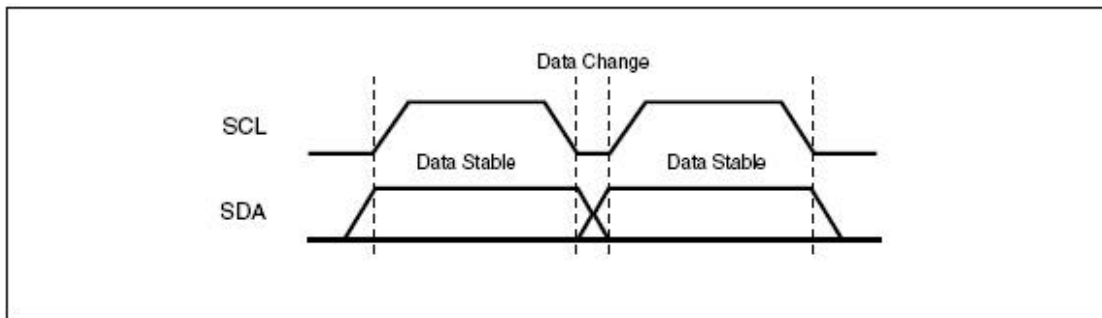
**Figure 2: output Acknowledge**



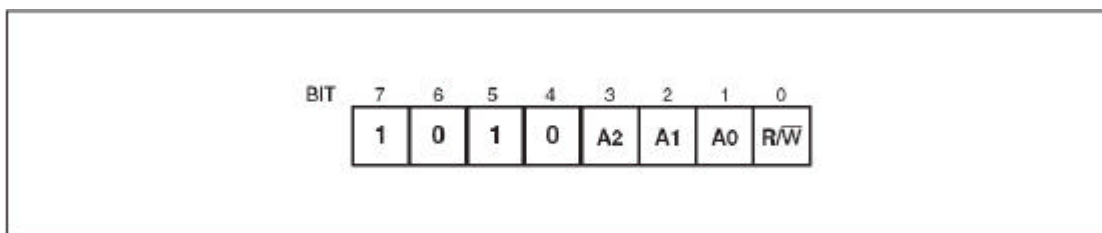
**Figure 3: Start and Stop Conditions**



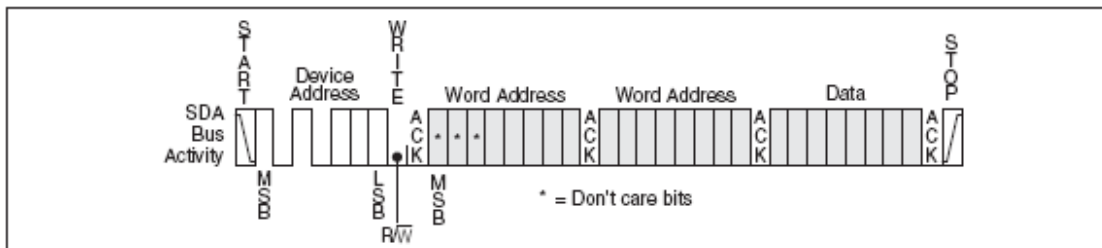
**Figure 4: Data Validity Protocol**



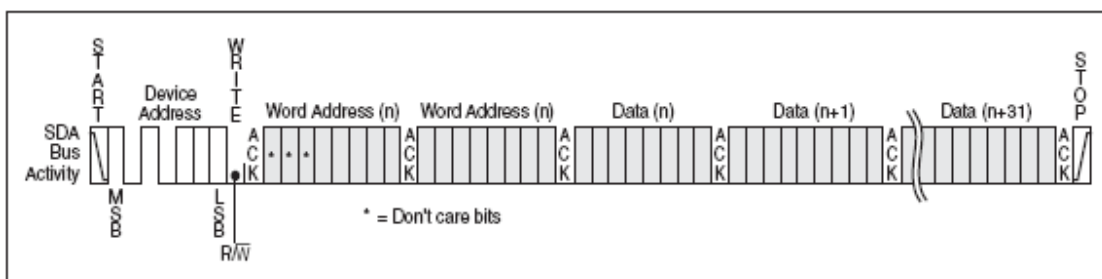
**Figure 5: Slave Address**



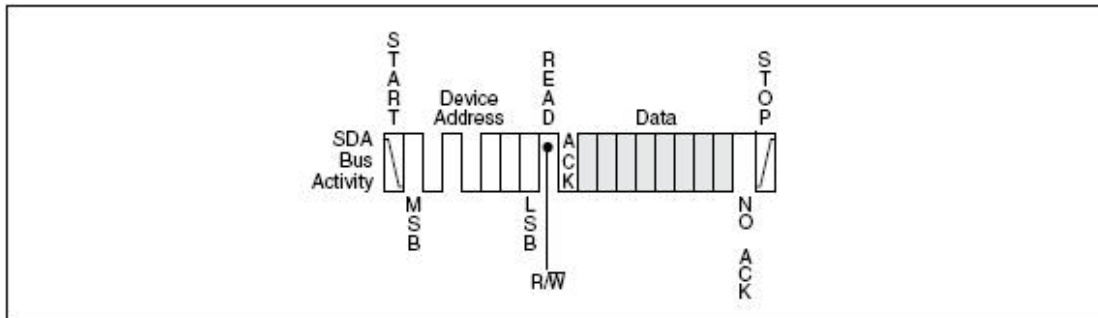
**Figure 6: Byte Write**



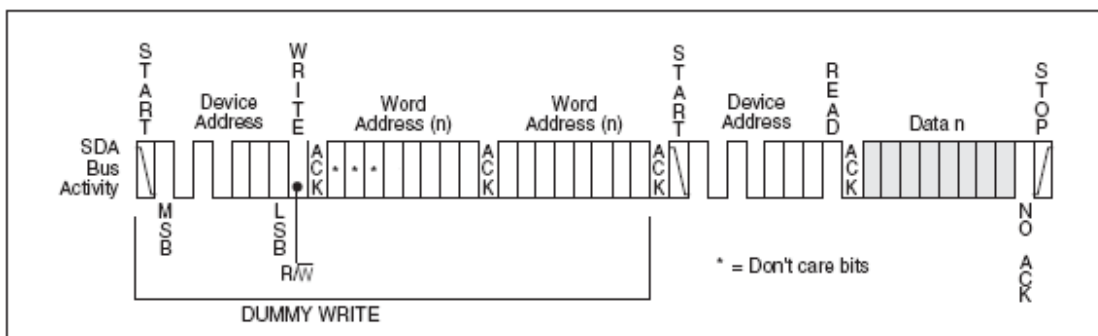
**Figure 7: Page Write**



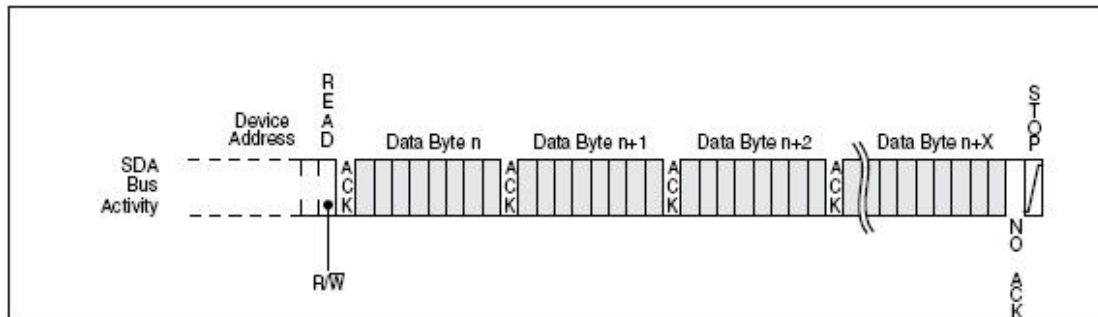
**Figure 8: Current Address Read**



**Figure 9: Random Address Read**

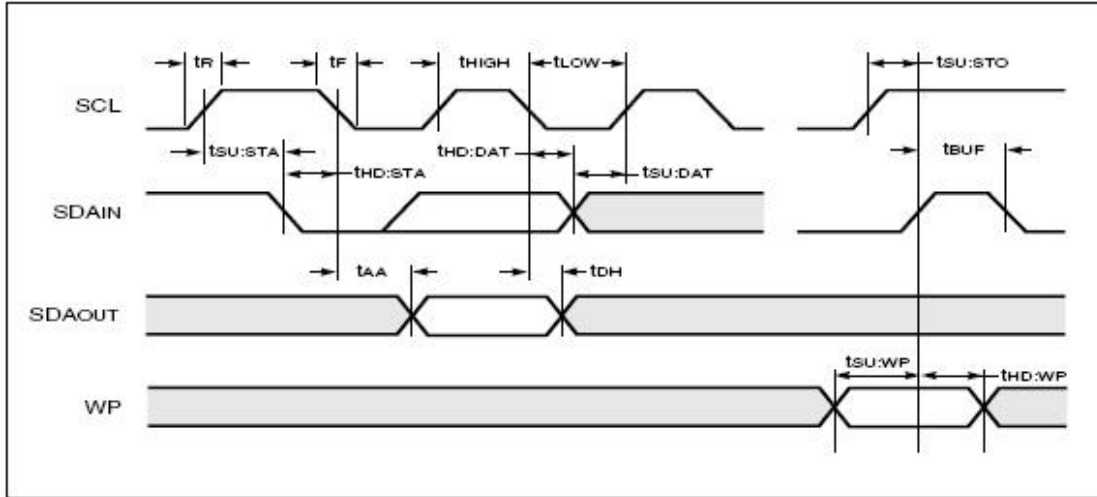


**Figure 10: Sequential Read**

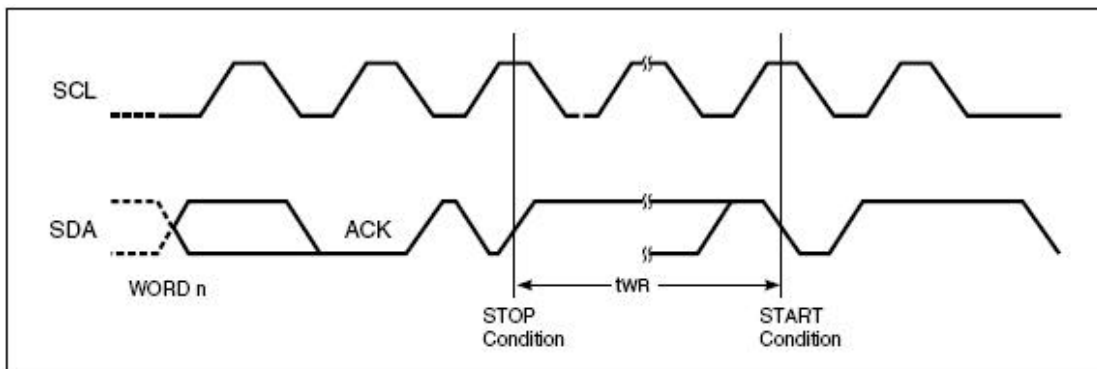


**AC Timing**

**Figure 11: Bus Timing**



**Figure 12: Write Cycle Timing**



## 8 ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V <sub>S</sub>	Supply Voltage	-0.5 to + 6.5	V
V <sub>P</sub>	Voltage on Any Pin	-0.5 to V <sub>CC</sub> + 0.5	V
T <sub>BIAS</sub>	Temperature Under Bias	-55 to +125	°C
T <sub>STG</sub>	Storage Temperature	-65 to +150	°C
I <sub>OUT</sub>	Output Current	5	mA

**Notes:**

Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## OPERATING RANGE

<b>Ambient Temperature (T<sub>A</sub>)</b>	<b>V<sub>CC</sub></b>
-30° C to +75° C	1.8V to 5.5V

## CAPACITANCE <sup>[1,2]</sup>

Symbol	Parameter	Conditions	Max.	Unit
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 0V	6	pF
C <sub>I/O</sub>	Input /Output Capacitance	V <sub>I/O</sub> = 0V	8	pF

**Notes:**

1. Tested initially and after any design or process changes that may affect these parameters and not 100% tested.
2. Test conditions: T<sub>A</sub> = 25°C, f = 1 MHz, V<sub>CC</sub> = 5.0V.

## 9 DC ELECTRICAL CHARACTERISTICS

Industrial:  $T_A = -30^\circ\text{C}$  to  $+75^\circ\text{C}$ ,  $V_{CC} = 1.8\text{V} \sim 5.5\text{V}$

Symbol	Parameter <sup>[1]</sup>	Vcc	Test Conditions	Min.	Max.	Unit
$V_{CC}$	Supply Voltage			1.8	5.5	V
$V_{IH}$	Input High Voltage (SDA, SCL, WP)			$0.7 \cdot V_{CC}$	$V_{CC}+1$	V
$V_{IL}$	Input Low Voltage (SDA, SCL, WP)			-1	$0.3 \cdot V_{CC}$	V
$I_{LI}$	Input Leakage Current (SDA, SCL, WP, A0, A1 & A2)	5V	$V_{IN} = 0\text{V} \sim V_{CC}$ , standby mode	--	2	$\mu\text{A}$
$I_{LO}$	Output Leakage Current	5V	$V_{OUT} = 0\text{V} \sim V_{CC}$ , SDA in Hi-Z	--	2	$\mu\text{A}$
$V_{OL1}$	Output Low Voltage	1.8V	$I_{OL} = 0.15\text{mA}$	—	0.2	V
$V_{OL2}$	Output Low Voltage	3V	$I_{OL} = 2.1\text{mA}$	—	0.4	V
$I_{SB1}$	Standby Current	1.8V	$V_{IN} = V_{CC}$ or GND	—	1	$\mu\text{A}$
		2.5V	$V_{IN} = V_{CC}$ or GND	—	1	$\mu\text{A}$
		5V	$V_{IN} = V_{CC}$ or GND	—	1	$\mu\text{A}$
$I_{CC1}$	Read Current	1.8V	Read at 400 KHz	—	1	mA
		2.5V	Read at 1 MHz	—	1	mA
		5.5V	Read at 1 MHz	—	2	mA
$I_{CC2}$	Write Current	1.8V	Write at 400 KHz	—	1	mA
		2.5V	Write at 1 MHz	—	2	mA
		5.5V	Write at 1 MHz	—	3	mA

Notes: <sup>[1]</sup> The parameters are characterized but not 100% tested.



## 10 AC ELECTRICAL CHARACTERISTICS

$T_A = -30^\circ\text{C}$  to  $+75^\circ\text{C}$ , Supply voltage = 1.8V to 5.5V

Symbol	Parameter <sup>[1,2]</sup>	1.8V $\leq$ Vcc < 2.5V		2.5V $\leq$ Vcc < 4.5V		4.5V $\leq$ Vcc $\leq$ 5.5V		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
$f_{\text{SCL}}$	SCK Clock Frequency		400		1000		1000	KHz
$t_{\text{LOW}}$	Clock Low Period	1200	—	400	—	400	—	ns
$t_{\text{high}}$	Clock High Period	600	—	400	—	400	—	ns
$T_r$	SCL and SDA Rise Time <sup>(1)</sup>	—	300	—	300	—	300	ns
$T_f$	SCL and SDA Fall Time <sup>(1)</sup>	—	300	—	100	—	100	ns
$t_{\text{su:sta}}$	Start Condition Setup Time	500	—	200	—	200	—	ns
$t_{\text{su:sto}}$	Stop Condition Setup Time	500	—	200	—	200	—	ns
$t_{\text{hd:sta}}$	Start Condition Hold Time	500	—	200	—	200	—	ns
$t_{\text{su:dat}}$	Data In Setup Time	100	—	40	—	40	—	ns
$t_{\text{hd:dat}}$	Data In Hold Time	0	—	0	—	0	—	ns
$T_{\text{aa}}$	Clock to Output (SCL Low to SDA Data Out Valid) Access time	100	900	50	400	50	400	ns
$T_{\text{dh}}$	Data Out Hold Time (SCL Low to SDA Data Out Change)	100	—	50	—	50	—	ns
$t_{\text{wr}}$	Write Cycle Time	—	5	—	5	—	5	ms
$t_{\text{buf}}$	Bus Free Time Before New Transmission <sup>(1)</sup>	1000	—	400	—	400	—	ns
$t_{\text{su:wp}}$	WP pin Setup Time	1000	—	400	—	400	—	ns
$t_{\text{hd:wp}}$	WP pin Hold Time	1000	—	400	—	400	—	ns
$T$	Noise Suppression Time	—	100	—	50	—	50	ns

**Notes:** 1. The parameters are characterized but not 100% tested.

2. AC measurement conditions:

$R_L$  (connects to Vcc): 1.3 k $\Omega$  (2.5V, 5.0V), 10 k $\Omega$  (1.8V)

$C_L = 100$  pF

Input pulse voltages: 0.3 Vcc to 0.7 Vcc

Input rise and fall times: = 50 ns

Timing reference voltages: half Vcc level

**11 ORDERING INFORMATION**

Voltage Range	Part Number*	Package
1.8V to 5.5V	GT24C64-X07M-TR	Tape module

## 12 REVISION HISTORY

Revision	Date	Descriptions
a0	Mar 2010	Initial version