GT25C128A

SPI

128K Bits

Serial EEPROM

Table of Contents

1. Features

- Serial Peripheral Interface (SPI) Compatible
  - Supports Mode 0 (0,0) and Mode 3 (1,1)
- Wide-voltage Operation
  - V_{CC} = 1.7V to 5.5V
- Low power CMOS
  - Standby current: ≤1 μA (1.7V)
  - Operating current: ≤2 mA (1.7V)
- Operating frequency: 20 MHz (5.5V)
- Memory organization: 128Kb (16,384 x 8)
- Byte and Page write (up to 64 bytes)
  - Partial page write allowed
- Block Write Protection
  - Protect 1/4, 1/2, or Entire Array
- Additional Write lockable Page (Identification page)
- Self timed write cycle: 5 ms (max.)
- High-reliability
  - Endurance: 1 million cycles
  - Data retention: 100 years
- Industrial temperature grade
- Packages (8-pin): SOIC, TSSOP and UDFN
- Lead-free, RoHS, Halogen free, Green

2. General Description

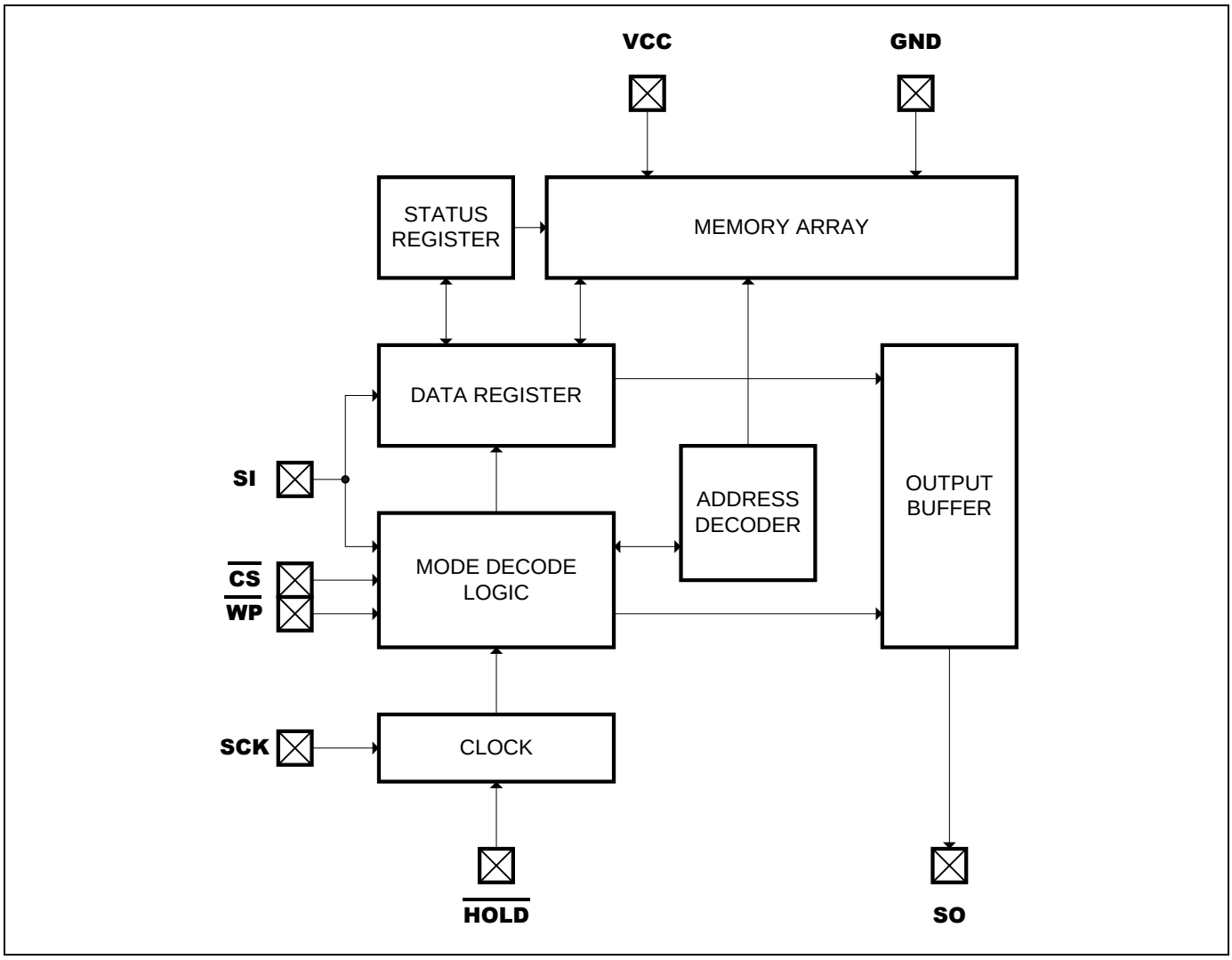
The GT25C128A is an industrial standard electrically erasable programmable read only memory (EEPROM) product that utilizes standard Serial Peripheral Interface (SPI) for communications. The GT25C128A contains a memory array of 128K bits (16,384x 8), which is organized in 64 bytes per page.

This EEPROM operates in a wide voltage range from 1.7V to 5.5V, which fits most application. The device provides low-power operations and low standby current. The product is offered in Lead-free, RoHS, halogen free or Green package. The available package types are 8-pin SOIC, TSSOP and UDFN.

The functionalities of the GT25C128A are optimized for most applications, such as consumer electronics, wireless, telecommunication, industrial, medical, instrumentation, commercial and others, where low-power and low-voltage are vital. This product has a compatible SPI interface: Chip-Select ($\overline{CS}$), Serial Data In (SI), Serial Data Out (SO) and Serial Clock (SCK) for high-speed communication. Furthermore, a Hold feature via $\overline{HOLD}$ pin allows the device entering into a suspended state whenever necessary and resuming the communication without re-initializing the serial sequence. A Status Register facilitates a flexible write protection mechanism and device status monitoring. The GT25C128A also offers an additional page, named the Identification Page (64 bytes) which can be written and (later) permanently locked in Read-only mode. This Identification Page offers flexibility in the application board production line, as the Identification Page can be used to store unique identification parameters and/or parameters specific to the production line.

In order to refrain the state machine from entering into a wrong state during power-up sequence or a power toggle off-on condition, a power on reset circuit is implemented. During power-up, the device does not respond to any instructions until the supply voltage (V_{CC}) has reached an acceptable stable level above the reset threshold voltage. Once V_{CC} passes the power on reset threshold, the device is reset and enters into Standby mode. This should also avoid any inadvertent Write operations during power-up stage. During power-down process, the device will enter into standby mode, once V_{CC} drops below the power on reset threshold voltage. In addition, the device will be in standby mode after receiving the Stop command, provided that no internal write operation is in progress. Nevertheless, it is illegal to send a command unless the V_{CC} is within its operating level.

3. Functional Block Diagram



Serial Interface Description

Master: The device that provides a clock signal.

Slave: GT25C128A.

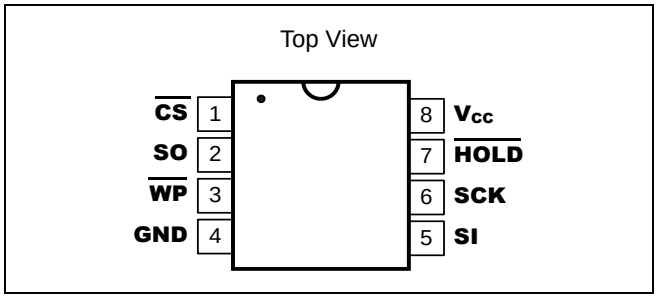
Transmitter/Receiver: The GT25C128A has both data input (SI) and data output (SO).

MSB MSB (Most Significant Bit) is the first bit being transmitted or received.

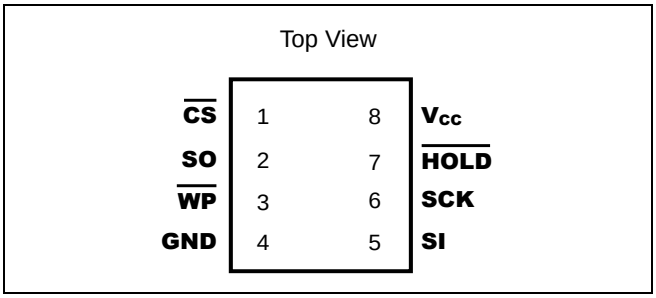
Op-Code: Operational instruction code typically sent to the GT25C128A is the first byte of information transmitted after $\overline{CS}$ is Low. If the Op-Code is a valid instruction as listed in Table 5.3, then it will be decoded appropriately. It is prohibited to send an invalid Op-Code.

4. Pin Configuration

4.1 8-Pin SOIC and TSSOP



4.2 8-Lead UDFN



4.3 Pin Definition

Pin No.	Pin Name	I/O	Definition
1	$\overline{CS}$	I	Chip Select
2	SO	O	Serial Data Output
3	$\overline{WP}$	I	Write Protect Input
4	GND	-	Ground
5	SI	I	Serial Data Input
6	SCK	I	Serial Clock
7	$\overline{HOLD}$	I	Hold function
8	V_{CC}	-	Supply Voltage

4.4 Pin Descriptions

Chip Select ($\overline{CS}$)

The $\overline{CS}$ pin is used to enable or disable the device. Upon power-up, $\overline{CS}$ must follow the supply voltage. When the device is ready for instruction input, this signal requires a High-to-Low transition. Once $\overline{CS}$ is stable at Low, the device is enabled. Then the master and slave can communicate among each other through SCK, SI, and SO pins. Upon completion of transmission, $\overline{CS}$ must be driven to High in order to stop the operation or start the internal write operation. And the device will enter into standby mode, unless an internal write operation is in progress. During this mode, SO becomes high impedance.

Serial Clock (SCK)

Under the SPI modes (0, 0) and (1, 1), this clock signal provides synchronization between the master and GT25C128A. Typically, Op-Codes, addresses and data are latched from SI at the rising edge of SCK, while data from SO are clocked out at the falling edge of SCK.

Serial Data Input (SI)

Data Input pin.

Serial Data Output (SO)

Data output pin.

Write Protect ($\overline{WP}$)

This active Low input signal is utilized to initiate Hardware Write Protection mode. This mode prevents the Block Protection bits and the WPEN bit in the Status Register from being modified. To activate the Hardware Write Protection, $\overline{WP}$ must be Low simultaneously when WPEN is set to 1.

Hold ($\overline{HOLD}$)

This feature is used to suspend the device in the middle of a serial sequence and temporarily ignore further communication on the bus (SI, SO, SCK). The $\overline{HOLD}$ signal transitions must occur only when SCK is Low and be held stable during SCK transitions. Connecting $\overline{HOLD}$ to High disables this feature. Figure. 5-8 shows Hold timing.

5. Device Operation

5.1 Status Register

The Status Register accessible by the user consists of 8-bits data for write protection control and write status. It becomes Read-Only under any of the following conditions: Hardware Write Protection is enabled or WEN is set to 0. If neither is true, it can be modified by a valid instruction.

Table 5.1: Status Register

Bit	Symbol	Name	Description
0	$\overline{RDY}$	Ready	When $\overline{RDY}$ = 0, device is ready for an instruction. When $\overline{RDY}$ = 1, device is busy. As busy, device only accepts Read Status Register command.
1	WEN	Write Enable	This represents the write protection status of the device. When WEN = 0, Status Register and entire array cannot be modified, regardless the setting of WPEN, $\overline{WP}$ pin or block protection. Write Enable command (WREN) can be used to set WEN to 1. Upon power-up stage, WEN is reset to 0.
2	BP0	Block Protect Bit	Despite of the status on WPEN, $\overline{WP}$ or WEN, BP0 and BP1 configure any combinations of the four blocks being protected (Table 5.2). They are non-volatile memory and programmed to 0 by factory.
3	BP1	Block Protect Bit	
4	X	Don't Care	Values can be either 0 or 1, but are not retained. Mostly always 0, except during write operation.
5	X	Don't Care	
6	X	Don't Care	
7	WPEN	Write Protect Enable	This bit can be utilized to enable Hardware Write Protection, together with $\overline{WP}$ pin. If enabled, Status Register becomes read-only. However, the memory array is not protected by this mode. Hardware Write Protection requires the setting of $\overline{WP}$ = 0 and WPEN = 1. Otherwise, it is disabled. WPEN cannot be altered from 1 to 0 if $\overline{WP}$ is already set to Low. (Table 5.4 for write protection)

Note: During internal write cycles, bits 0 to 7 are temporarily 1's.

Table 5.2: Block Protection by BP0 and BP1

Level	Status Register Bits		Array Addresses Protected
	BP1	BP0	
0	0	0	None
1 (1/4)	0	1	3000h-3FFFh
2 (1/2)	1	0	2000h-3FFFh
3 (All)	1	1	0000h-3FFFh

5.2 Op-Code Instructions

The operations of the GT25C128A are controlled by a set of instruction Op-Codes (Table 5.3) that are clocked-in serially via SI pin. To initiate an instruction, the chip select ($\overline{CS}$) must be Low. Subsequently, each Low-to-High transition of the clock (SCK) will latch a stable level from SI. After the 8-bit Op-Code, it may continue to latch-in an address and/or data from SI accordingly, or to output data from SO. During data output, data are latched out at the falling edge of SCK. All communications start with MSB first. Upon the transmission of the last bit but prior to any following Low-to-High transition on SCK, $\overline{CS}$ must be brought to High in order to end the transaction and start the operation. The device will enter into Standby Mode after the operation is completed.

Table 5.3: Instruction Op-Codes[1,2,3]

Name	Op-Code	Operation	Address	Data (SI)	Data (SO)
WREN	0000 X110	Set Write Enable Latch	-	-	-
WRDI	0000 X100	Reset Write Enable Latch	-	-	-
RDSR	0000 X101	Read Status Register	-	-	D_7-D_0 -
WRSR	0000 X001	Write Status Register	-	D_7-D_0	-
READ	0000 X011	Read Data from Array	A_{15}-A_0	-	D_7-D_0, ...
WRITE	0000 X010	Write Data to Array	A_{15}-A_0	D_7-D_0, ...	-
Read Identification Page	1000 X011[4]	Read the page dedicated to identification	A_{15}-A_0	D_7-D_0, ...	-
Write Identification Page	1000 X010[4]	Write the page dedicated to identification	A_{15}-A_0	D_7-D_0, ...	-
Read Lock Status	1000 X010[5]	Reads the lock status of the Identification Page.	A_{15}-A_0	D_7-D_0, ...	-
Lock ID	1000 X010[5]	Locks the Identification page in read-only mode.	A_{15}-A_0	D_7-D_0, ...	-

Notes: [1] X = Don't care bit. However, it is recommended to be "0".

[2] Some address bits may be don't care (Table 5.5).

[3] It is strongly recommended that an appropriate format of Op-Code must be entered. Otherwise, it may cause unexpected phenomenon to be occurred. Nevertheless, it is illegal to input invalid any Op-Code.

[4] Address bit A10 must be 0, all other address bits are Don't Care.

[5] Address bit A10 must be 1, all other address bits are Don't Care.

5.3 Write Enable

When V_{CC} is initially applied, the device powers up with both status register and entire array in a write-disabled state. Upon completion of Write Disable (WRDI), Write Status Register (WRSR) or Write Data to Array (WRITE), the device resets the WEN bit in the Status Register to 0. Prior to any data modification, a Write Enable (WREN) instruction is necessary to set WEN to 1 (Figure. 5-2).

5.4 Write Disable

The device can be completely protected from modification by resetting WEN to 0 through the Write Disable (WRDI) instruction (Figure. 5-3).

5.5 Read Status Register

The Read Status (RDSR) instruction reviews the status of Write Protect Enable, Block Protection setting (Table 5.2), Write Enable state and $\overline{RDY}$ status. RDSR is the only instruction accepted when a write cycle is underway. It is

recommended that the status of Write Enable and $\overline{RDY}$ be checked, especially prior to an attempted modification of data. These 8 bits information can be repeatedly output on SO after the initial Op-Code (Figure. 5-4).

5.6 Write Status Register

The Write Status Register (WRSR) instruction allows the user to choose a Block Protection setting and set or reset the WPEN bit. The values of the other data bits incorporated into WRSR can be 0 or 1 and are not stored in the Status Register. WRSR will be ignored unless both following conditions are true: a) WEN = 1, due to a prior WREN instruction; and b) Hardware Write Protection is not enabled (Table 5.4). Except for $\overline{RDY}$ status, the values in the Status Register remain unchanged until the moment when the write cycle is completed and the register is updated. Note that WPEN can be changed from 1 to 0 only if $\overline{WP}$ is already set High. Once completed, WEN is reset for complete chip write protection (Fig. 5-5).

5.7 Read Data

This instruction includes an Op-Code and 16-bit address, then results the selected data to be shifted out from SO. Following the first data byte, additional sequential data can be output. If the data byte of the last address is initially output, then address will rollover to the first address in the array, and the output could loop indefinitely. At any time, a rising $\overline{CS}$ signal ceases the operation (Figure. 5-6).

5.8 Write Data

The WRITE instruction contains an Op-Code, a 16-bit address and the first data byte. Additional data bytes may be supplied sequentially after the first byte. Each WRITE instruction can affect up to 64 bytes of data in a page. Each page has a starting address XXXXXXXX XX000000 and an ending address XXXXXXXX XX111111. After the last byte of data in a page is input, the address rolls over to the beginning of the same page. If more than 64 bytes of data is input during a single instruction, then only the last 64 bytes will be retained, but the initial data will be overwritten.

The contents of the array defined by Block Protection cannot be modified as long as that block configuration is selected. The contents of the array outside the Block Protection can only be modified if Write Enable (WEN) is set to 1. Therefore, it may be necessary that a WREN instruction is initiated prior to WRITE. Once Write operation is completed, WEN is reset for complete chip write protection (Figure. 5-7). Besides, Hardware Write Protection has no affect on the memory array.

5.9 Read Identification Page

The Identification Page (64 bytes) is an additional page which can be written and (later) permanently locked in Read-only mode. Reading this page is achieved with the Read Identification Page instruction (see Table 5.3).

The Chip Select signal ($\overline{CS}$) is first driven low, the bits of the instruction byte and address bytes are then shifted in, on Serial Data input (SI). Address bit A10 must be 0, address bits [A15:A11] and [A9:A6] are Don't Care, and the data byte pointed to by [A5:A0] is shifted out on Serial Data output (SO). If Chip Select ($\overline{CS}$) continues to be driven low, the internal address register is automatically incremented, and the byte of data at the new address is shifted out.

The number of bytes to read in the ID page must not exceed the page boundary (e.g. when reading the ID page from location 24d, the number of bytes should be less than or equal to 40d, as the ID page boundary is 64 bytes). The read cycle is terminated by driving Chip Select ($\overline{CS}$) high. The rising edge of the Chip Select ($\overline{CS}$) signal can occur at any time during the cycle. The first byte addressed can be any byte within any page (Figure. 5-8).

The instruction is not accepted, and is not executed, if a write cycle is currently in progress.

5.10 Write Identification Page

The Identification Page (64 bytes) is an additional page which can be written and (later) permanently locked in Read-only mode. Writing this page is achieved with the Write Identification Page instruction (see Table 5.3), the Chip Select signal ($\overline{CS}$) is first driven low. The bits of the instruction byte, address byte, and at least one data byte are then shifted in on Serial Data input (SI). Address bit A10 must be 0, address bits [A15:A11] and [A9:A6] are Don't Care, the [A5:A0] address bits define the byte address inside the identification page. The instruction sequence is shown in Figure 5-9.

5.11 Read Lock Status

The Read Lock Status instruction (see Table 5.3) allows to check if the Identification Page is locked (or not) in read-only mode. The Read Lock Status sequence is defined with the Chip Select ($\overline{CS}$) first driven low. The bits of the instruction byte and address bytes are then shifted in on Serial Data input (SI). Address bit A10 must be 1, all other address bits are Don't Care. The Lock bit is the LSB (least significant bit) of the byte read on Serial Data output (SO). It is at '1' when the lock is active and at '0' when the lock is not active. If Chip Select ($\overline{CS}$) continues to be driven low, the same data byte is shifted out. The read cycle is terminated by driving Chip Select ($\overline{CS}$) high (Figure 5-10).

5.12 Lock ID

The Lock ID instruction permanently locks the Identification Page in read-only mode. Before this instruction can be accepted, a Write Enable (WREN) instruction must have been executed. The Lock ID instruction is issued by driving Chip Select ($\overline{CS}$) low, sending the instruction code, the address and a data byte on Serial Data input (SI), and driving Chip Select ($\overline{CS}$) high. In the address sent, A10 must be equal to 1, all other address bits are Don't Care. The data byte sent must be equal to the binary value xxxx xx1x, where x = Don't Care.

Chip Select ($\overline{CS}$) must be driven high after the rising edge of Serial Clock (SCK) that latches in the eighth bit of the data byte, and before the next rising edge of Serial Clock (SCK). Otherwise, the Lock ID instruction is not executed. Driving Chip Select ($\overline{CS}$) high at a byte boundary of the input data triggers the self-timed write cycle whose duration is T_{WR}. The instruction sequence is shown in Figure 5-11.

The instruction is not accepted, and so not executed, under the following conditions:

- If the Write Enable Latch (WEL) bit has not been set to 1 (by previously executing a Write Enable instruction).
- If Status register bits (BP1,BP0) = (1,1).
- If a write cycle is already in progress.
- If the device has not been deselected, by Chip Select ($\overline{CS}$) being driven high, at a byte boundary (after the eighth bit, b0, of the last data byte that was latched in).
- If the Identification page is locked by the Lock Status bit.

Table 5.4: Write Protection

WPEN	$\overline{WP}$	Hardware Write Protection	WEN	Inside Block	Outside Block	Status Register (WPEN, BP1, BP0)
0	X	Not Enabled	0	Read-only	Read-only	Read-only
0	X	Not Enabled	1	Read-only	Unprotected	Unprotected
1	0	Enabled	0	Read-only	Read-only	Read-only
1	0	Enabled	1	Read-only	Unprotected	Read-only
X	1	Not Enabled	0	Read-only	Read-only	Read-only
X	1	Not Enabled	1	Read-only	Unprotected	Unprotected

Note: X = Don't care bit.

Table 5.5: Address Key

Name	GT25C128A
A_N	A_{13}-A_0
Don't Care Bits	A_{15}-A_{14}

5.13. Diagrams

Figure 5-1. Synchronous Data Timing

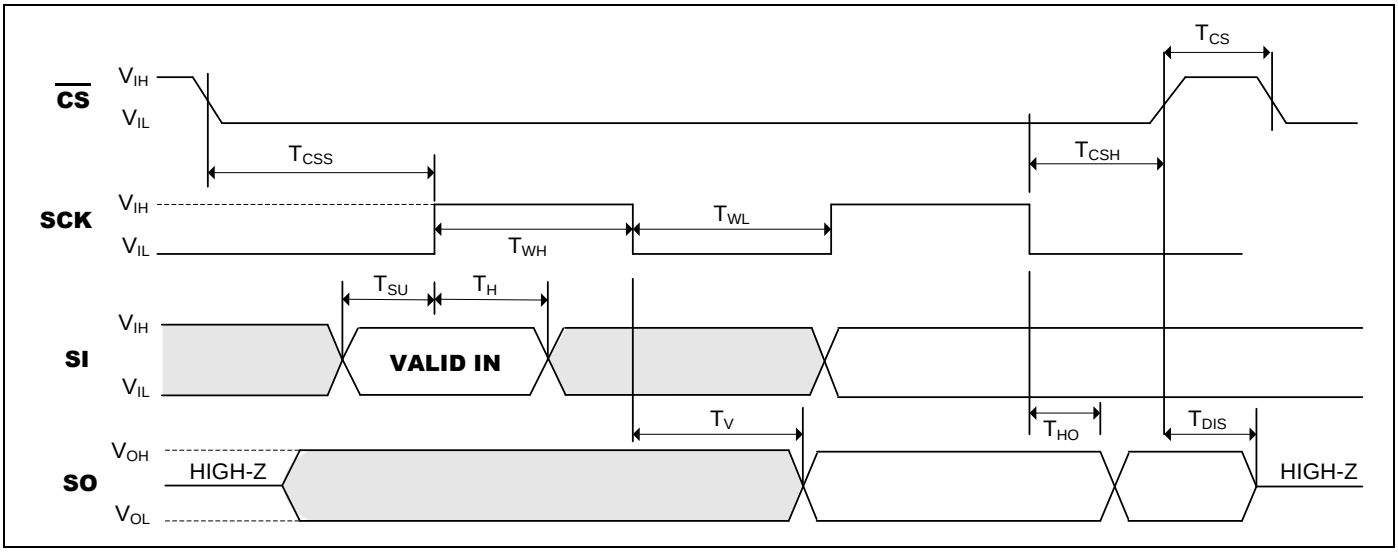


Figure 5-2. WREN Timing

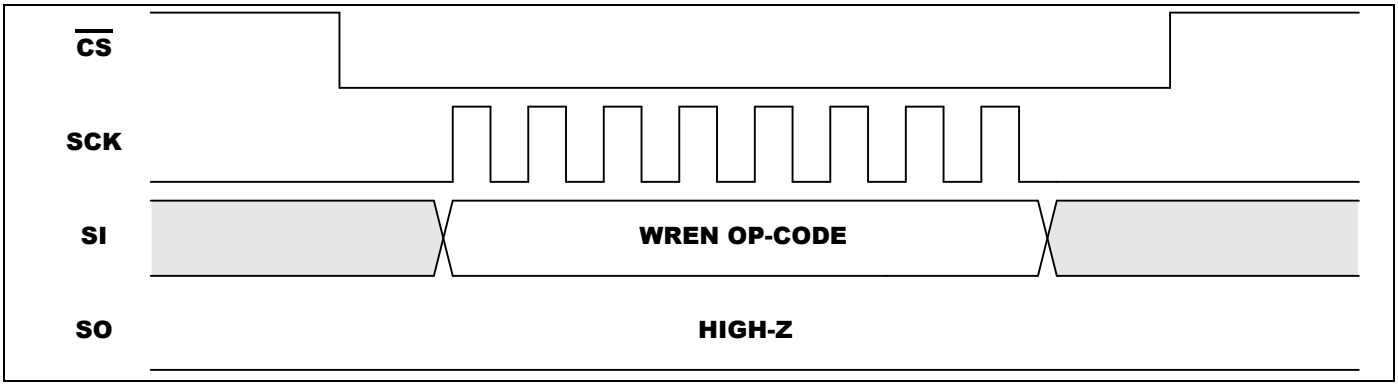


Figure 5-3. WRDI Timing

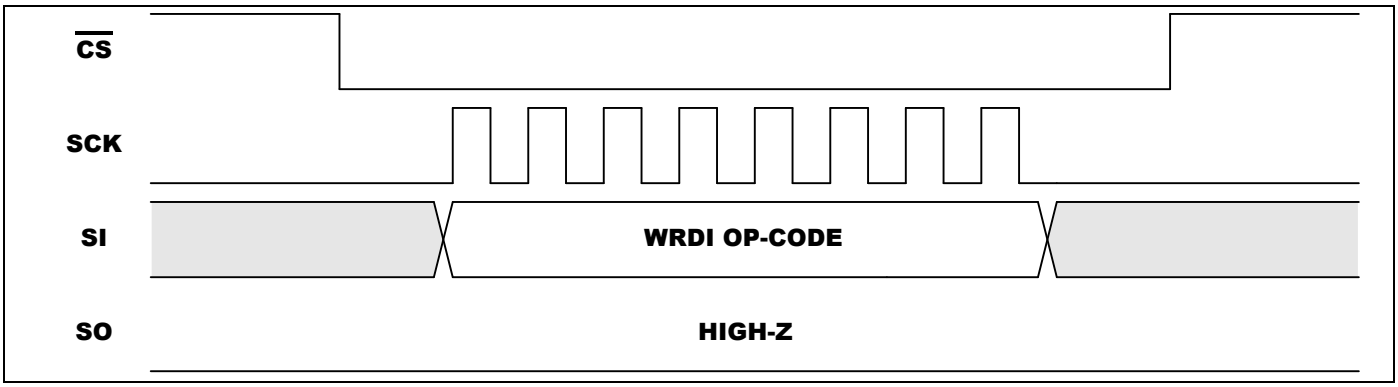


Figure 5-4. RDSR Timing

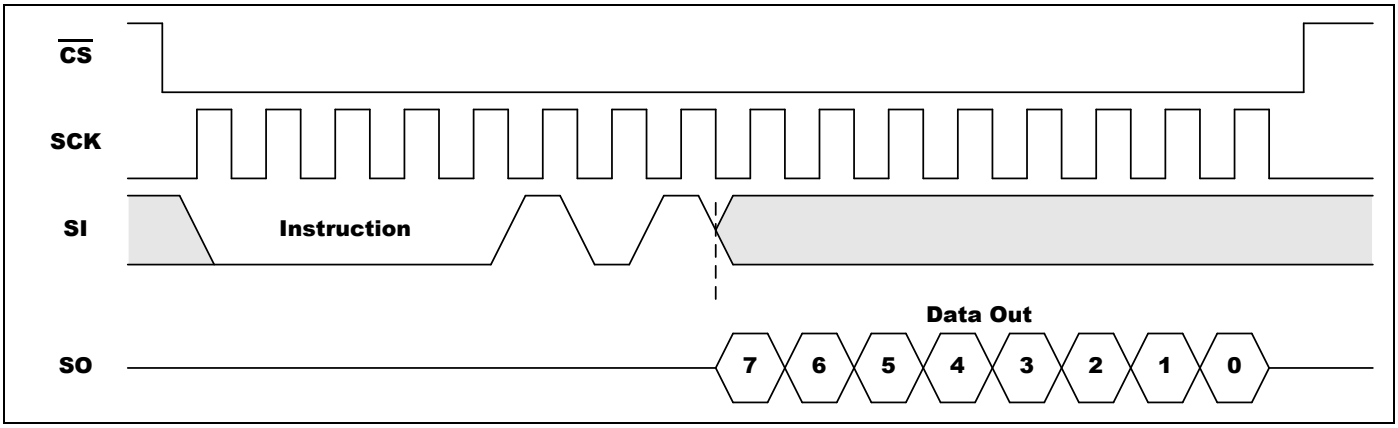


Figure 5-5. WRSR Timing

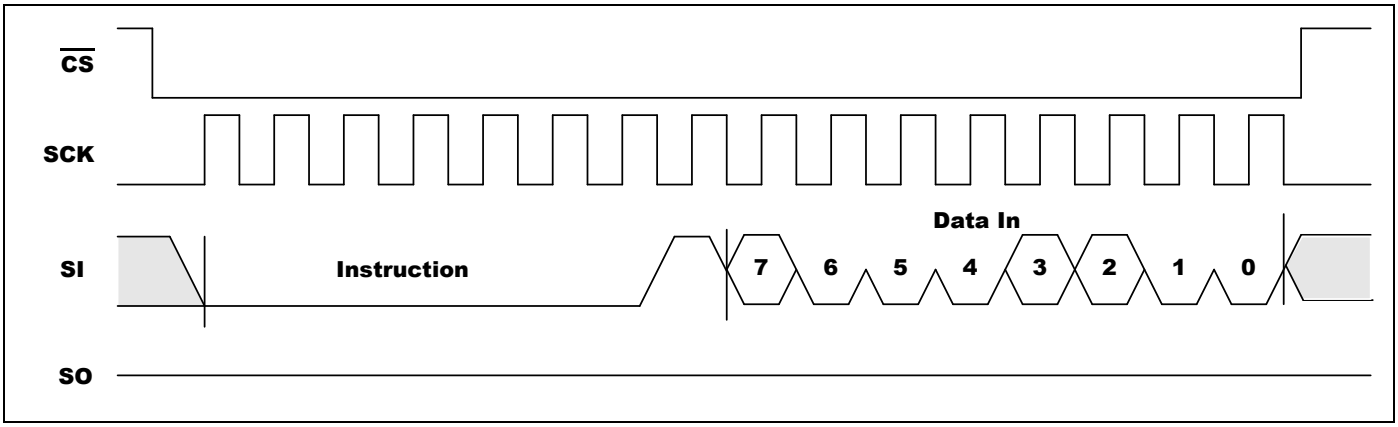


Figure 5-6. READ Timing

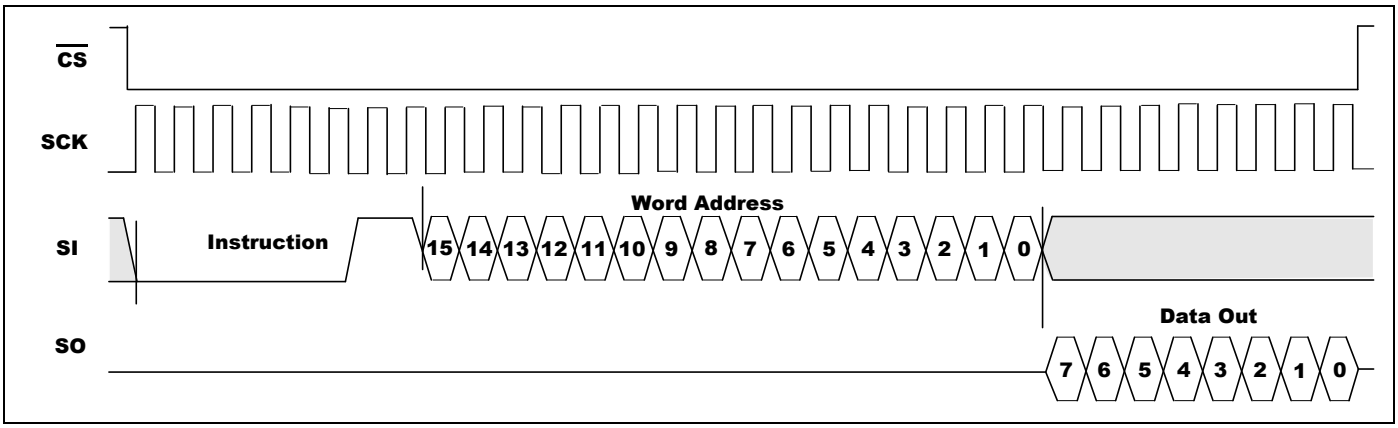


Figure 5-7. WRITE Timing

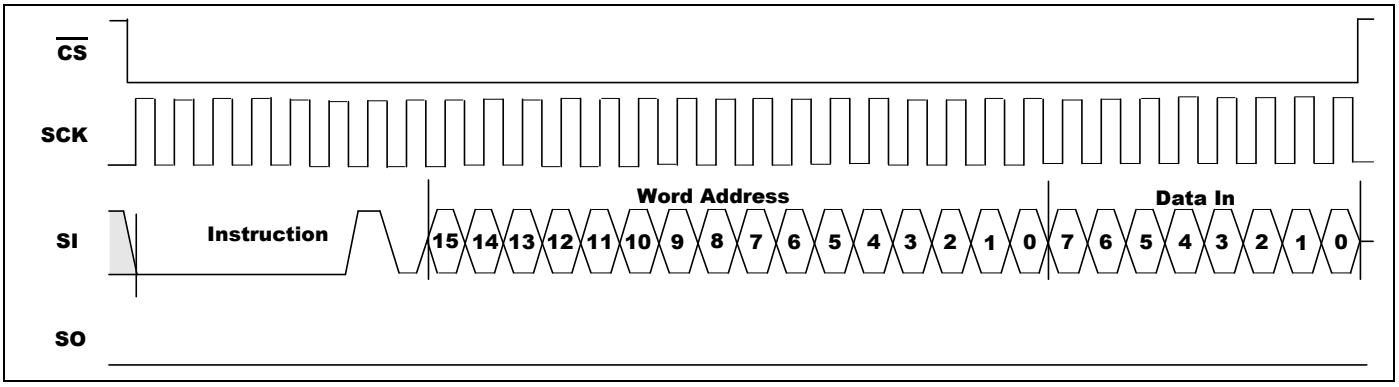


Figure 5-8. Read Identification Page

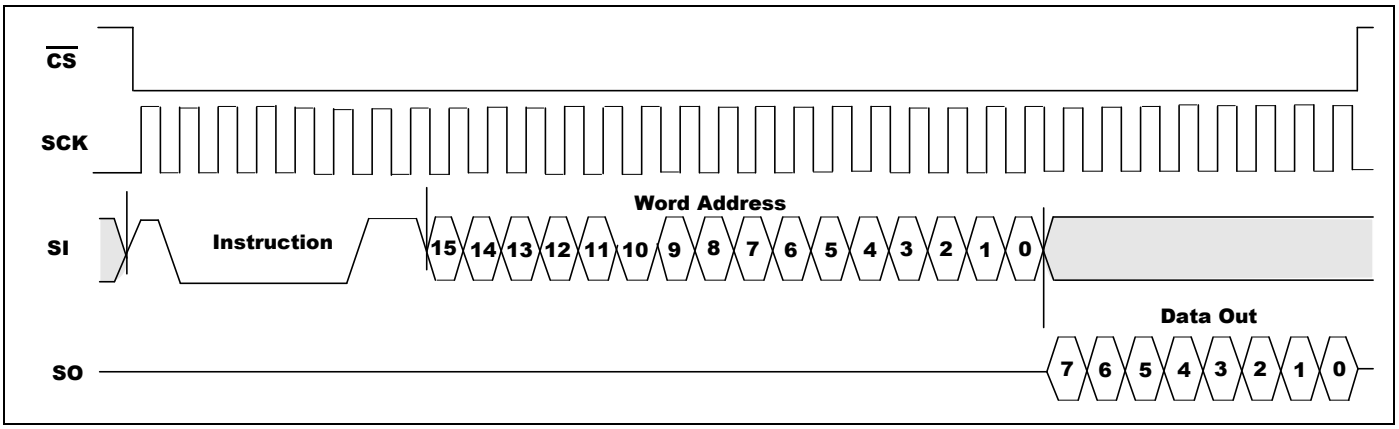


Figure 5-9. Write Identification Page

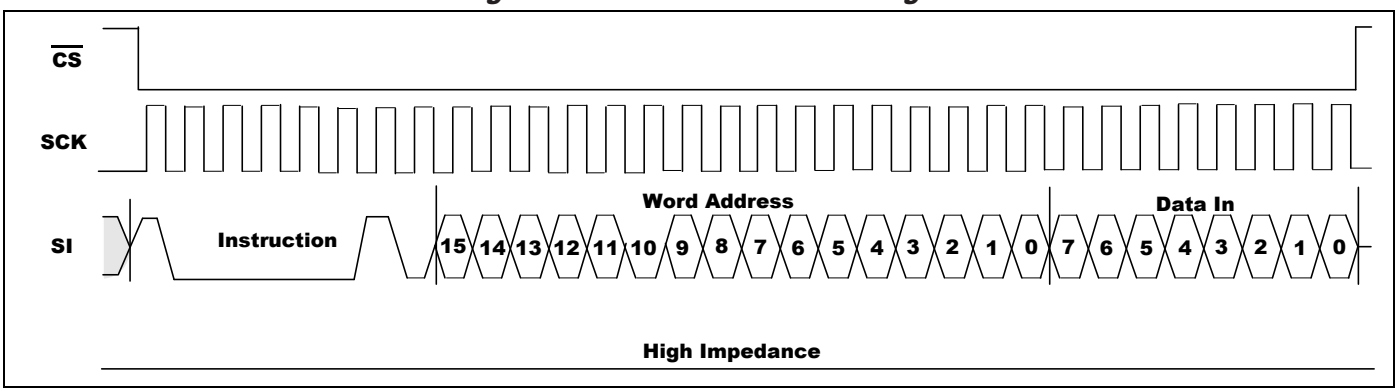


Figure 5-10. Read Lock Status

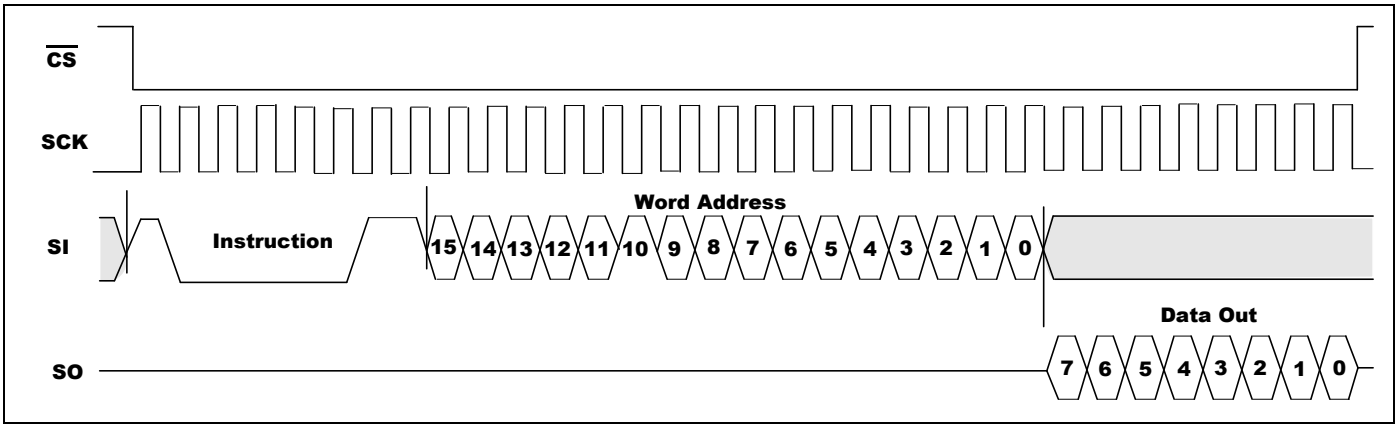


Figure 5-11. Lock ID

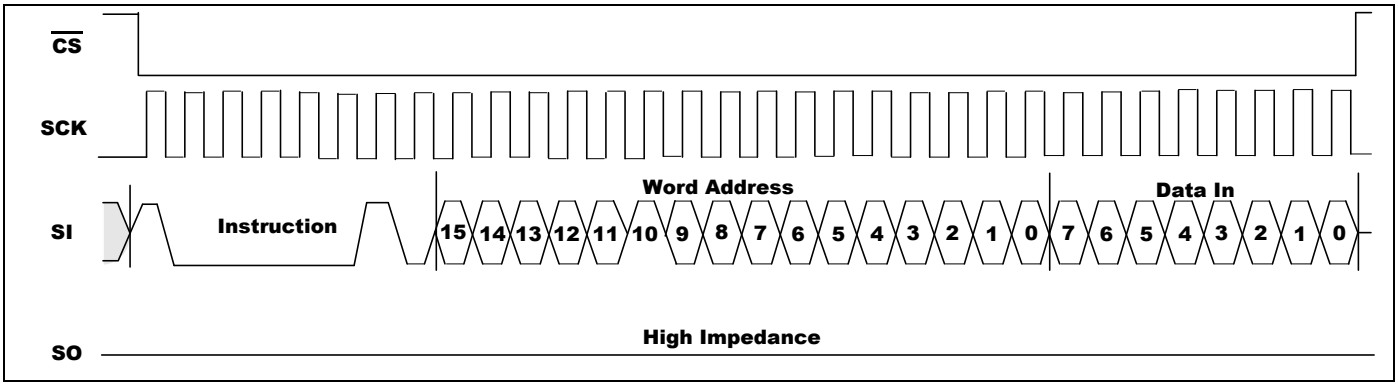
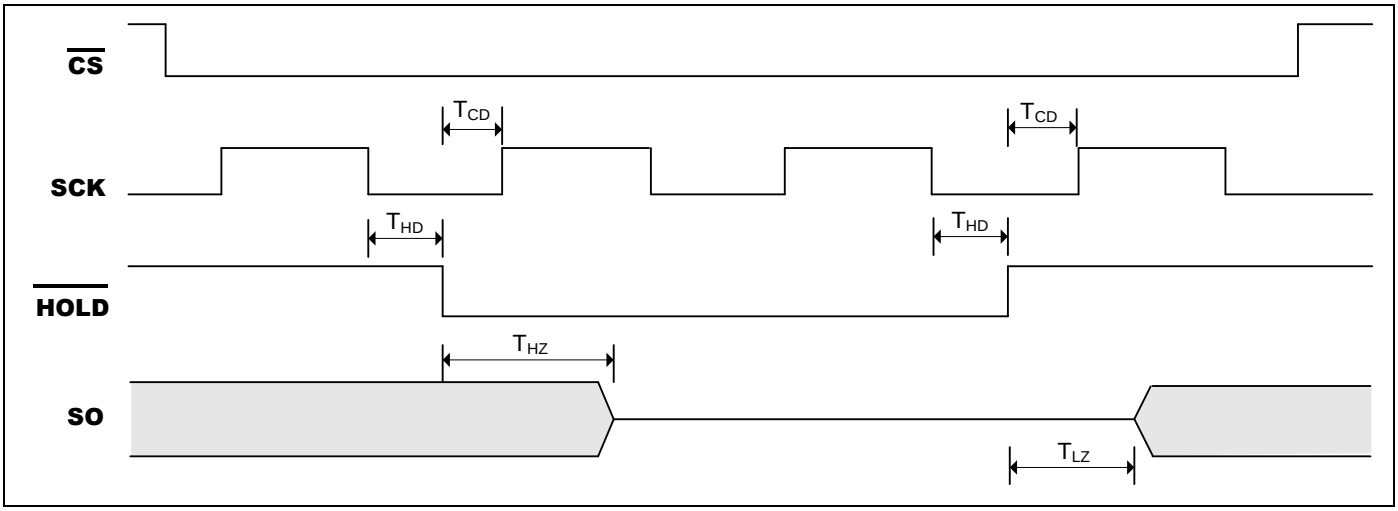


Figure 5-12. HOLD Timing



6. Electrical Characteristics

6.1 Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
V_S	Supply Voltage	-0.5 to + 6.5	V
V_P	Voltage on Any Pin	-0.5 to + 6.5	V
T_{BIAS}	Temperature Under Bias	–55 to +125	°C
T_{STG}	Storage Temperature	–65 to +150	°C
I_{OUT}	Output Current	5	mA

Note: Stress greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

6.2 Operating Range

Range	Ambient Temperature (T_A)	V_{CC}
Industrial	–40°C to +85°C	1.7V to 5.5V

Note: Giantec offers Industrial grade for Commercial applications (0°C to +70°C).

6.3 Capacitance

Symbol	Parameter[1, 2]	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	pF
$C_{I/O}$	Input / Output Capacitance	$V_{I/O}$ = 0V	8	pF

Notes: [1] Tested initially and after any design or process changes that may affect these parameters and not 100% tested.

[2] Test conditions: T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V

6.4 DC Electrical Characteristic

Industrial: T_A = –40°C to +85°C, V_{CC} = 1.7V ~ 5.5V

Symbol	Parameter	Vcc	Test Conditions	Min.	Max.	Unit
V_{CC}	Supply Voltage			1.7	5.5	V
V_{IH}	Input High Voltage			0.7* V_{CC}	V_{CC}+1	V
V_{IL}	Input Low Voltage			-0.3	0.3* V_{CC}	V
I_{LI}	Input Leakage Current		V_{IN} = 0V To V_{CC}	-2	2	µA
I_{LO}	Output Leakage Current		V_{OUT} = 0V To V_{CC}, $\overline{CS}$ = V_{CC}	-2	2	µA
V_{OH}	Output High Voltage	1.7	I_{OH} = -0.1mA	0.8*V_{CC}	—	V
		2.5	I_{OH} = -0.4mA	0.8*V_{CC}	—	V
		5	I_{OH} = -2 mA	0.8*V_{CC}	—	V
V_{OL}	Output Low Voltage	1.7	I_{OL} = 0.15 mA	—	0.2	V
		2.5	I_{OL} = 1.5 mA	—	0.4	V
		5	I_{OL} = 2 mA	—	0.4	V
I_{CC1}	Write Operating Current	1.7	Write at 5 MHz, SO=Open	—	2	mA
		2.5	Write at 10 MHz, SO=Open	—	2	mA
		5	Write at 20 MHz, SO=Open	—	3	mA
I_{CC2}	Read Operating Current	1.7	Read at 5 MHz, SO=Open	—	1	mA
		2.5	Read at 10 MHz, SO=Open	—	3	mA
		5	Read at 20 MHz, SO=Open	—	5	mA
I_{SB}	Standby Current	1.7	V_{IN}= V_{CC} or GND, $\overline{CS}$ = V_{CC}	—	1	µA
		2.5	V_{IN}= V_{CC} or GND, $\overline{CS}$ = V_{CC}	—	1	µA
		5	V_{IN}= V_{CC} or GND, $\overline{CS}$ = V_{CC}	—	2	µA

6.5 AC Electrical Characteristic

Industrial: T_A = –40°C to +85°C, Supply voltage = 1.7V to 5.5V

Symbol	Parameter[1]	1.7V≤Vcc<2.5V		2.5V≤Vcc<4.5V		4.5V≤Vcc≤5.5V		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
F_{SCK}	SCK Clock Frequency	0	5	0	10	0	20	MHz
T_{RI}	Input Rise Time	—	1	—	1	—	1	μs
T_{FI}	Input Fall Time	—	1	—	1	—	1	μs
T_{WH}	SCK High Time	80	—	40	—	20	—	ns
T_{WL}	SCK Low Time	80	—	40	—	20	—	ns
T_{CS}	$\overline{CS}$ High Time	100	—	50	—	25	—	ns
T_{CSS}	$\overline{CS}$ Setup Time	100	—	50	—	25	—	ns
T_{CSH}	$\overline{CS}$ Hold Time	100	—	50	—	25	—	ns
T_{SU}	Data In Setup Time	20	—	10	—	5	—	ns
T_H	Data In Hold Time	20	—	10	—	5	—	ns
T_{HD}	$\overline{HOLD}$ Setup Time	20	—	10	—	5	—	ns
T_{CD}	$\overline{HOLD}$ Hold Time	20	—	10	—	5	—	ns
T_V[2]	Output Valid	0	80	0	40	0	20	ns
T_{HO}	Output Hold Time	0	—	0	—	0	—	ns
T_{LZ}	$\overline{HOLD}$ to Output Low Z	0	80	0	40	0	25	ns
T_{HZ}	$\overline{HOLD}$ to Output High Z	—	80	—	40	—	40	ns
T_{DIS}	Output Disable Time	—	80	—	40	—	40	ns
T_{WC}	Write Cycle Time	—	5	—	5	—	5	ms

Notes: [1] The parameters are characterized but not 100% tested.

[2] C_L = 30pF (typical)

7. Ordering Information

Industrial Grade: -40°C to +85°C, Lead-free

Voltage Range	Part Number*	Package (8-pin)*
1.7V to 5.5V	GT25C128A-2GLI-TR	150-mil SOIC
	GT25C128A-2ZLI-TR	3 x 4.4 mm TSSOP
	GT25C128A-2UDLI-TR	2 x 3 x 0.55 mm UDFN

*

1. Contact Giantec Sales Representatives for availability and other package information.
2. The product is packed in tape and reel “-TR” (4K per reel), except UDFN is 5K per reel.
3. Refer to Giantec website for related declaration document on lead free, RoHS, halogen free or Green, whichever is applicable.
4. Giantec offers Industrial grade for Commercial applications (0°C to +70°C).

8. Top Markings

8.1 SOIC Package

G: Giantec Logo

5128A2GLI: GT25C128A-2GLI-TR

YWW: Date Code, Y=year, WW=week

8.2 TSSOP Package

GT: Giantec Logo

5128A2ZLI: GT25C128A-2ZLI-TR

YWW: Date Code, Y=year, WW=week

8.3 UDFN Package

GT*:* Giantec Logo

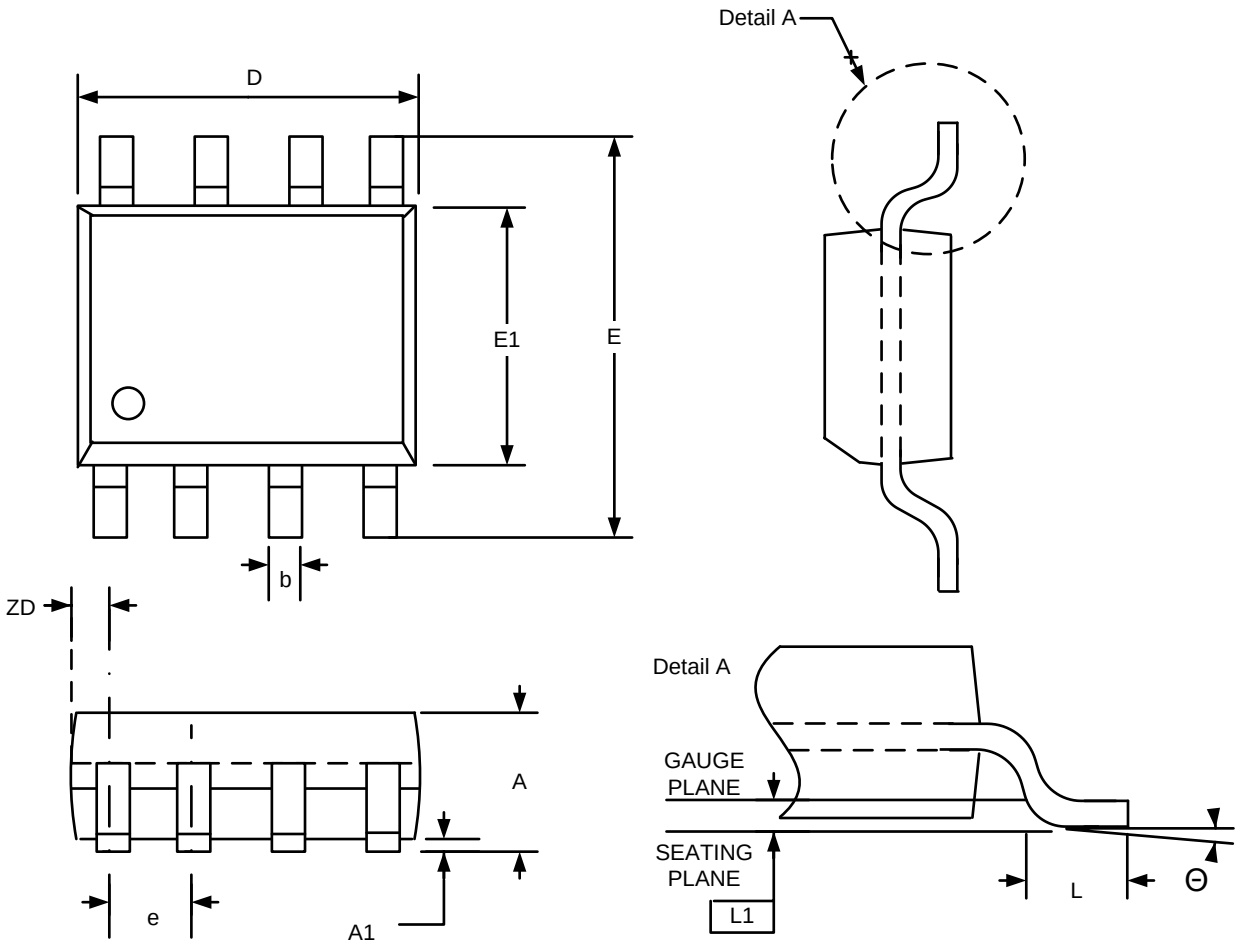
57A: GT25C128A-2UDLI-TR

YWW: Date Code, Y=year, WW=week

9. Package Information

9.1 SOIC

8L 150mil SOIC Package Outline

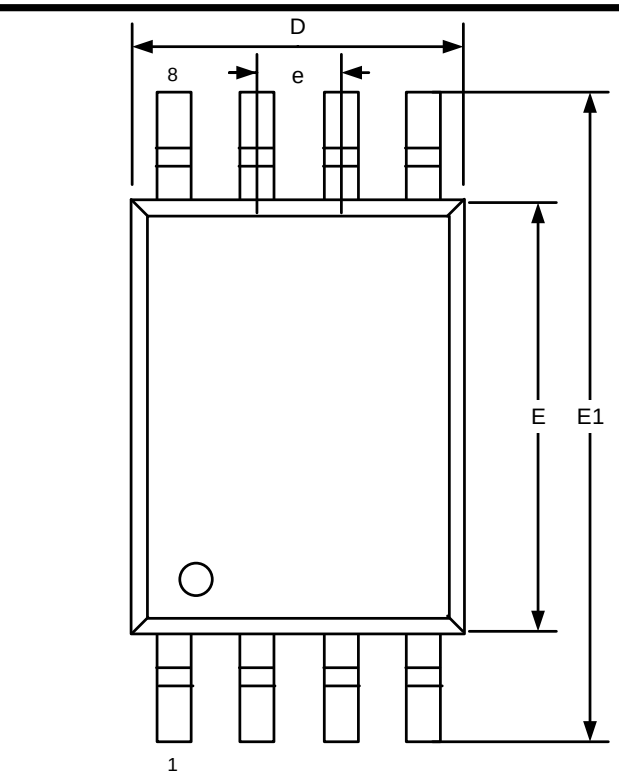


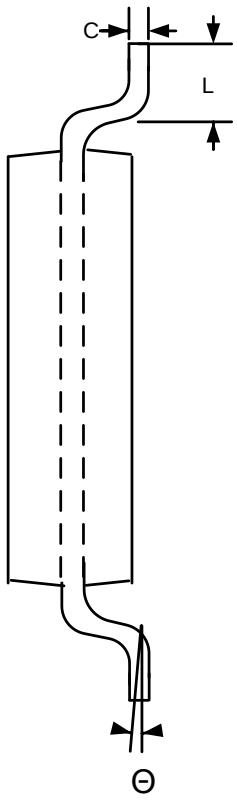
SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.35	--	1.75	0.053	--	0.069
A1	0.10	--	0.25	0.004	--	0.010
b	0.33	--	0.51	0.013	--	0.020
D	4.80	--	5.00	0.189	--	0.197
E	5.80	--	6.20	0.228	--	0.244
E1	3.80	--	4.00	0.150	--	0.157
e	1.27 BSC.			0.050 BSC.		
L	0.38	--	1.27	0.015		0.050
L1	0.25 BSC.			0.010 BSC.		
ZD	0.545 REF.			0.021 REF.		
Θ	0	--	8°	0	--	8°

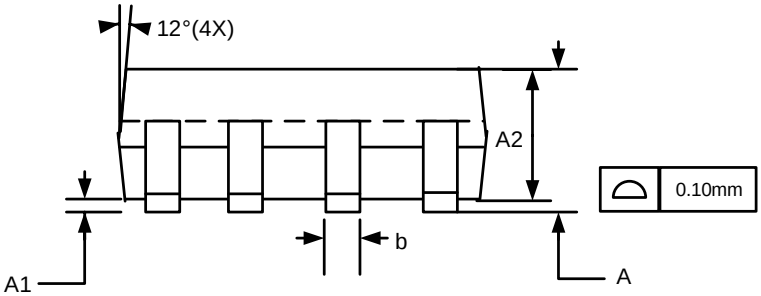
Note:
1. Controlling Dimension:MM
2. Dimension D and E1 do not include Mold protrusion
3. Dimension b does not include dambar protrusion/intrusion.
4. Refer to Jedec standard MS-012
5. Drawing is not to scale

9.2 TSSOP

8L 3x4.4mm TSSOP Package Outline





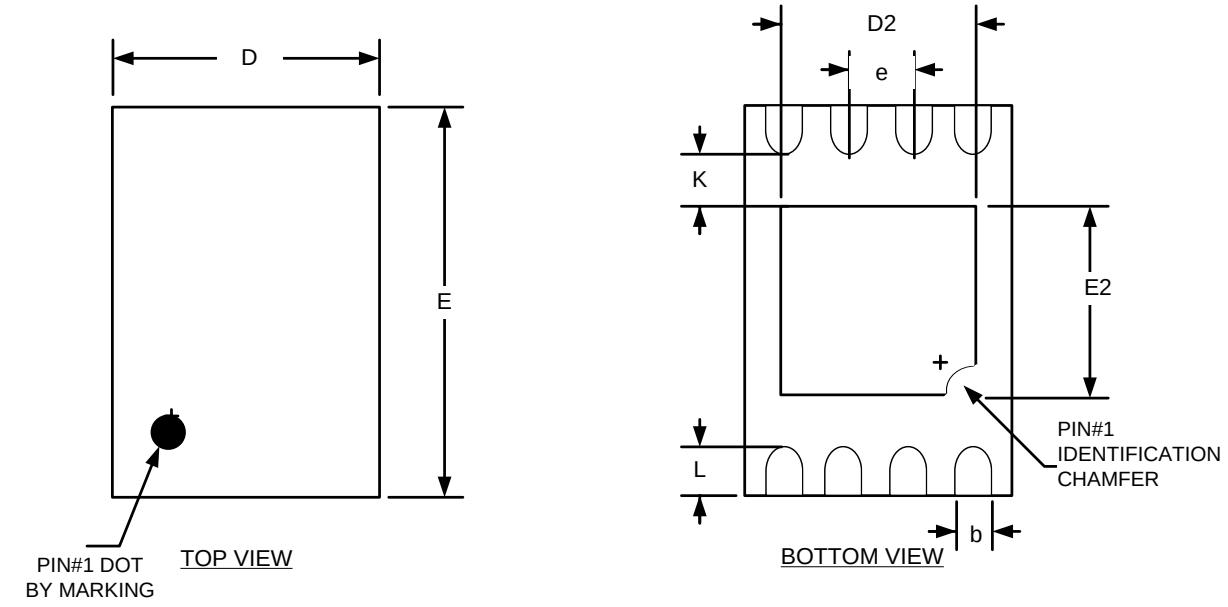


Note:
1. Controlling Dimension:MM
2. Dimension D and E do not include Mold protrusion
3. Dimension b does not include dambar protrusion/intrusion
4. Refer to Jedec standard MO-153 AA
5. Drawing is not to scale
6. Package may have exposed tie bar.

SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	--	--	1.20	--	--	0.047
A1	0.05	--	0.15	0.002	--	0.006
A2	0.80	1.00	1.05	0.031	0.039	0.041
b	0.19	--	0.30	0.007	--	0.012
c	0.09	--	0.20	0.004	--	0.008
D	2.90	3.00	3.10	0.114	0.118	0.122
E	4.30	4.40	4.50	0.169	0.173	0.177
E1	6.20	6.40	6.60	0.244	0.252	0.230
e	0.65 BSC			0.026 BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
Θ	0	--	8°	0	--	8°

9.3 UDFN

8L 2x3mm UDFN Package Outline



SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.50	0.55	0.60	0.020	0.022	0.024
A1	0.00	--	0.05	0.000	--	0.002
b	0.18	0.25	0.30	0.007	0.010	0.012
A2	0.152 REF			0.006 REF		
D	2.00 BSC			0.079 BSC		
D2	1.25	1.40	1.50	0.049	0.055	0.059
E	3.00 BSC			0.118 BSC		
E2	1.15	1.30	1.40	0.045	0.051	0.055
e	0.50 BSC.			0.020 BSC.		
K	0.40	--	--	0.016	--	--
L	0.20	0.30	0.40	0.008	0.012	0.016

Note:

1. Controlling Dimension:MM
2. Drawing is not to scale

10. Revision History

Revision	Date	Descriptions
A0	Sep. 2011	Initial version
C1	Oct. 2013	Revise SOIC/SOP to SOIC
C2	Jul. 2019	Update TSSOP POD and VP