# TVS Diodes

Transient Voltage Suppressor Diodes

# ESD3V3U4ULC

Ultra-low Capacitance ESD / Transient Protection Array

ESD3V3U4ULC

## Data Sheet

Rev. 1.2, 2012-07-03
Final

Power Management & Multimarket

**Edition 2012-07-03**

**Published by**
**Infineon Technologies AG**
**81726 Munich, Germany**



### Legal Disclaimer

The information given in this document shall in no event be regarded as a guarantee of conditions or characteristics. With respect to any examples or hints given herein, any typical values stated herein and/or any information regarding the application of the device, Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind, including without limitation, warranties of non-infringement of intellectual property rights of any third party.

### Information

For further information on technology, delivery terms and conditions and prices, please contact the nearest Infineon Technologies Office (**www.infineon.com**).

### Warnings

Due to technical requirements, components may contain dangerous substances. For information on the types in question, please contact the nearest Infineon Technologies Office.

Infineon Technologies components may be used in life-support devices or systems only with the express written approval of Infineon Technologies, if a failure of such components can reasonably be expected to cause the failure of that life-support device or system or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.

| Revision History Revision 1.1, 2012-04-18 | |
|---|---|
| **Page or Item** | **Subjects (major changes since previous revision)** |
| **Rev. 1.2, 2012-07-03** | |
| 7 | **Figure 1** |
| | |
| | |
| | |
| | |

### Trademarks of Infineon Technologies AG

AURIX™, BlueMoon™, COMNEON™, C166™, CROSSAVE™, CanPAK™, CIPOS™, CoolMOS™, CoolSET™, CORECONTROL™, DAVE™, EasyPIM™, EconoBRIDGE™, EconoDUAL™, EconoPACK™, EconoPIM™, EiceDRIVER™, EUPEC™, FCOS™, HITFET™, HybridPACK™, ISOFACE™, I²RF™, IsoPACK™, MIPAQ™, ModSTACK™, my-d™, NovalithIC™, OmniTune™, OptiMOS™, ORIGA™, PROFET™, PRO-SIL™, PRIMARION™, PrimePACK™, RASIC™, ReverSave™, SatRIC™, SIEGET™, SINDRION™, SMARTi™, SmartLEWIS™, TEMPFET™, thinQ!™, TriCore™, TRENCHSTOP™, X-GOLD™, XMM™, X-PMU™, XPOSYS™.

### Other Trademarks

Advance Design System™ (ADS) of Agilent Technologies, AMBA™, ARM™, MULTI-ICE™, PRIMECELL™, REALVIEW™, THUMB™ of ARM Limited, UK. AUTOSAR™ is licensed by AUTOSAR development partnership. Bluetooth™ of Bluetooth SIG Inc. CAT-iq™ of DECT Forum. COLOSSUS™, FirstGPS™ of Trimble Navigation Ltd. EMV™ of EMVCo, LLC (Visa Holdings Inc.). EPCOS™ of Epcos AG. FLEXGO™ of Microsoft Corporation. FlexRay™ is licensed by FlexRay Consortium. HYPERTERMINAL™ of Hilgraeve Incorporated. IEC™ of Commission Electrotechnique Internationale. IrDA™ of Infrared Data Association Corporation. ISO™ of INTERNATIONAL ORGANIZATION FOR STANDARDIZATION. MATLAB™ of MathWorks, Inc. MAXIM™ of Maxim Integrated Products, Inc. MICROTEC™, NUCLEUS™ of Mentor Graphics Corporation. Mifare™ of NXP. MIPI™ of MIPI Alliance, Inc. MIPS™ of MIPS Technologies, Inc., USA. muRata™ of MURATA MANUFACTURING CO., MICROWAVE OFFICE™ (MWO) of Applied Wave Research Inc., OmniVision™ of OmniVision Technologies, Inc. Openwave™ Openwave Systems Inc. RED HAT™ Red Hat, Inc. RFMD™ RF Micro Devices, Inc. SIRIUS™ of Sirius Sattelite Radio Inc. SOLARIS™ of Sun Microsystems, Inc. SPANSION™ of Spansion LLC Ltd. Symbian™ of Symbian Software Limited. TAIYO YUDEN™ of Taiyo Yuden Co. TEAKLITE™ of CEVA, Inc. TEKTRONIX™ of Tektronix Inc. TOKO™ of TOKO KABUSHIKI KAISHA TA. UNIX™ of X/Open Company Limited. VERILOG™, PALLADIUM™ of Cadence Design Systems, Inc. VLYNQ™ of Texas Instruments Incorporated. VXWORKS™, WIND RIVER™ of WIND RIVER SYSTEMS, INC. ZETEX™ of Diodes Zetex Limited.

Last Trademarks Update 2010-06-09

# 1 Ultra-low Capacitance ESD / Transient Protection Array

## 1.1 Features

- ESD / transient protection of high speed data lines exceeding :
  - IEC61000-4-2 (ESD) : ±20 kV (air/contact)
  - IEC61000-4-4 (EFT) : 2.5 kV (5/50ns)
  - IEC61000-4-5 (Surge) : 3 A (8/20µs)
- Maximum working voltage: $V_{RWM}$ = 3.3 V
- Ultra low capacitance $C_L$ = 0.4 pF I/O to GND (typical)
- Very low clamping voltage: $V_{CL}$ = 8 V at $I_{PP}$ = 16 A (typical)
- Very low dynamic resistance: $R_{DYN}$ = 0.19 Ω (typical)
- TSLP-9-1 package with pad pitch 0.5 mm, optimized pad design to simplify PCB layout
- Pb-free and halogen free package (RoHS compliant)

## 1.2 Application Examples

- USB 3.0, 10/100/1000 Ethernet, Firewire
- DVI, HDMI, S-ATA, DisplayPort
- Mobile HDMI Link, MDDI, MIPI, etc.

# 2 Product Description

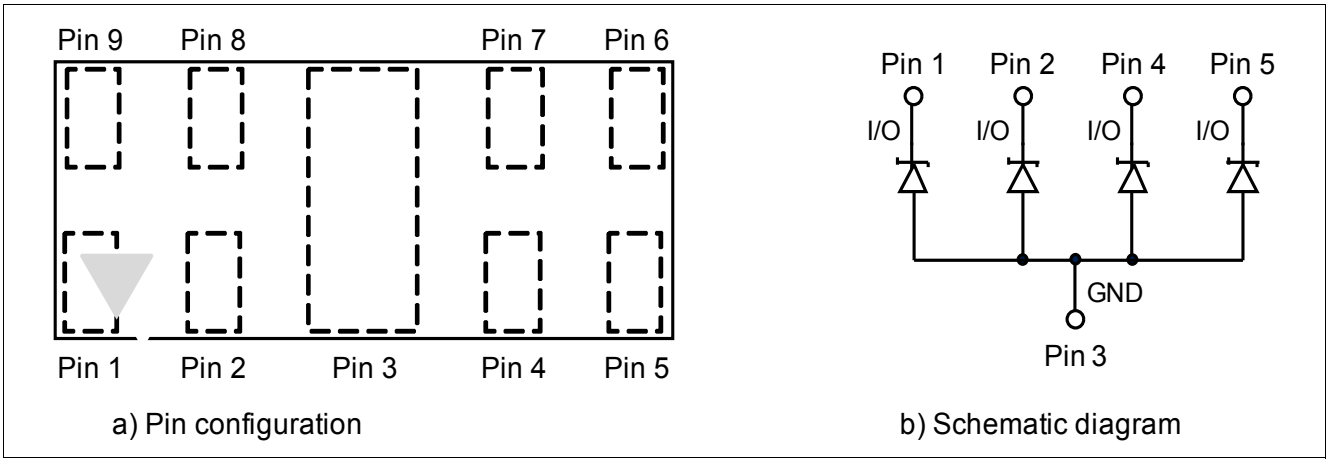


**Figure 1 Pin Configuration and Schematic Diagram**

**Table 1 Ordering Information**

| Type | Package | Configuration | Marking code |
|---|---|---|---|
| ESD3V3U4ULC | TSLP-9-1 | 4 lines, uni-directional | Z2 |

# 3 Characteristics

**Table 2 Maximum Rating** at $T_A$ = 25 °C, unless otherwise specified

| Parameter | Symbol | Values | | | Unit |
|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | |
| ESD contact discharge[1)] | $V_{ESD}$ | – | – | 20 | kV |
| Peak pulse current ($t_p$ = 8/20 µs)[2)] | $I_{PP}$ | – | – | 3 | A |
| Operating temperature | $T_{OP}$ | -40 | – | 125 | °C |
| Storage temperature | $T_{stg}$ | -65 | – | 150 | °C |

1) $V_{ESD}$ according to IEC61000-4-2
2) $I_{PP}$ according to IEC61000-4-5

## 3.1 Electrical Characteristics at $T_A$ = 25 °C, unless otherwise specified

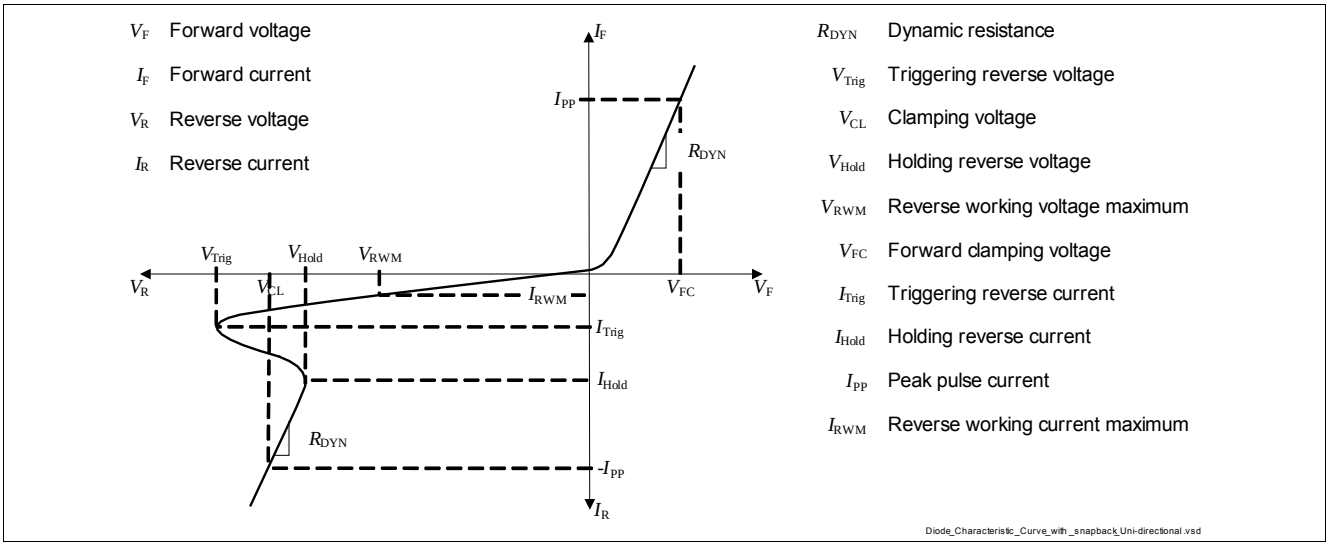


**Figure 2 Definitions of electrical characteristics[1]**

**Table 3 DC Characteristics** at $T_A$ = 25 °C, unless otherwise specified

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Reverse working voltage | $V_{RWM}$ | – | – | 3.3 | V | I/O to *GND* |
| Reverse current | $I_R$ | – | 1 | 50 | nA | $V_R$ = 3.3 V, I/O to *GND* |

**Table 4 RF Characteristics** at $T_A$ = 25 °C, unless otherwise specified

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Line capacitance[1] | $C_L$ | – | 0.4 | 0.65 | pF | $V_R$ = 0 V, $f$ = 1 MHz, I/O to $GND$ |
| | | – | 0.2 | 0.35 | pF | $V_R$ = 0 V, $f$ = 1 MHz, I/O to I/O |
| Channel capacitance matching between I/O to GND | $\Delta C_{i/o\text{-}GND}$ | – | 0.035 | – | pF | $V_R$ = 0 V, $f$ = 1 MHz, I/O to GND |
| Channel capacitance matching between I/O to I/O | $\Delta C_{i/o\text{-}i/o}$ | – | 0.017 | – | pF | $V_R$ = 0 V, $f$ = 1 MHz, I/O to I/O |

1) Total capacitance line to ground

**Table 5 ESD Characteristics** at $T_A$ = 25 °C, unless otherwise specified

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Clamping voltage[1] [2] | $V_{CL}$ | – | 8 | – | V | $I_{PP}$ = 16 A, from I/O to GND |
| | | – | 11 | – | V | $I_{PP}$ = 30 A, from I/O to GND |
| Forward clamping voltage[1] [2] | $V_{FC}$ | – | 6 | – | V | $I_{PP}$ = 16 A, from GND to I/O |
| | | – | 9 | – | V | $I_{PP}$ = 30 A, from GND to I/O |
| Dynamic resistance[1] [2] | $R_{DYN}$ | – | 0.19 | – | Ω | I/O to GND |
| | | – | 0.23 | – | Ω | GND to I/O |

1) Please refer to Application Note AN210. TLP parameter: $Z_0$ = 50 Ω , $t_p$ = 100ns, $t_r$ = 300ps, averaging window: $t_1$ = 30 ns to $t_2$ = 60 ns, extraction of dynamic resistance using least squares fit of TLP charactertistic between $I_{PP1}$ = 10 A and $I_{PP2}$ = 40 A.

## 3.2 Typical Characteristics at $T_A$ = 25 °C, unless otherwise specified

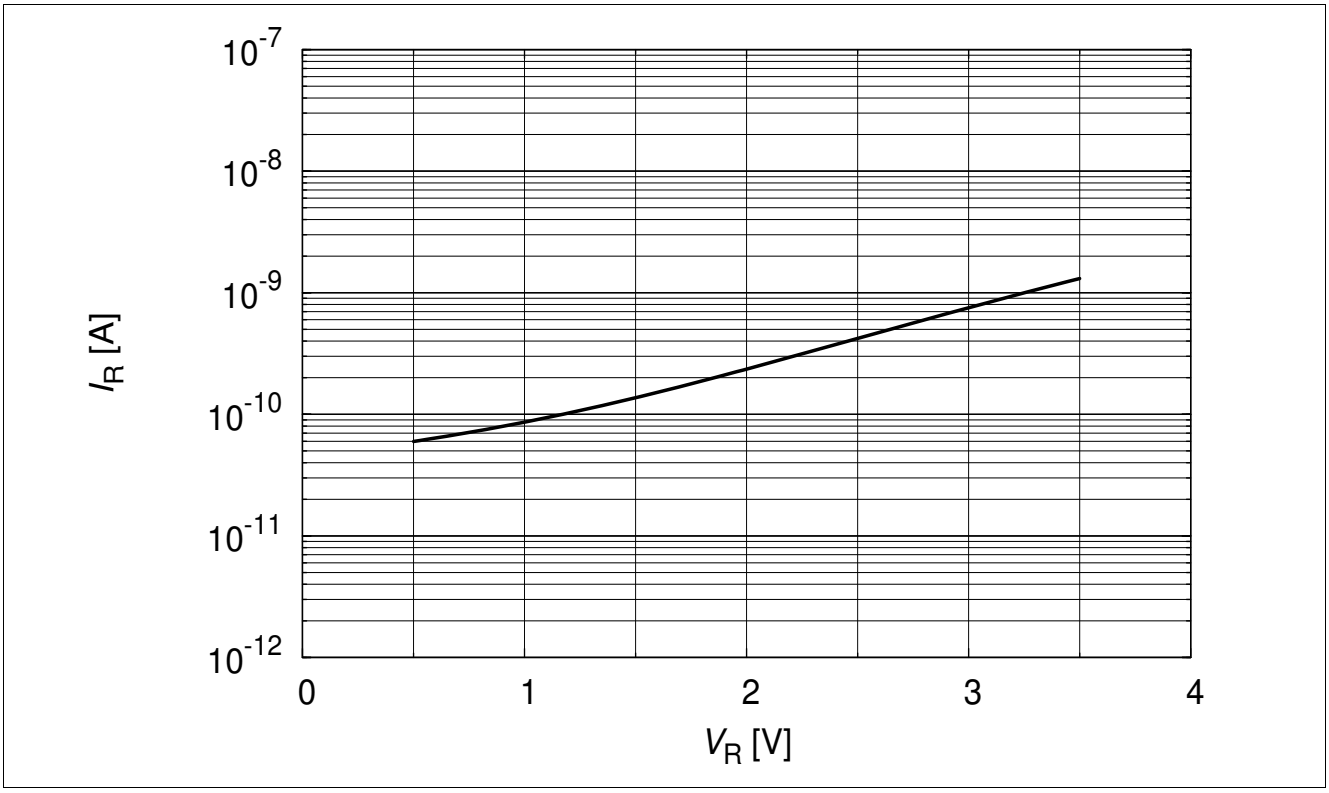


**Figure 3 Reverse curent, $I_R = (V_R)$**

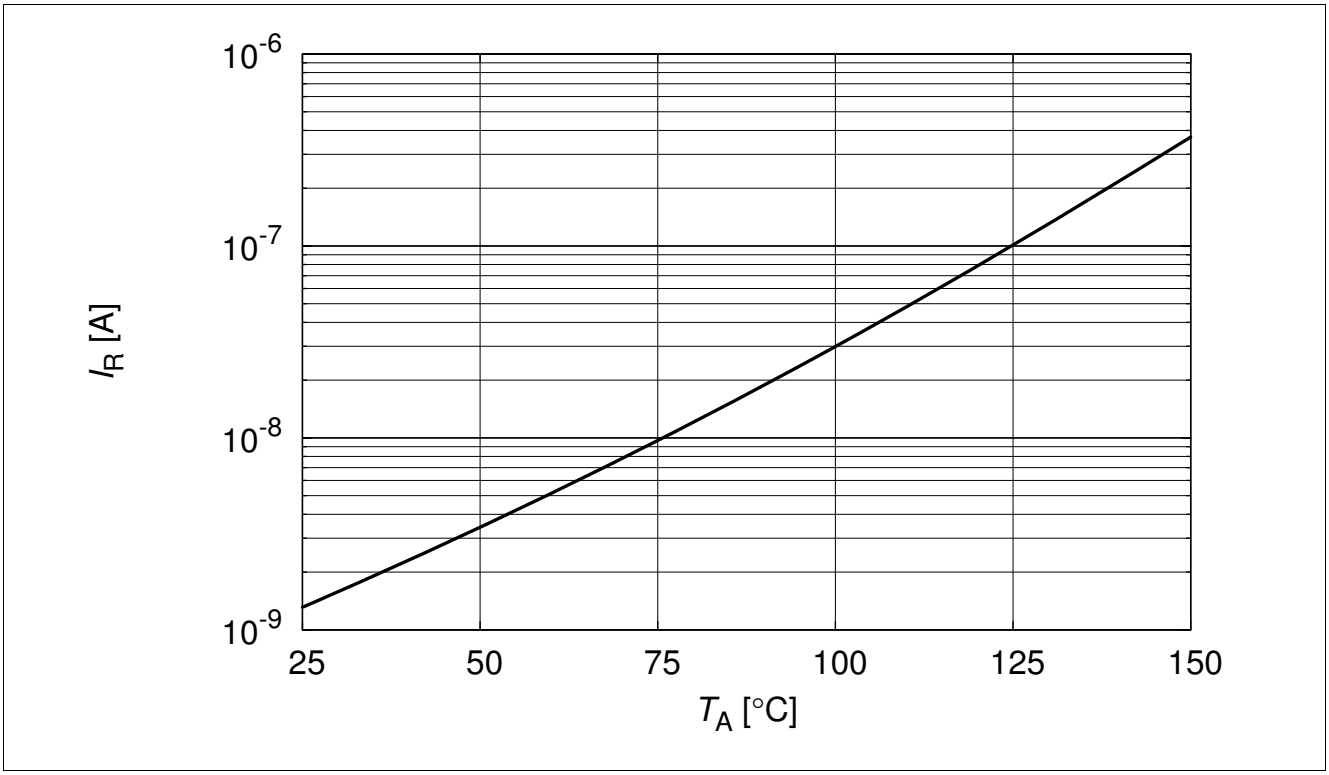


**Figure 4 Reverse current: $I_R = f(T_A)$, $V_R$ = 3.3 V**

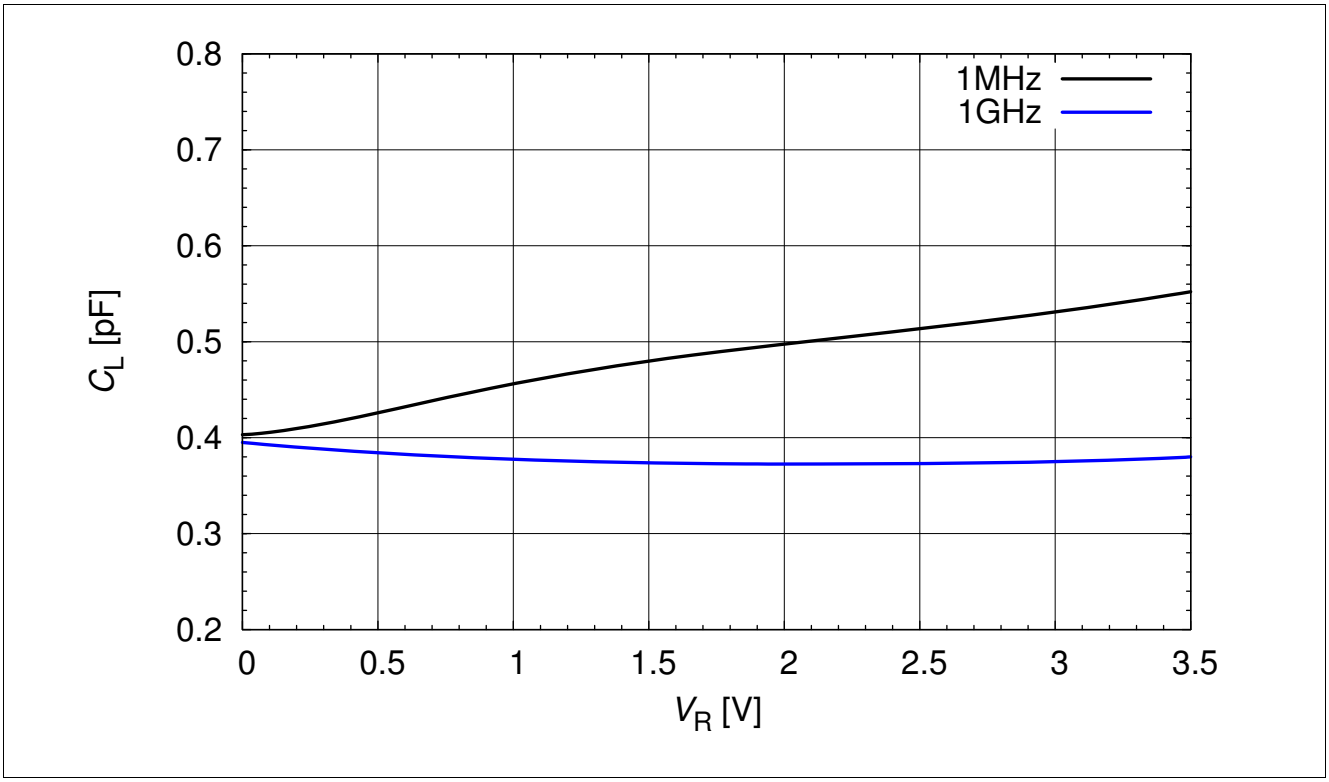


**Figure 5 Line capacitance: $C_L = f(V_R)$, $f$ = 1MHz, from I/O to GND**

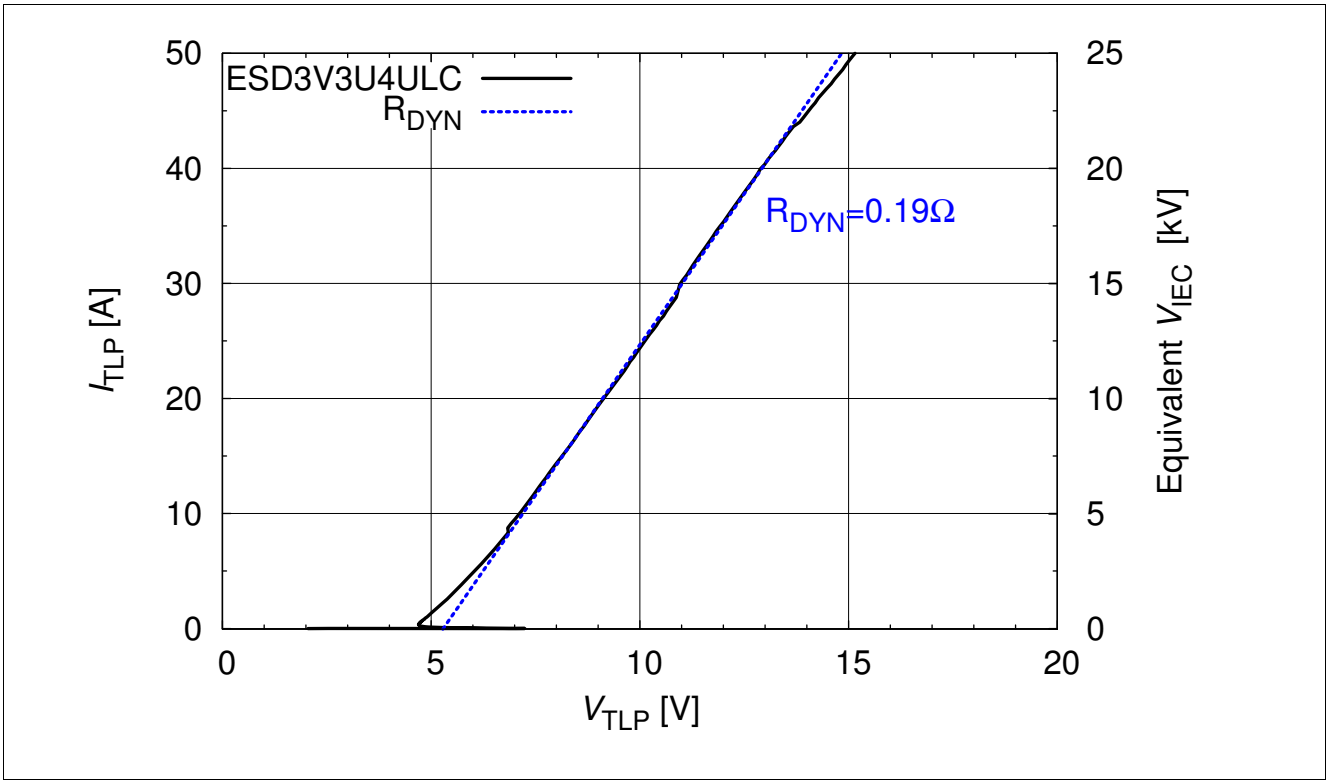


**Figure 6 Clamping voltage $V_{TLP} = f(I_{TLP})$, from I/O to GND** Note: [2]

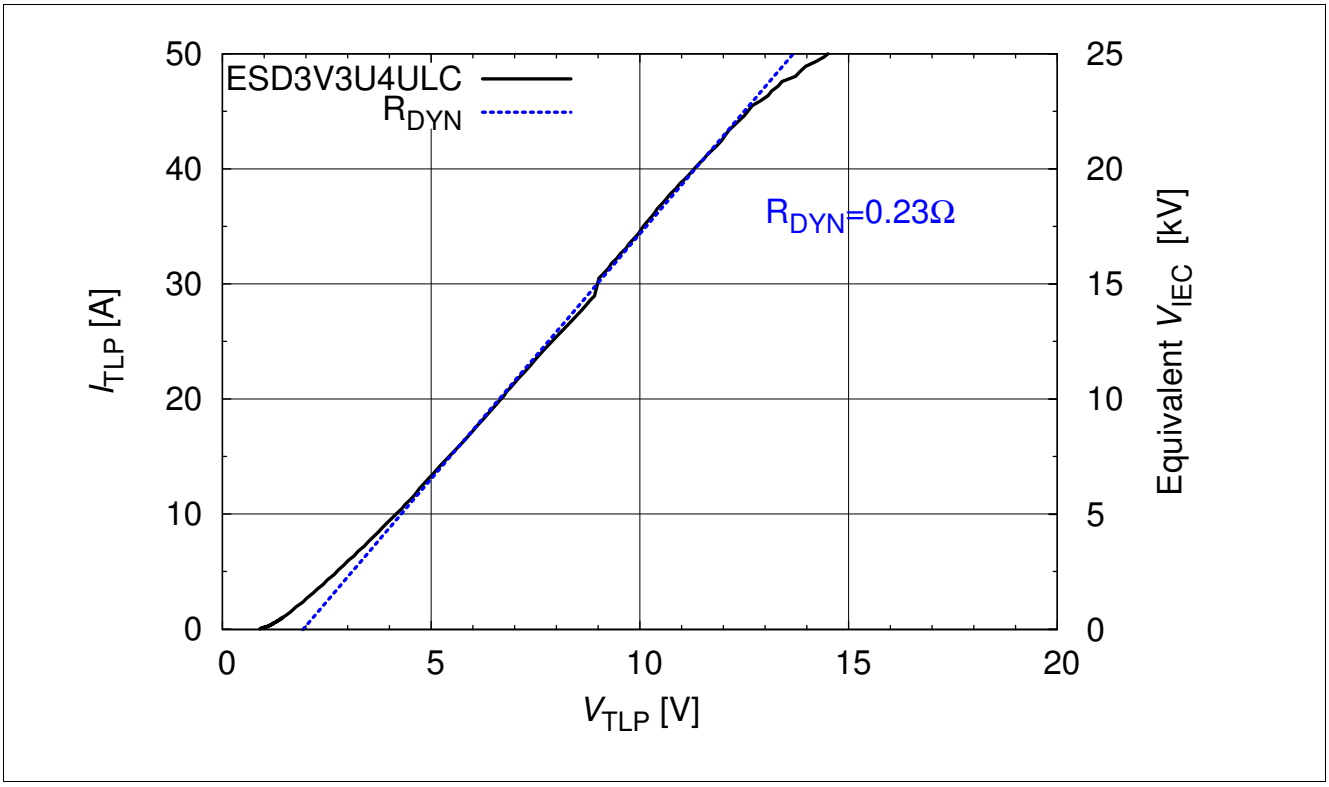


**Figure 7 Forward clamping voltage $V_{TLP} = f(I_{TLP})$, from GND to I/O** Note: [2]

*Note: TLP parameter: $Z_0$ = 50 Ω, $t_p$ = 100 ns, $t_r$ = 300 ps, averaging window: $t_1$ = 30 ns to $t_2$ = 60 ns, extraction of dynamic resistance using least squares fit of TLP charactertistic between $I_{PP1}$ = 10 A and $I_{PP2}$ = 40 A. The equivalent stress level $V_{IEC}$ according IEC 61000-4-2 ($R$ = 330 Ω, $C$ = 150 pF) is calculated at the broad peak of the IEC waveform at $t$ = 30 ns with 2 A / kV*

# 4 Application Information

To design USB3.0 link for best system level ESD performance and error free Signal Integrity is mandatory.

To bring both requirements together, the ESD protection devices has to provide excellent ESD and a very low device capacitance. The Infineon ESD3V3U4ULC in “array” configuration, combined with a clear and straight forward “full through” layout fulfills these requirements in the best way.

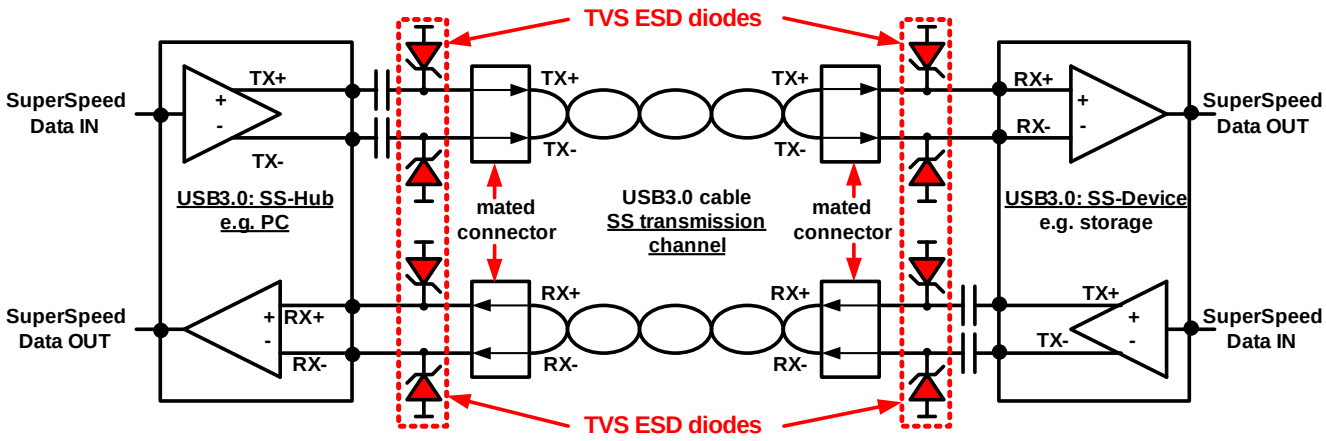


**Figure 8 USB3.0 structure with ESD protection devices [3]**

# 5 Ordering Information Scheme

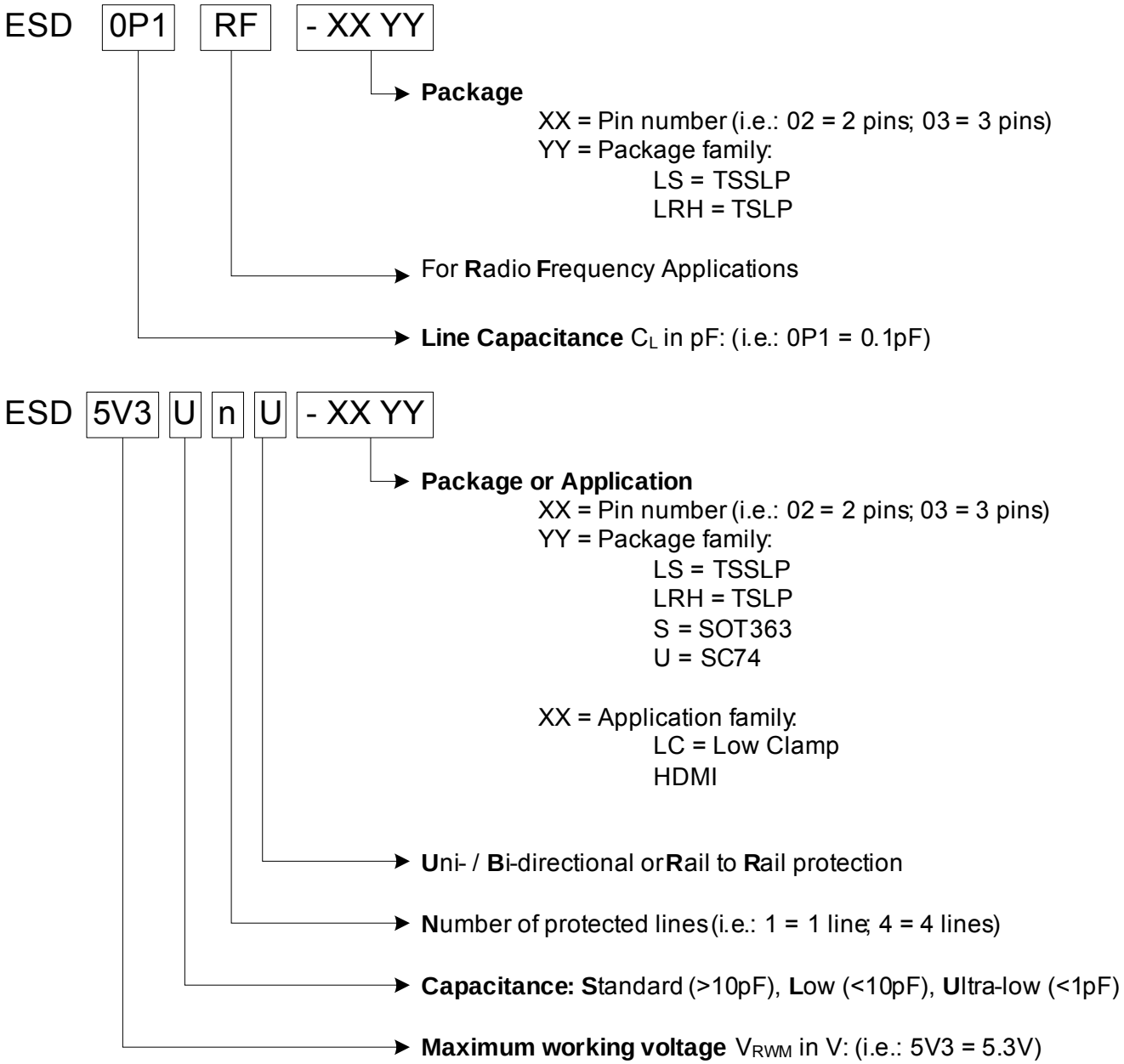


**Figure 9 Ordering information scheme**

# 6 Package Information

## 6.1 TSLP-9-1 (mm)

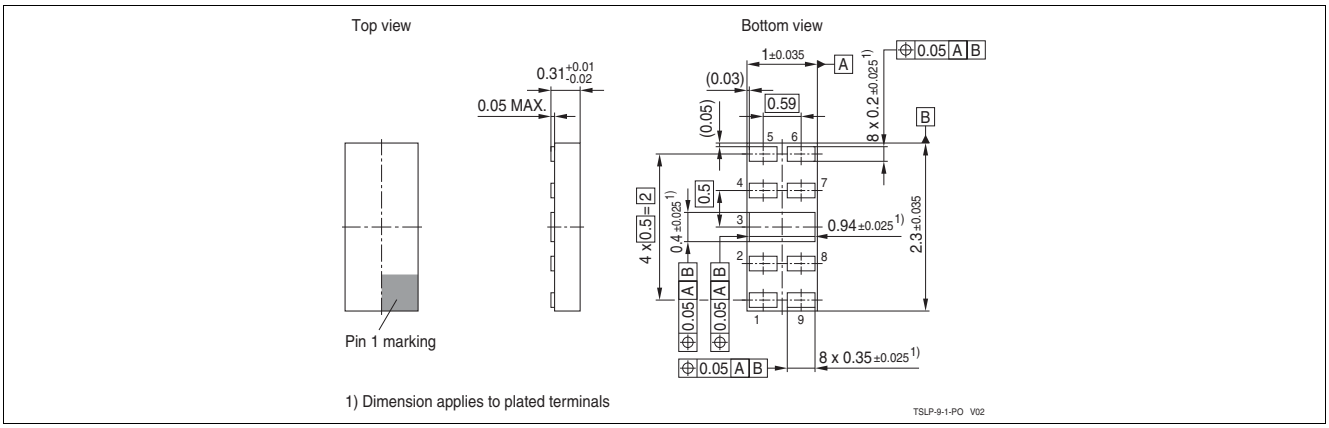


**Figure 10 TSLP-9-1: Package overview**

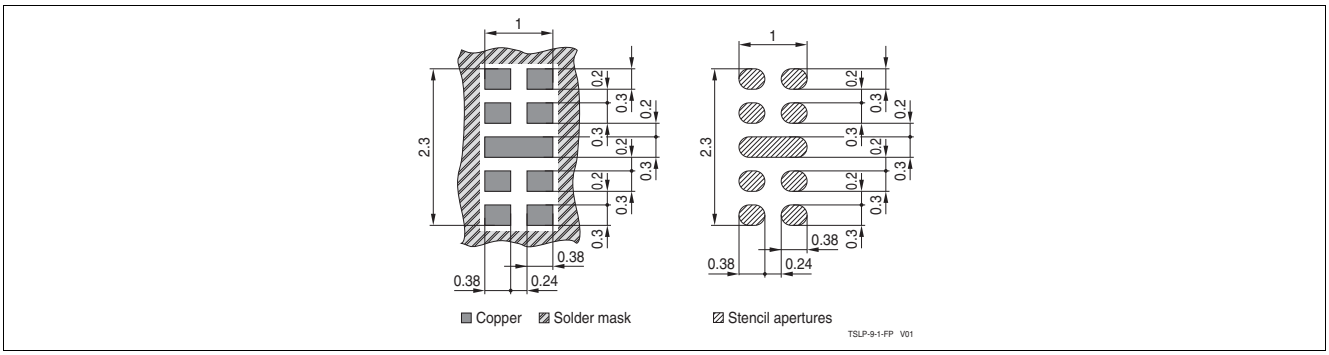


**Figure 11 TSLP-9-1: Footprint**

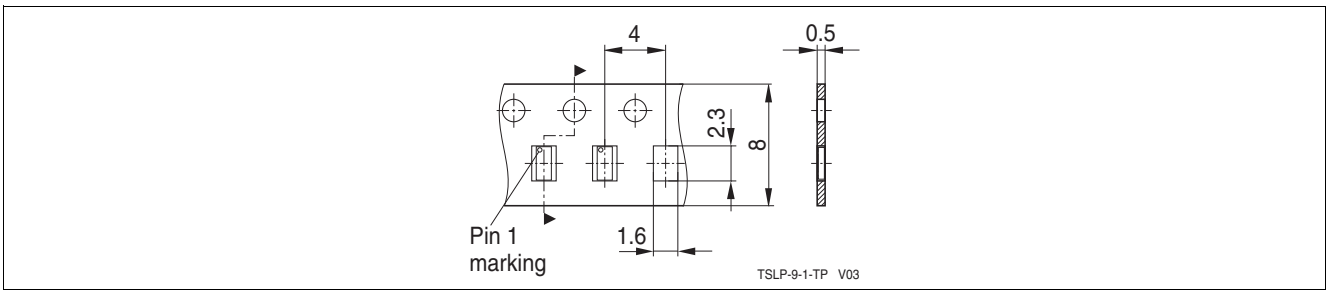


**Figure 12 TSLP-9-1: Packing**

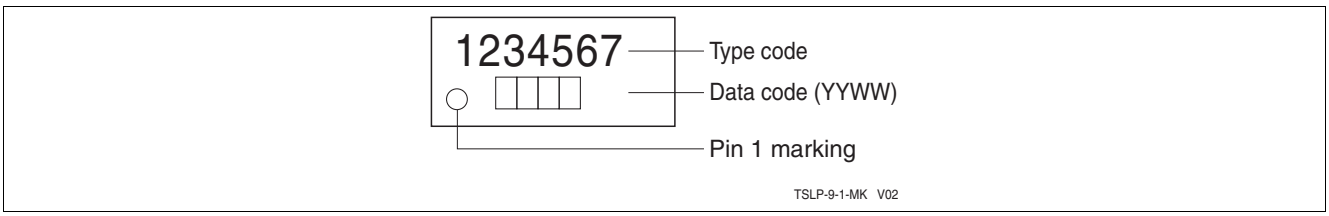


**Figure 13 TSLP-9-1: Marking**

# References

[1] **On-chip ESD protection for integrated circuits**, Albert Z. H. Wang, ISBN:0-7923-7647-1

[2] Infineon Technologie AG - **Application Note AN210**: Effective ESD Protection Design at System Level Using VF-TLP Characterization Methodology

[3] Infineon Technologie AG - **Application Note AN240**: Effective ESD Protection for USB3.0, combined with perfect Signal Intergrity.

w w w . i n f i n e o n . c o m

Published by Infineon Technologies AG