OptiMOS™ Power-Transistor

Features

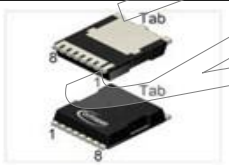
- N-channel, normal level
- Excellent gate charge x $R_{DS(on)}$ product (FOM)
- Extremely low on-resistance $R_{DS(on)}$
- High current capability
- 175 °C operating temperature
- Pb-free lead plating; RoHS compliant
- Qualified according to JEDEC[1] for target application
- Halogen-free according to IEC61249-2-21

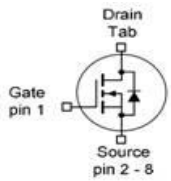
Product Summary

V_{DS}	100	V
$R_{DS(on),max}$	2.0	mΩ
I_D	300	A

RoHS

Halogen-Free

Type	IPT020N10N3
	
Package	PG-HSOF-8
Marking	020N10N3



Maximum ratings, at T_j=25 °C, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current	I_D	T_C=25 °C[2]	300	A
		T_C=100 °C	212	
Pulsed drain current[2]	$I_{D,pulse}$	T_C=25 °C	1200	
Avalanche energy, single pulse	E_{AS}	I_D=150 A, R_{GS}=25 Ω	800	mJ
Gate source voltage	V_{GS}		±20	V
Power dissipation	P_{tot}	T_C=25 °C	375	W
Operating and storage temperature	T_j, T_{stg}		-55 ... 175	°C
IEC climatic category; DIN IEC 68-1			55/175/56	

[1] J-STD20 and JESD22

[2] See figure 3

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Thermal characteristics						
Thermal resistance, junction - case	R_{thJC}		-	-	0.4	K/W
Thermal resistance, junction - ambient	R_{thJA}	minimal footprint	-	-	62	
		6 cm^2 cooling area[3)]	-	-	40	
Electrical characteristics, at T_j=25 °C, unless otherwise specified						
Static characteristics						
Drain-source breakdown voltage	$V_{(BR)DSS}$	V_{GS}=0 V, I_D=1 mA	100	-	-	V
Gate threshold voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=272 µA	2	2.7	3.5	
Zero gate voltage drain current	I_{DSS}	V_{DS}=100 V, V_{GS}=0 V, T_j=25 °C	-	0.1	1	µA
		V_{DS}=100 V, V_{GS}=0 V, T_j=125 °C	-	10	100	
Gate-source leakage current	I_{GSS}	V_{GS}=20 V, V_{DS}=0 V	-	1	100	nA
Drain-source on-state resistance	$R_{DS(on)}$	V_{GS}=10 V, I_D=150 A	-	1.7	2.0	mΩ
		V_{GS}=6 V, I_D=75 A,	-	2.2	3.7	
Gate resistance	R_G		-	1.9	-	Ω
Transconductance	g_{fs}	$\|V_{DS}\|>2\|I_D\|R_{DS(on)max}$, I_D=150 A	125	250	-	S

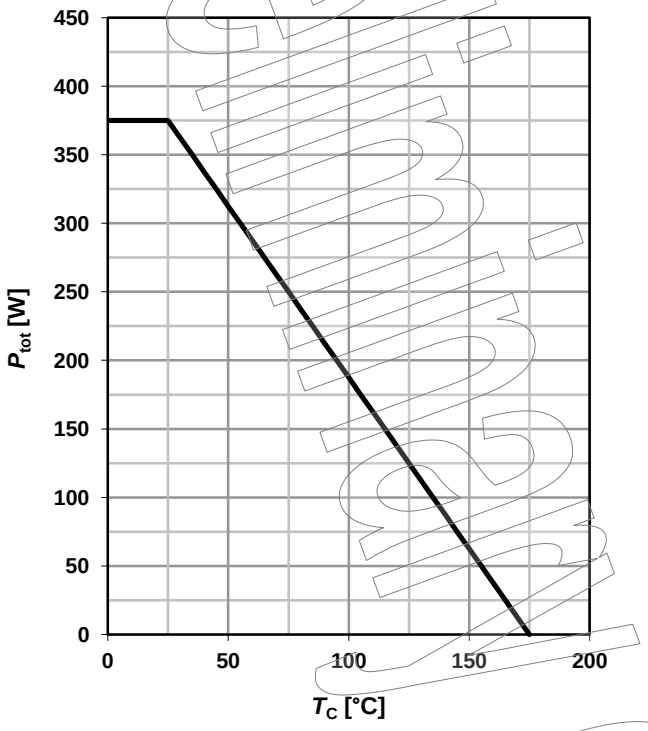
[3)] Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm^2 (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Dynamic characteristics						
Input capacitance	C_{iss}	V_{GS}=0 V, V_{DS}=50 V, f=1 MHz	-	11200	-	pF
Output capacitance	C_{oss}		-	2010	-	
Reverse transfer capacitance	C_{rss}		-	69	-	
Turn-on delay time	$t_{d(on)}$	V_{DD}=50 V, V_{GS}=10 V, I_D=100 A, $R_{G,ext}$=1.6 Ω	-	34	-	ns
Rise time	t_r		-	58	-	
Turn-off delay time	$t_{d(off)}$		-	84	-	
Fall time	t_f		-	18	-	
Gate Charge Characteristics[4)]						
Gate to source charge	Q_{gs}	V_{DD}=50 V, I_D=100 A, V_{GS}=0 to 10 V	-	48	-	nC
Gate to drain charge	Q_{gd}		-	27	-	
Switching charge	Q_{sw}		-	42	-	
Gate charge total	Q_g		-	156	-	
Gate plateau voltage	$V_{plateau}$		-	4.3	-	V
Output charge	Q_{oss}	V_{DD}=50 V, V_{GS}=0 V	-	192	-	nC
Reverse Diode						
Diode continous forward current	I_S	T_C=25 °C	-	-	300	A
Diode pulse current	$I_{S,pulse}$		-	-	1200	
Diode forward voltage	V_{SD}	V_{GS}=0 V, I_F=150 A, T_j=25 °C	-	0.89	1	V
Reverse recovery time	t_{rr}	V_R=50 V, I_F=I_S, di_F/dt=100 A/µs	-	86		ns
Reverse recovery charge	Q_{rr}		-	232	-	nC

[4)] See figure 16 for gate charge parameter definition

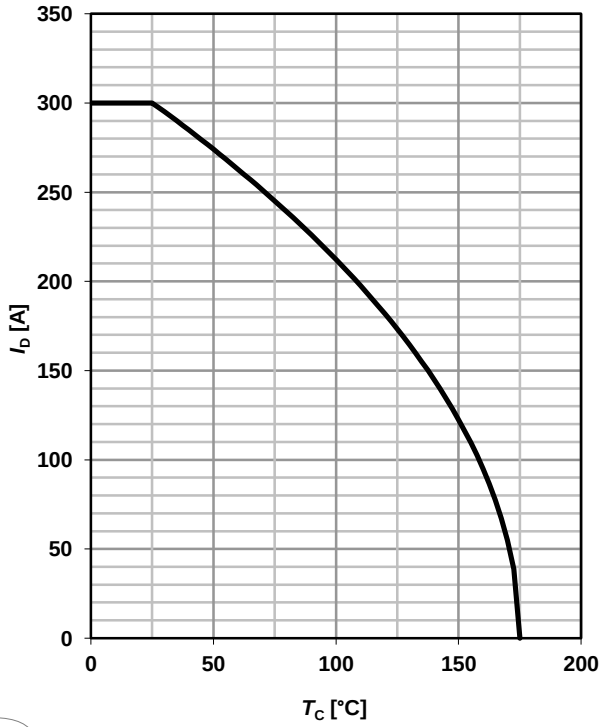
1 Power dissipation

$P_{tot}=f(T_C)$



2 Drain current

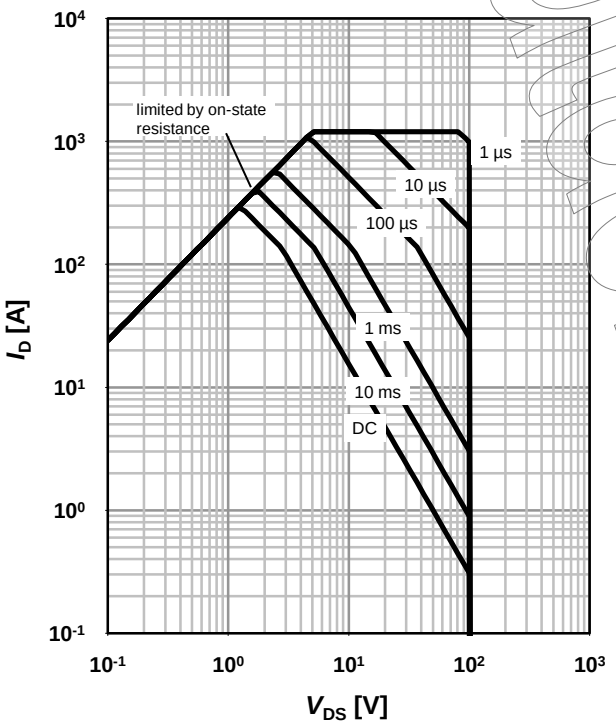
$I_D=f(T_C)$; $V_{GS}\geq 10$ V



3 Safe operating area

$I_D=f(V_{DS})$; $T_C=25$ °C; $D=0$

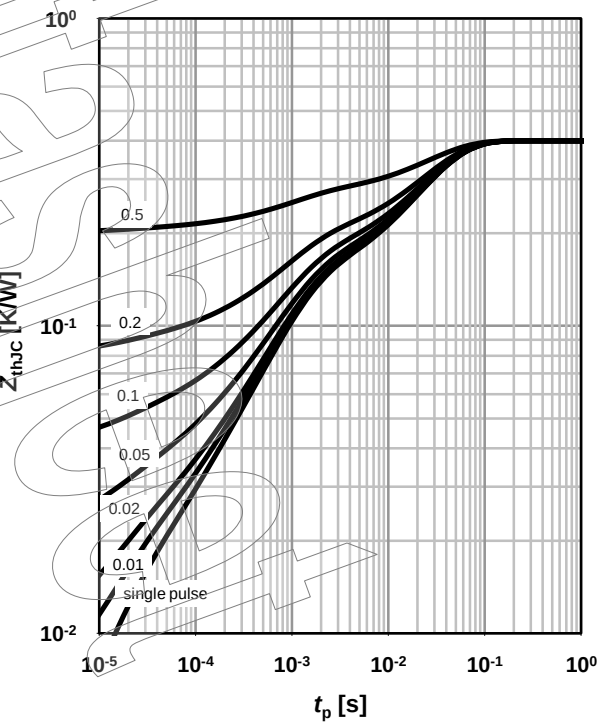
parameter: t_p



4 Max. transient thermal impedance

$Z_{thJC}=f(t_p)$

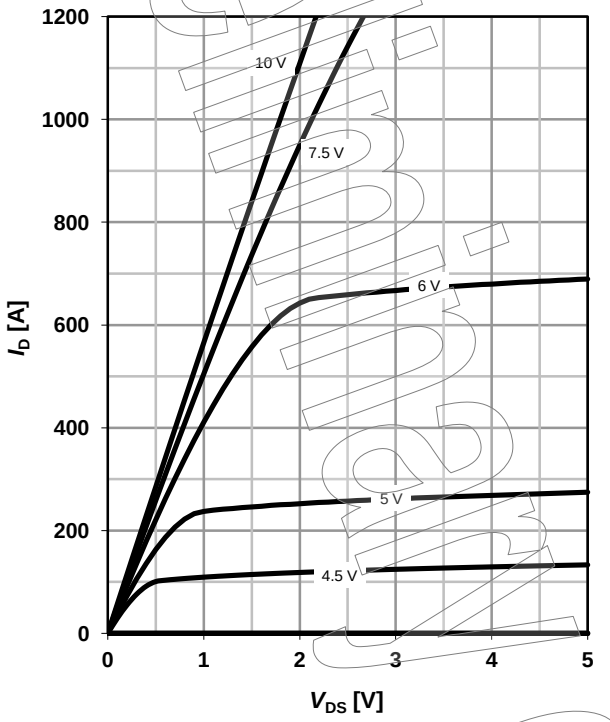
parameter: $D=t_p/T$



5 Typ. output characteristics

$I_D=f(V_{DS})$; $T_j=25$ °C

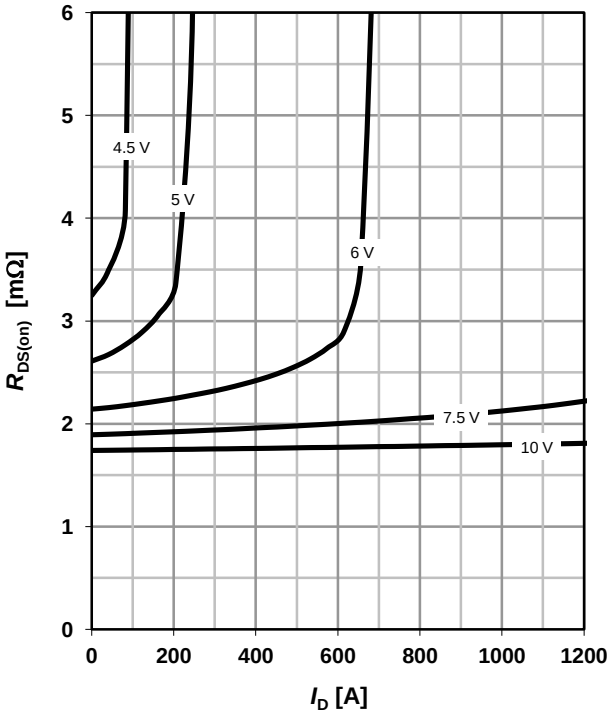
parameter: V_{GS}



6 Typ. drain-source on resistance

$R_{DS(on)}=f(I_D)$; $T_j=25$ °C

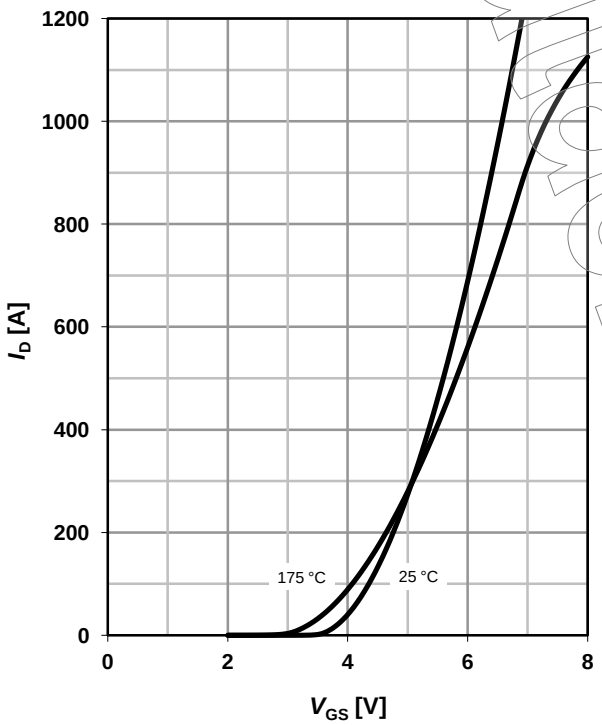
parameter: V_{GS}



7 Typ. transfer characteristics

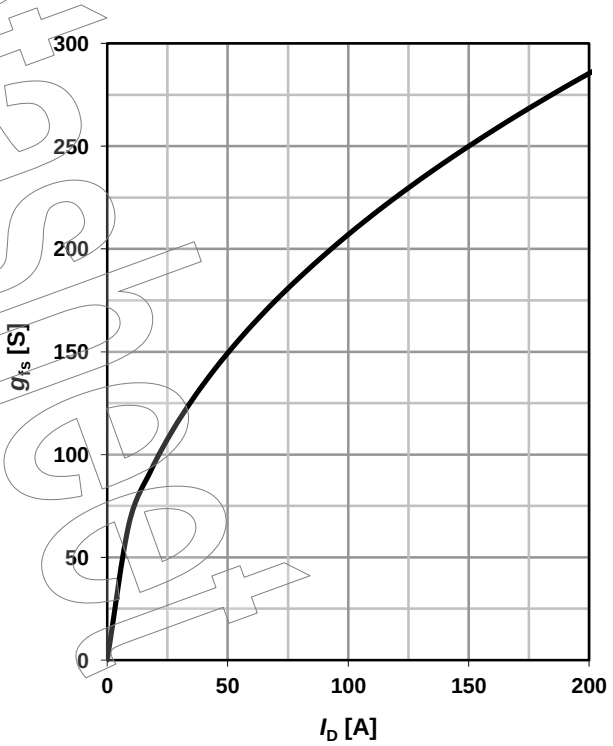
$I_D=f(V_{GS})$; $|V_{DS}|>2|I_D|R_{DS(on)max}$

parameter: T_j



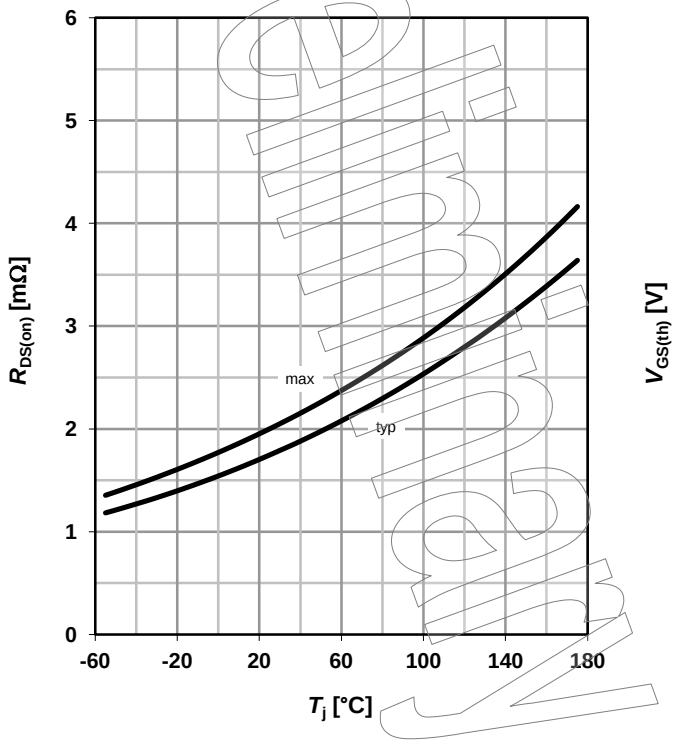
8 Typ. forward transconductance

$g_{fs}=f(I_D)$; $T_j=25$ °C



9 Drain-source on-state resistance

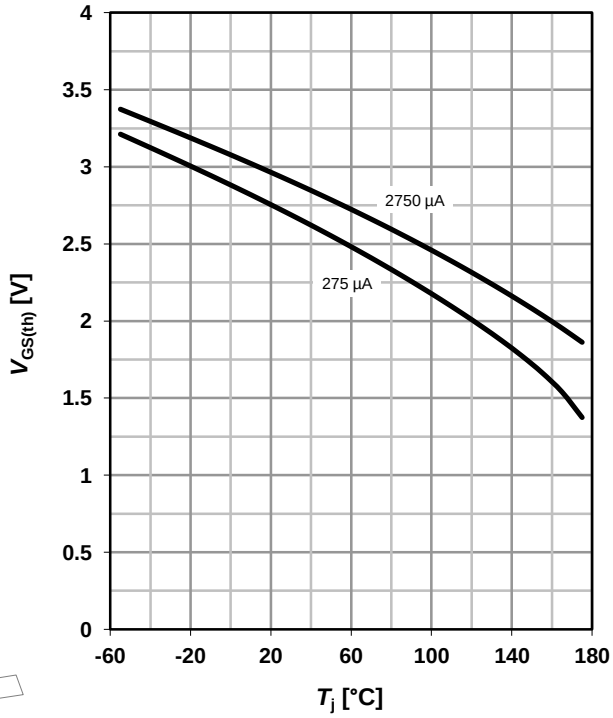
$R_{DS(on)}=f(T_j)$; $I_D=150$ A; $V_{GS}=10$ V



10 Typ. gate threshold voltage

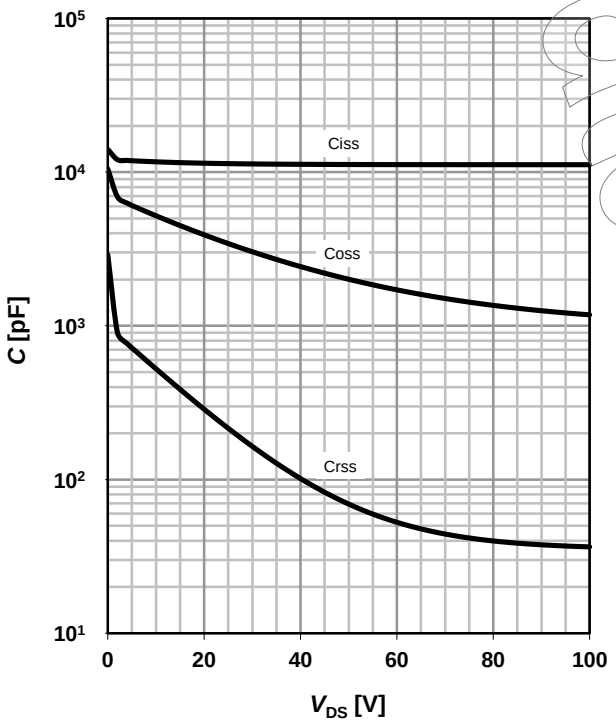
$V_{GS(th)}=f(T_j)$; $V_{GS}=V_{DS}$

parameter: I_D



11 Typ. capacitances

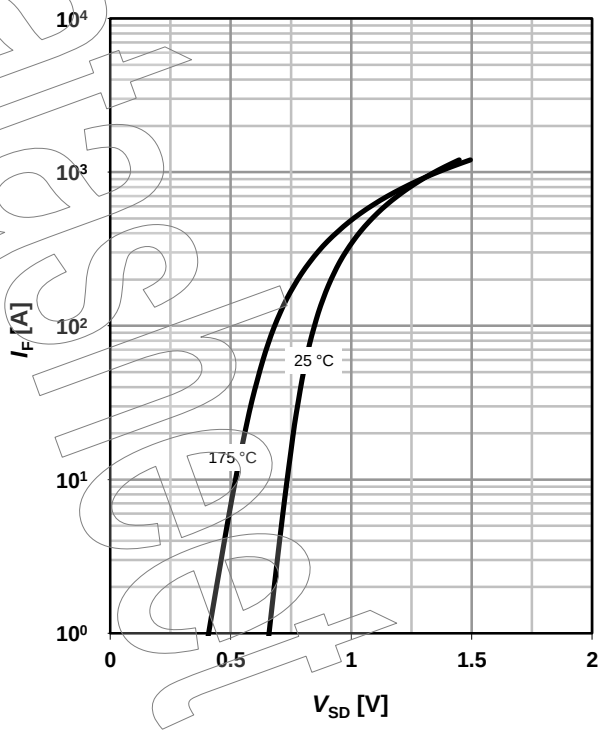
$C=f(V_{DS})$; $V_{GS}=0$ V; $f=1$ MHz



12 Forward characteristics of reverse diode

$I_F=f(V_{SD})$

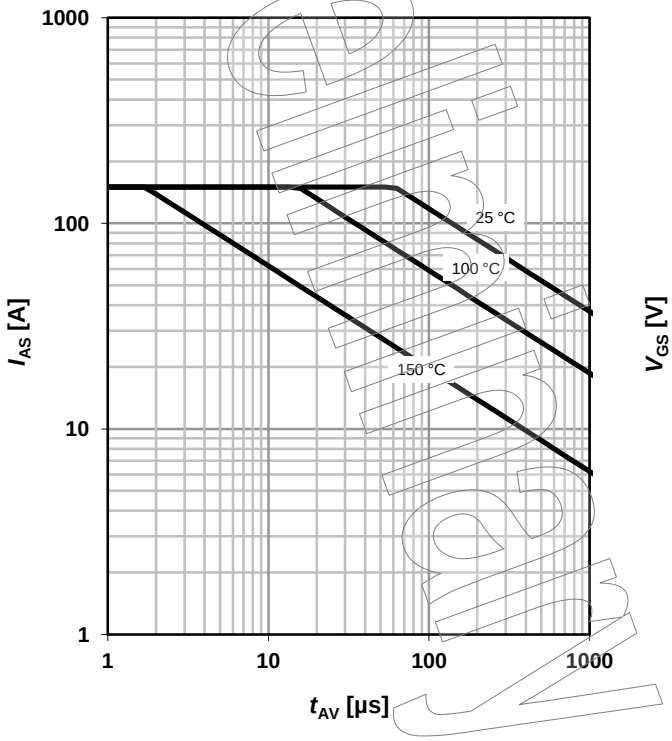
parameter: T_j



13 Avalanche characteristics

I_{AS}=f(t_{AV}); R_{GS}=25 Ω

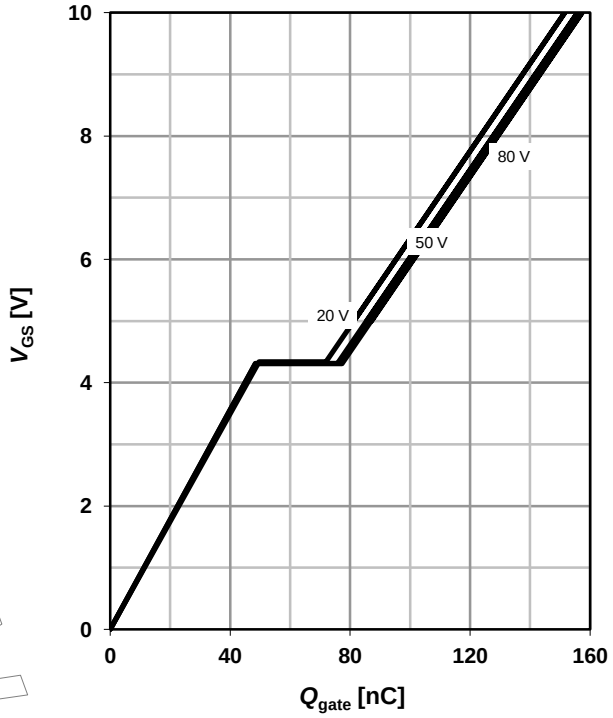
parameter: $T_{j(start)}$



14 Typ. gate charge

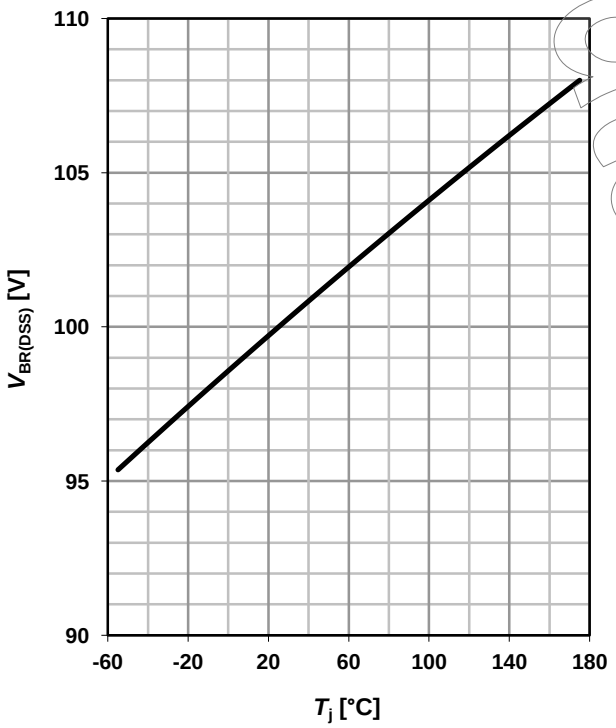
V_{GS}=f(Q_{gate}); I_D=100 A pulsed

parameter: V_{DD}

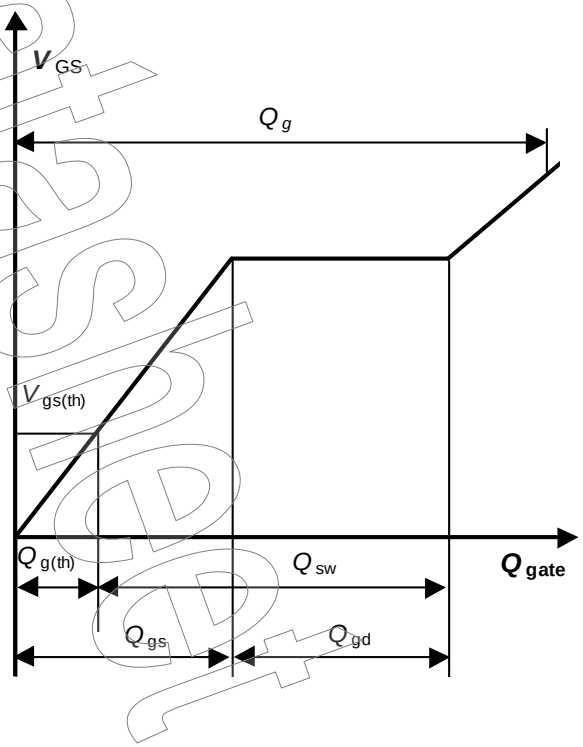


15 Drain-source breakdown voltage

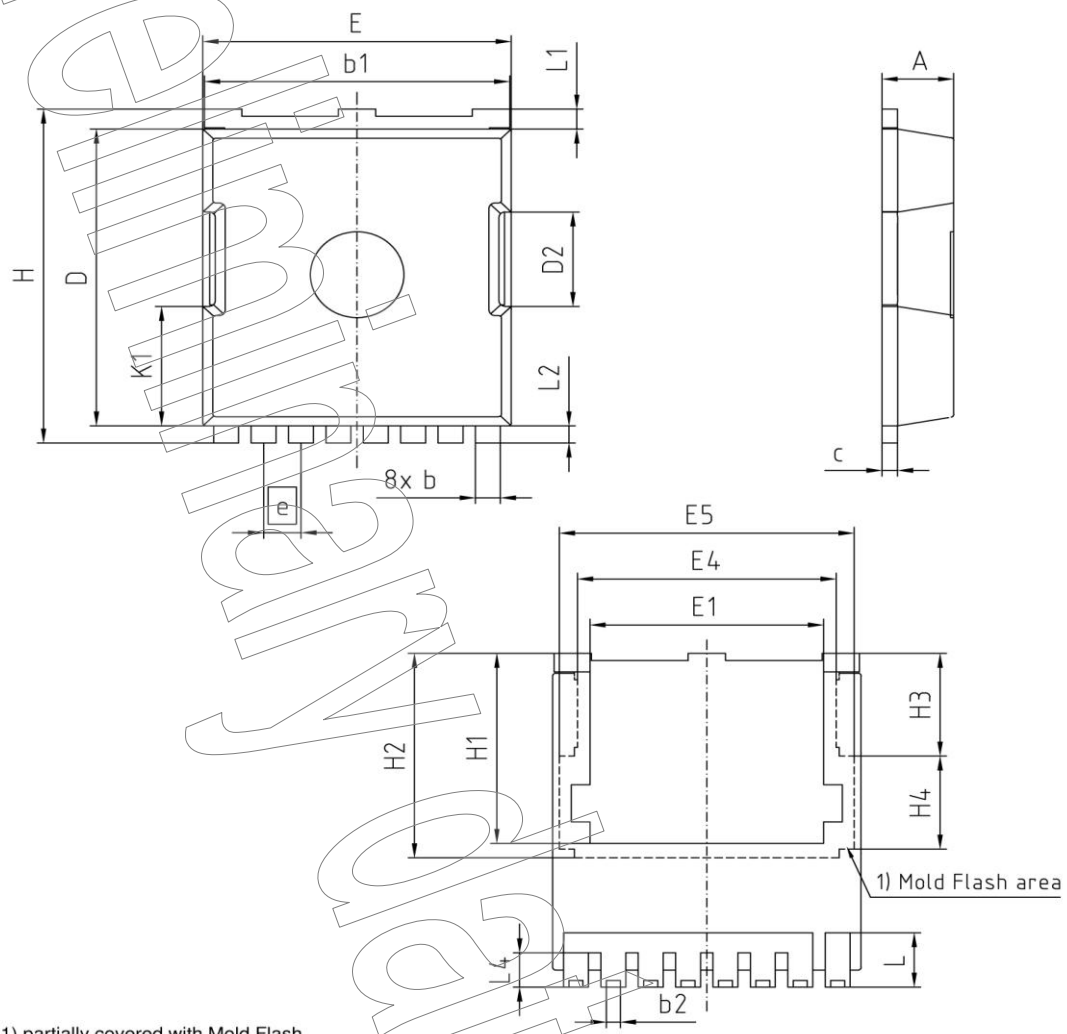
$V_{BR(DSS)}$=f(T_j); I_D=1 mA



16 Gate charge waveforms

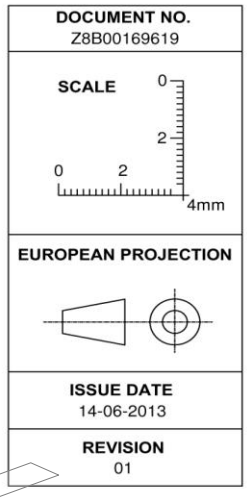


Package Outline



1) partially covered with Mold Flash

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.20	2.40	0.087	0.094
b	0.70	0.90	0.028	0.035
b1	9.70	9.90	0.382	0.390
b2	0.42	0.50	0.017	0.020
c	0.40	0.60	0.016	0.024
D	10.28	10.58	0.405	0.416
D2	3.30		0.130	
E	9.70	10.10	0.382	0.398
E1	7.50		0.295	
E4	8.50		0.335	
E5	9.46		0.372	
e	1.20 (BSC)		0.047 (BSC)	
H	11.48	11.88	0.452	0.468
H1	6.55	6.75	0.258	0.266
H2	7.15		0.281	
H3	3.59		0.141	
H4	3.26		0.128	
N	8		8	
K1	4.18		0.165	
L	1.60	2.10	0.063	0.083
L1	0.50	0.90	0.020	0.035
L2	0.50	0.70	0.020	0.028
L4	1.00	1.30	0.039	0.051



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