intel

87C51/80C51BH/80C31BH
CHMOS SINGLE-CHIP 8-BIT MICROCONTROLLER WITH 4 KBYTES INTERNAL PROGRAM MEMORY

87C51/80C51BH/80C31BH—3.5 to 12 MHz, V_{CC} = 5V ±20%
87C51-1/80C51BH-1/80C31BH-1—3.5 to 16 MHz, V_{CC} = 5V ±20%
87C51-2/80C51BH-2/80C31BH-2—0.5 to 12 MHz, V_{CC} = 5V ±20%
87C51-L—3.5 MHz to 8 MHz, V_{CC} = 3.3V ±0.3V

- **High Performance CHMOS EPROM**
- **Low Voltage Operation (-L Only)**
- **Improved Quick-Pulse Programming Algorithm**
- **3-Level Program Memory Lock**
- **Boolean Processor**
- **128-Byte Data RAM**
- **32 Programmable I/O Lines**
- **Two 16-Bit Timer/Counters**
- **5 Interrupt Sources**
- **Programmable Serial Port**
- **TTL- and CMOS-Compatible Logic Levels**
- **64K External Program Memory Space**
- **64K External Data Memory Space**
- **Idle and Power Down Modes**
- **ONCE Mode Facilitates System Testing**
- **Power Control Modes**

MEMORY ORGANIZATION

PROGRAM MEMORY: Up to 4 Kbytes of the program memory can reside on-chip (except 80C31BH). In addition the device can address up to 64K of program memory external to the chip.

DATA MEMORY: This microcontroller has a 128 x 8 on-chip RAM. In addition it can address up to 64 Kbytes of external data memory.

The Intel 87C51 is a single-chip control-oriented microcontroller which is fabricated on Intel's reliable CHMOS III-E technology. The Intel 80C51BH/80C31BH is fabricated on CHMOS III technology. Being a member of the MCS®-51 family, the 87C51/80C51BH/80C31BH uses the same powerful instruction set, has the same architecture, and is pin-for-pin compatible with the existing MCS-51 family of products.

Applications that require low voltage can use the 87C51-L. The 87C51-L will operate at 3.3V ±0.3V at a frequency range of 3.5 MHz to 8 MHz.

The extremely low operating power, along with the two reduced power modes, Idle and Power Down, make this part very suitable for low power applications. The Idle mode freezes the CPU while allowing the RAM, timer/counters, serial port and interrupt system to continue functioning. The Power Down mode saves the RAM contents but freezes the oscillator, causing all other chip functions to be inoperative.

For the remainder of this document, the 87C51, 80C51BH, and 80C31BH will be referred to as the 87C51/BH, unless information applies to a specific device.

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October 1992
Order Number: 270147-008

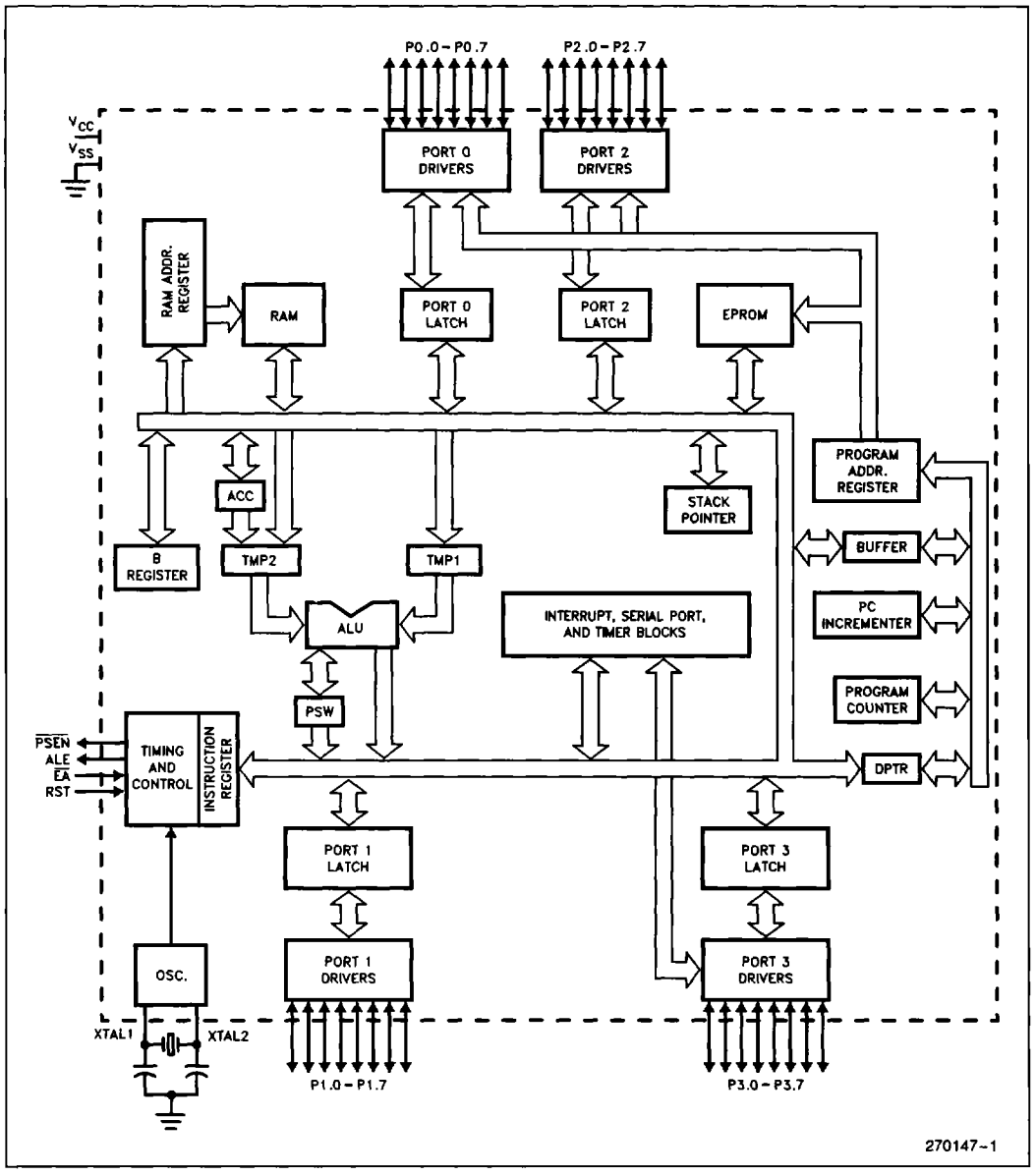

Figure 1. 87C51/BH Block Diagram

PROCESS INFORMATION

The 87C51 is manufactured on P629.0, a CHMOS III-E process. The 80C51BH/80C31BH are manufactured on P645, a CHMOS III process. Additional process and reliability information is available in Intel's *Components Quality and Reliability Handbook,* Order Number 210997.

PACKAGES

Part	Prefix	Package Type	θ_{ja}	θ_{jc}
87C51	P	40-Pin Plastic DIP (OTP)	45°C/W	16°C/W
	D	40-Pin CERDIP (EPROM)	45°C/W	15°C/W
	N	44-Pin PLCC (OTP)	46°C/W	16°C/W
	S	44-Pin QFP (OTP)	98°C/W	24°C/W

Part	Prefix	Package Type	θ_{ja}	θ_{jc}
80C51BH/ 80C31BH	P	40-Pin Plastic DIP	75°C/W	23°C/W
	D	40-Pin CERDIP	36°C/W	13°C/W
	N	44-Pin PLCC	46°C/W	16°C/W
	S	44-Pin QFP	98°C/W	24°C/W

All thermal impedance data is approximate for static air conditions at 1W of power dissipation. Values will change depending on operating conditions and application. See the Intel *Packaging Handbook* (Order Number 240800) for a description of Intel's thermal impedance test methodology.

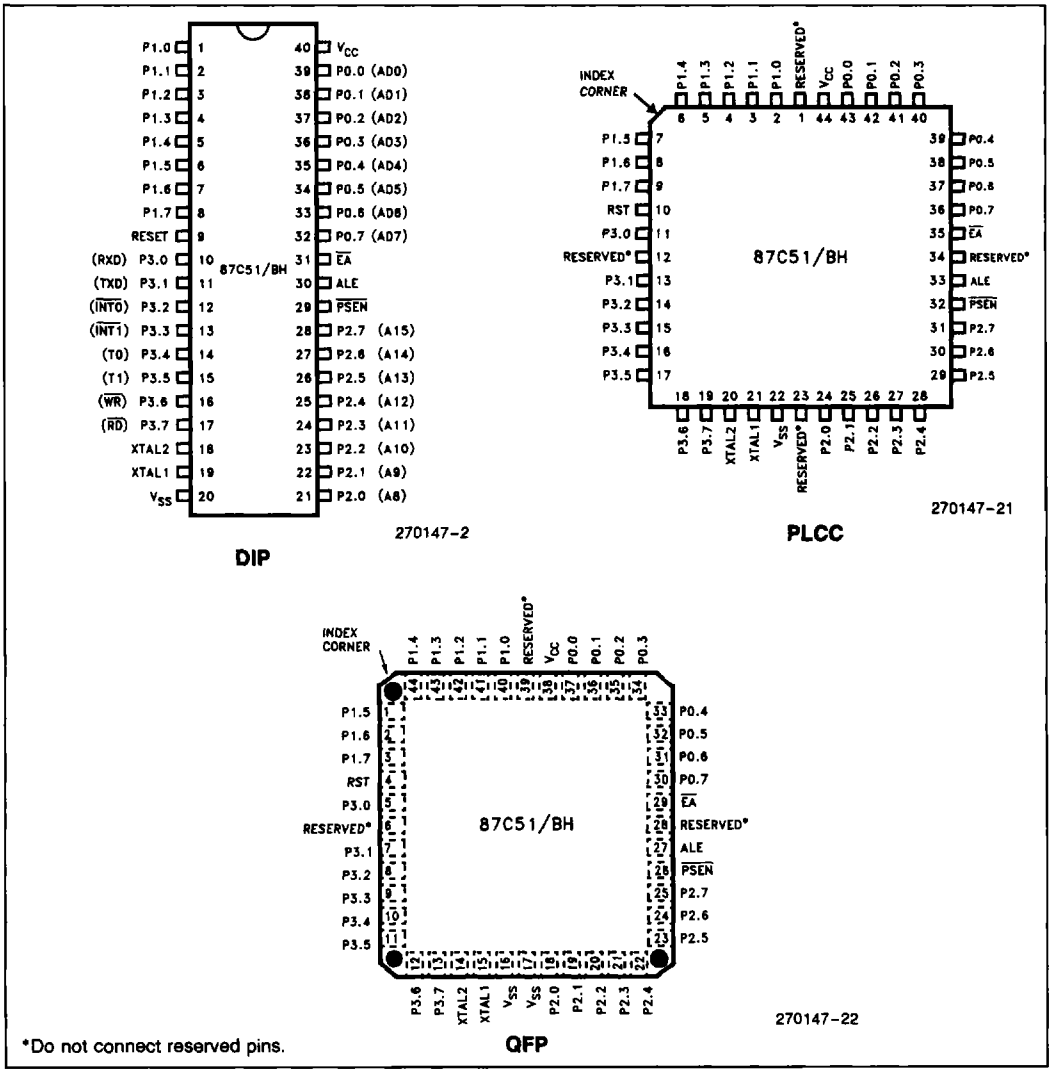

Figure 2. Pin Connections

PIN DESCRIPTION

V_{CC}: Supply voltage during normal, Idle and Power Down operations.

V_{SS}: Circuit ground.

Port 0: Port 0 is an 8-bit open drain bidirectional I/O port. As an output port each pin can sink 8 LS TTL inputs. Port 0 pins that have 1's written to them float, and in that state can be used as high-impedance inputs.

Port 0 is also the multiplexed low-order address and data bus during accesses to external memory. In this application it uses strong internal pullups when emitting 1's.

Port 0 also receives the code bytes during EPROM programming, and outputs the code bytes during program verification. External pullups are required during program verification.

Port 1: Port 1 is an 8-bit bidirectional I/O port with internal pullups. Port 1 pins that have 1's written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 1 pins that are externally pulled low will source current (I_{IL}, on the data sheet) because of the internal pullups.

Port 1 also receives the low-order address bytes during EPROM programming and program verification.

Port 2: Port 2 is an 8-bit bidirectional I/O port with internal pullups. Port 2 pins that have 1's written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 2 pins that are externally pulled low will source current (I_{IL}, on the data sheet) because of the internal pullups.

Port 2 emits the high-order address byte during fetches from external Program memory and during accesses to external Data Memory that use 16-bit address (MOVX @DPTR). In this application it uses strong internal pullups when emitting 1's.

During accesses to external Data Memory that use 8-bit addresses (MOVX @Ri), Port 2 emits the contents of the P2 Special Function Register.

Port 2 also receives some control signals and the high-order address bits during EPROM programming and program verification.

Port 3: Port 3 is an 8-bit bidirectional I/O port with internal pullups. Port 3 pins that have 1's written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 3 pins that are externally pulled low will source current (I_{IL}, on the data sheet) because of the pullups.

Port 3 also serves the functions of various special features of the MCS-51 Family, as listed below:

Pin	Name	Alternate Function
P3.0	RXD	Serial input line
P3.1	TXD	Serial output line
P3.2	$\overline{INT0}$	External Interrupt 0
P3.3	$\overline{INT1}$	External Interrupt 1
P3.4	T0	Timer 0 external input
P3.5	T1	Timer 1 external input
P3.6	$\overline{WR}$	External Data Memory Write strobe
P3.7	$\overline{RD}$	External Data Memory Read strobe

Port 3 also receives some control signals for EPROM programming and program verification.

RST: Reset input. A high on this pin for two machine cycles while the oscillator is running resets the device. The port pins will be driven to their reset condition when a minimum V_{IH1} voltage is applied whether the oscillator is running or not (87C51 only). An internal pulldown resistor permits a power-on reset with only a capacitor connected to V_{CC}.

ALE/$\overline{PROG}$: Address Latch Enable output signal for latching the low byte of the address during accesses to external memory. This pin is also the program pulse input ($\overline{PROG}$) during EPROM programming.

If desired, ALE operation can be disabled by setting bit 0 of SFR location 8EH. With the bit set, ALE is active only during a MOVX or MOVC instruction. Otherwise the pin is weakly pulled high. Setting the ALE-disable bit has no effect if the microcontroller is in external execution mode.

In normal operation ALE is emitted at a constant rate of 1/6 the oscillator frequency, and may be used for external timing or clocking purposes. Note, however, that one ALE pulse is skipped during each access to external Data Memory.

$\overline{PSEN}$: Program Store Enable is the Read strobe to External Program Memory. When the 87C51/BH is executing from Internal Program Memory, $\overline{PSEN}$ is inactive (high). When the device is executing code from External Program Memory, $\overline{PSEN}$ is activated

twice each machine cycle, except that two $\overline{PSEN}$ activations are skipped during each access to External Data Memory.

$\overline{EA}$/V_{PP}: External Access enable. $\overline{EA}$ must be strapped to V_{SS} in order to enable the 87C51/BH to fetch code from External Program Memory locations starting at 0000H up to FFFFH. Note, however, that if either of the Lock Bits is programmed, the logic level at $\overline{EA}$ is internally latched during reset.

$\overline{EA}$ must be strapped to V_{CC} for internal program execution.

This pin also receives the 12.75V programming supply voltage (V_{PP}) during EPROM programming.

XTAL1: Input to the inverting oscillator amplifier.

XTAL2: Output from the inverting oscillator amplifier.

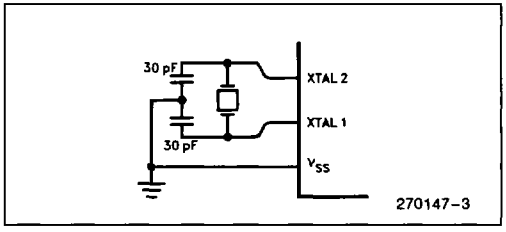

Figure 3. Using the On-Chip Oscillator

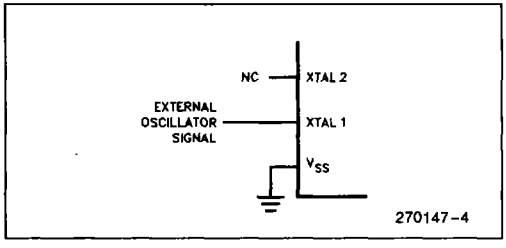

Figure 4. External Clock Drive

OSCILLATOR CHARACTERISTICS

XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier which can be configured for use as an on-chip oscillator, as shown in Figure 3.

To drive the device from an external clock source, XTAL1 should be driven, while XTAL2 is left unconnected, as shown in Figure 4. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide-by-two flip-flop, but minimum and maximum high and low times specified on the data sheet must be observed.

An external oscillator may encounter as much as a 100 pF load at XTAL1 when it starts up. This is due to interaction between the amplifier and its feedback capacitance. Once the external signal meets the V_{IL} and V_{IH} specifications the capacitance will not exceed 20 pF.

IDLE MODE

In Idle Mode, the CPU puts itself to sleep while all the on-chip peripherals remain active. The mode is invoked by software. The content of the on-chip RAM and all the Special Functions Registers remain unchanged during this mode. The Idle Mode can be terminated by any enabled interrupt or by a hardware reset.

It should be noted that when Idle is terminated by a hardware reset, the device normally resumes program execution, from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hardware inhibits access to internal RAM in this event, but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write to a port pin when Idle is terminated by reset, the instruction following the one that invokes Idle should not be one that writes to a port pin or to external memory.

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Table 1. Status of the External Pins during Idle and Power Down

Mode	Program Memory	ALE	$\overline{PSEN}$	PORT0	PORT1	PORT2	PORT3
Idle	Internal	1	1	Data	Data	Data	Data
Idle	External	1	1	Float	Data	Address	Data
Power Down	Internal	0	0	Data	Data	Data	Data
Power Down	External	0	0	Float	Data	Data	Data

NOTE:
For more detailed information on the reduced power modes refer to current Embedded Microcontrollers and Processors Handbook Volume I, and Application Note AP-252 (Embedded Applications Handbook), "Designing with the 80C51BH."

POWER DOWN MODE

In the Power Down mode the oscillator is stopped, and the instruction that invokes Power Down is the last instruction executed. The on-chip RAM and Special Function Registers retain their values until the Power Down mode is terminated.

The only exit from Power Down is a hardware reset. Reset redefines the SFRs but does not change the on-chip RAM. The reset should not be activated before V_{CC} is restored to its normal operating level and must be held active long enough to allow the oscillator to restart and stabilize.

DESIGN CONSIDERATIONS

- The 87C51-L will operate at 3.3V ±0.3V at a frequency range of 3.5 MHz to 8 MHz. Operating beyond these specifications could cause improper device functionality. (To program the 87C51-L, follow the same procedure as the 87C51.)
- Exposure to light when the device is in operation may cause logic errors. For this reason, it is suggested that an opaque label be placed over the window when the die is exposed to ambient light.
- The 87C51 has some additional features that are not available on the 80C51BH/80C31BH. The features are: asynchronous port reset, 4 interrupt priority levels, power off flag, ALE disable, serial port automatic address recognition, serial port framing error detection, 64-byte encryption array, and 3 program lock bits. These features cannot be used with the 80C51BH/80C31BH.

ONCE MODE

The ONCE ("On-Circuit Emulation") mode facilitates testing and debugging of systems using the 87C51/BH without the 87C51/BH having to be removed from the circuit. The ONCE mode is invoked by:

1. Pull ALE low while the device is in reset and $\overline{PSEN}$ is high;
2. Hold ALE low as RST is deactivated.

While the device is in ONCE mode, the Port 0 pins float, and the other port pins and ALE and $\overline{PSEN}$ are weakly pulled high. The oscillator circuit remains active. While the 87C51BH is in this mode, an emulator or test CPU can be used to drive the circuit. Normal operation is restored when a normal reset is applied.

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias . −40°C to +85°C
Storage Temperature ..... −65°C to +150°C
Voltage on $\overline{EA}$/V_{PP} Pin to V_{SS} ..... 0V to +13.0V
Voltage on Any Other Pin to V_{SS} .. −0.5V to +6.5V
Maximum I_{OL} per I/O Pin ..... 15 mA
Power Dissipation 1.5W
(Based on package heat transfer limitations, not device power consumption).

NOTICE: This data sheet contains preliminary information on new products in production. It is valid for the devices indicated in the revision history. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

OPERATING CONDITIONS

T_A (under Bias) = 0°C to +70°C; V_{CC} = 5V ±20%; V_{SS} = 0V (87C51-L, V_{CC} = 3.3V ±0.3V)

DC CHARACTERISTICS (Over Operating Conditions)

All parameter values apply to all devices unless otherwise indicated.

Symbol	Parameter	Min	Typ(1)	Max	Unit	Test Conditions
V_{IL}	Input Low Voltage	−0.5		0.2 V_{CC} − 0.1	V	
V_{IL1}	Input Low Voltage $\overline{EA}$	0		0.2 V_{CC} − 0.3	V	
V_{IH}	Input High Voltage (Except XTAL1, RST)	0.2 V_{CC} + 0.9		V_{CC} + 0.5	V	
V_{IH1}	Input High Voltage (XTAL1, RST)	0.7 V_{CC}		V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage(6) (Ports 1, 2, 3)			0.3	V	I_{OL} = 100 μA(2)
				0.45	V	I_{OL} = 1.6 mA(2)
				1.0	V	I_{OL} = 3.5 mA(2)
V_{OL1}	Output Low Voltage(6) (Port 0, ALE, $\overline{PSEN}$)			0.3	V	I_{OL} = 200 μA(2)
				0.45	V	I_{OL} = 3.2 mA (2)
				1.0	V	I_{OL} = 7.0 mA(2)
V_{OH}	Output High Voltage (Ports 1, 2, 3, ALE, $\overline{PSEN}$) 87C51	V_{CC} − 0.3			V	I_{OH} = −10 μA(3)
		V_{CC} − 0.7			V	I_{OH} = −30 μA(3)
		V_{CC} − 1.5			V	I_{OH} = −60 μA(3)
V_{OH}	Output High Voltage (Ports 1, 2, 3, ALE, $\overline{PSEN}$) 80C51BH/31BH	0.9 V_{CC}			V	I_{OH} = −10 μA(3) V_{CC} = 5V ±10%
		0.75 V_{CC}			V	I_{OH} = −25 μA
		2.4			V	I_{OH} = −60 μA(3)
V_{OH1}	Output High Voltage (Port 0 in External Bus Mode) 87C51	V_{CC} − 0.3			V	I_{OH} = −200 μA(3)
		V_{CC} − 0.7			V	I_{OH} = −3.2 mA(3)
		V_{CC} − 1.5			V	I_{OH} = −7.0 mA(3)
V_{OH1}	Output High Voltage (Port 0 in External Bus Mode) 80C51BH/31BH	0.9 V_{CC}			V	I_{OH} = −80 μA V_{CC} = 5V ±10%
		0.75 V_{CC}			V	I_{OH} = −300 μA
		2.4			V	I_{OH} = −800 μA

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DC CHARACTERISTICS (Over Operating Conditions) (Continued)

Symbol	Parameter	Min	Typ(1)	Max	Unit	Test Conditions
I_{IL}	Logical 0 Input Current (Ports 1, 2, 3)			−50	μA	V_{IN} = 2V (87C51) V_{IN} = 0.45V
I_{LI}	Input Leakage Current (Port 0)			±10	μA	0.45 < V_{IN} < V_{CC}
I_{TL}	Logical 1-to-0 Transition Current (Ports 1, 2, 3)			−650	μA	V_{IN} = 2V
RRST	RST Pulldown Resistor	50		300	KΩ	
C_{IO}	Pin Capacitance		10		pF	@ 1 MHz, 25°C
I_{CC}	Power Supply Current					(Note 5)
	Active Mode					
	87C51-L at 8 MHz			12	mA	
	All Others at 12 MHz(4)		11.5	20	mA	
	Idle Mode @ 12 MHz(4)		1.7	5	mA	
	Power Down Mode		5	50	μA	

NOTES:
1. "Typicals" are based on a limited number of samples taken from early manufacturing lots and are not guaranteed. The values listed are at room temp, 5V.
2. Capacitive loading on Ports 0 and 2 may cause noise pulses above 0.4V to be superimposed on the V_{OL}s of ALE and Ports 1, 2 and 3. The noise is due to external bus capacitance discharging into the Port 0 and Port 2 pins when these pins change from 1 to 0. In applications where capacitive loading exceeds 100 pF, the noise pulses on these signals may exceed 0.8V. It may be desirable to qualify ALE or other signals with a Schmitt Trigger, or CMOS-level input logic.
3. Capacitive loading on Ports 0 and 2 may cause the V_{OH} on ALE and $\overline{PSEN}$ to momentarily fall below the $0.9V_{CC}$ specification when the address bits are stabilizing.
4. I_{CC}MAX at other frequencies is given by:

$$\text{Active Mode: } I_{CC}MAX = 0.94 \times FREQ + 13.71$$

$$\text{Idle Mode: } I_{CC}MAX = 0.14 \times FREQ + 2.31$$

where FREQ is the external oscillator frequency in MHz. I_{CC}MAX is given in mA. See Figure 5.
5. See Figures 6 through 9 for I_{CC} test conditions. Minimum V_{CC} for Power Down is 2V.
6. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:

Maximum I_{OL} per port pin: 10 mA
Maximum I_{OL} per 8-bit port—
Port 0: 26 mA
Ports 1, 2, and 3: 15 mA
Maximum total I_{OL} for all output pins: 71 mA

If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification.
Pins are not guaranteed to sink greater than the listed test conditions.

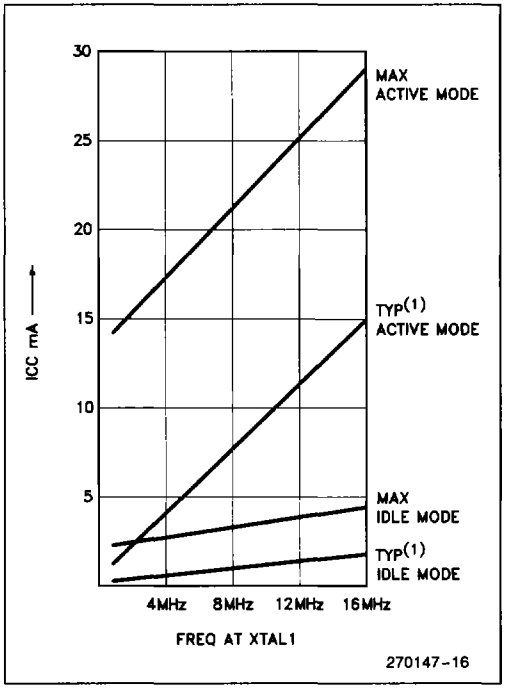


Figure 5. I_{CC} vs. FREQ. Valid only within frequency specifications of the device under test.

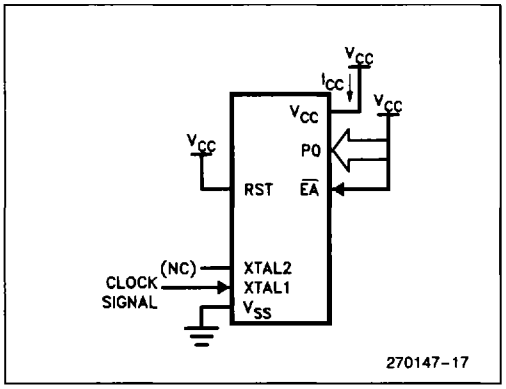


Figure 6. I_{CC} Test Condition, Active Mode. All other pins are disconnected.

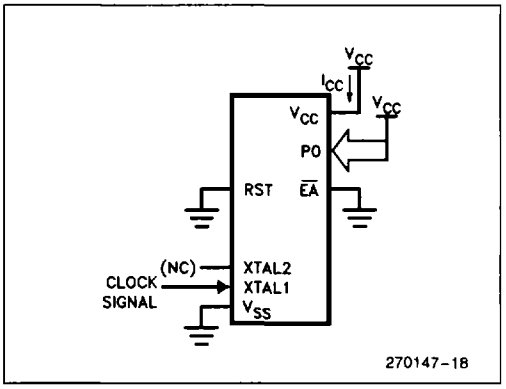


Figure 7. I_{CC} Test Condition, Idle Mode. All other pins are disconnected.

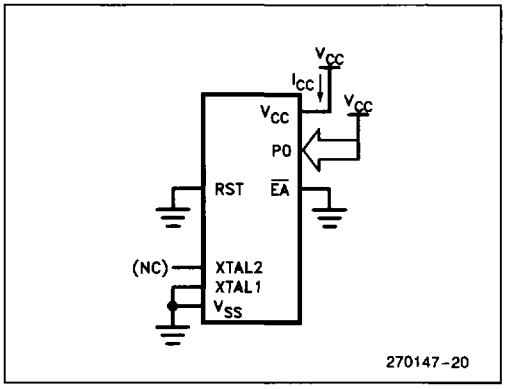


Figure 9. I_{CC} Test Condition, Power Down Mode. All other pins are disconnected. V_{CC} = 2V to 5.5V.

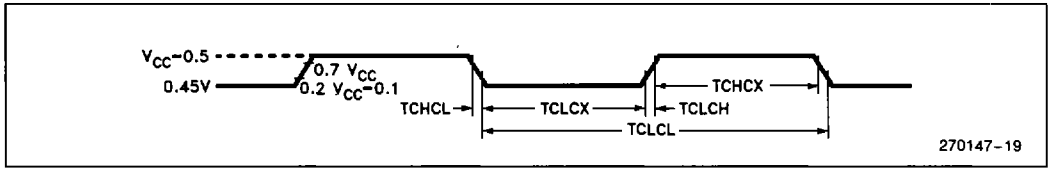


Figure 8. Clock Signal Waveform for I_{CC} tests in Active and Idle Modes. TCLCH = TCHCL = 5 ns.

EXPLANATION OF THE AC SYMBOLS

Each timing symbol has 5 characters. The first character is always a 'T' (stands for time). The other characters, depending on their positions, stand for the name of a signal or the logical status of that signal. The following is a list of all the characters and what they stand for.

A:Address.
C:Clock.
D:Input data.
H:Logic level HIGH.
I:Instruction (program memory contents).
L:Logic level LOW, or ALE.
P:$\overline{PSEN}$.
Q:Output data.
R:$\overline{RD}$ signal.
T:Time.
V:Valid.
W:$\overline{WR}$ signal.
X:No longer a valid logic level.
Z:Float.

For example,

TAVLL = Time from Address Valid to ALE Low.
TLLPL = Time from ALE Low to PSEN Low.

AC CHARACTERISTICS: (Over Operating Conditions; Load Capacitance for Port 0, ALE, and $\overline{PSEN}$ = 100 pF; Load Capacitance for All Other Outputs = 80 pF)

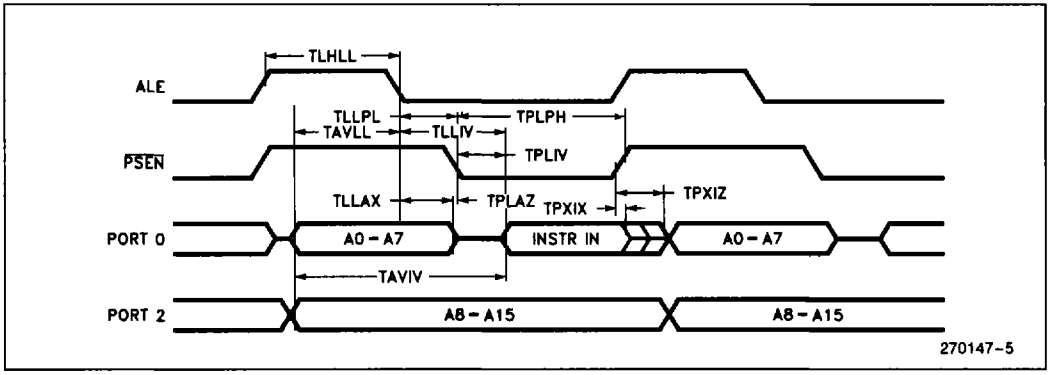
EXTERNAL MEMORY CHARACTERISTICS

Symbol	Parameter	12 MHz Oscillator		Variable Oscillator		Units
		Min	Max	Min	Max	
1/TCLCL	Oscillator Frequency 87C51/BH 87C51-1/BH-1 87C51-2/BH-2			 3.5 3.5 0.5	 12 16 12	MHz
TLHLL	ALE Pulse Width	127		2TCLCL−40		ns
TAVLL	Address Valid to ALE Low 87C51 80C51BH/C31BH	 43 28		 TCLCL−40 TCLCL−55		 ns ns
TLLAX	Address Hold After ALE Low 87C51 80C51BH/C31BH	 53 48		 TCLCL−30 TCLCL−35		 ns ns
TLLIV	ALE Low to Valid Instr In		234		4TCLCL−100	ns
TLLPL	ALE Low to $\overline{PSEN}$ Low 87C51 80C51BH/C31BH	 53 43		 TCLCL−30 TCLCL−40		 ns ns
TPLPH	$\overline{PSEN}$ Pulse Width	205		3TCLCL−45		ns
TPLIV	$\overline{PSEN}$ Low to Valid Instr In		145		3TCLCL−105	ns
TPXIX	Input Instr Hold After $\overline{PSEN}$	0		0		ns
TPXIZ	Input Instr Float After $\overline{PSEN}$		59		TCLCL−25	ns
TAVIV	Address to Valid Instr In		312		5TCLCL−105	ns
TPLAZ	$\overline{PSEN}$ Low to Address Float		10		10	ns
TRLRH	$\overline{RD}$ Pulse Width	400		6TCLCL−100		ns
TWLWH	$\overline{WR}$ Pulse Width	400		6TCLCL−100		ns
TRLDV	$\overline{RD}$ Low to Valid Data In		252		5TCLCL−165	ns
TRHDX	Data Hold After $\overline{RD}$	0		0		ns

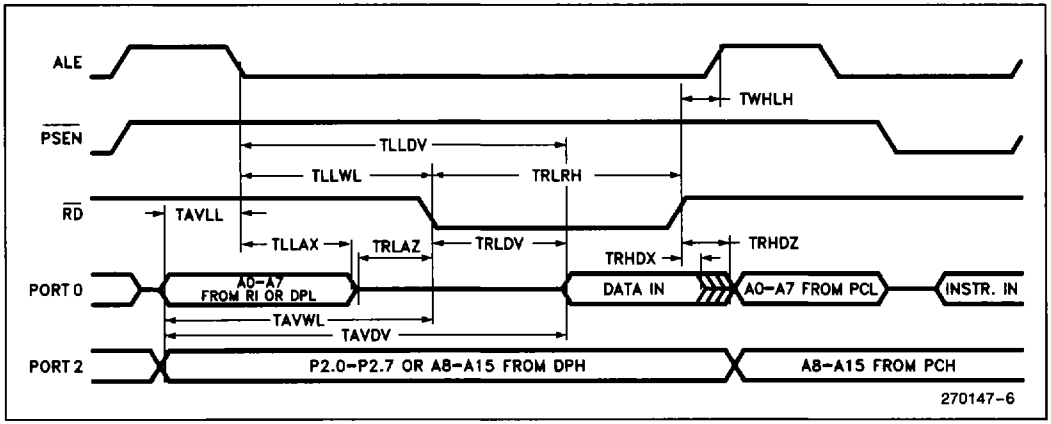
EXTERNAL MEMORY CHARACTERISTICS (Continued)

Symbol	Parameter	12 MHz Oscillator		Variable Oscillator		Units
		Min	Max	Min	Max	
TRHDZ	Data Float After $\overline{RD}$ 87C51 80C51BH/C31BH		 107 97		 2TCLCL−60 2TCLCL−70	 ns ns
TLLDV	ALE Low to Valid Data In		517		8TCLCL−150	ns
TAVDV	Address to Valid Data In		585		9TCLCL−165	ns
TLLWL	ALE Low to $\overline{RD}$ or $\overline{WR}$ Low	200	300	3TCLCL−50	3TCLCL+50	ns
TAVWL	Address to $\overline{RD}$ or $\overline{WR}$ Low	203		4TCLCL−130		ns
TQVWX	Data Valid to $\overline{WR}$ Transition 87C51 80C51BH/C31BH	 33 23		 TCLCL−50 TCLCL−60		 ns ns
TWHQX	Data Hold After $\overline{WR}$	33		TCLCL−50		ns
TRLAZ	$\overline{RD}$ Low to Address Float		0		0	ns
TWHLH	$\overline{RD}$ or $\overline{WR}$ High to ALE High	43	123	TCLCL−40	TCLCL+40	ns

EXTERNAL PROGRAM MEMORY READ CYCLE



EXTERNAL DATA MEMORY READ CYCLE



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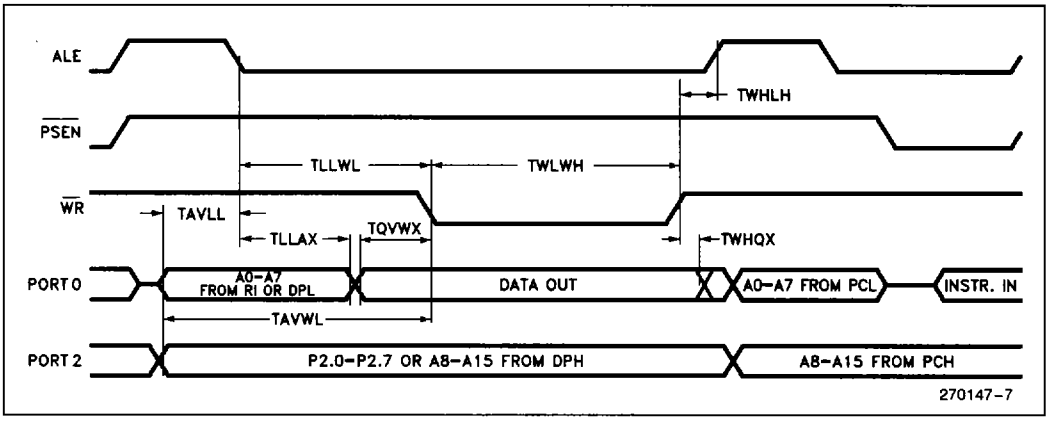
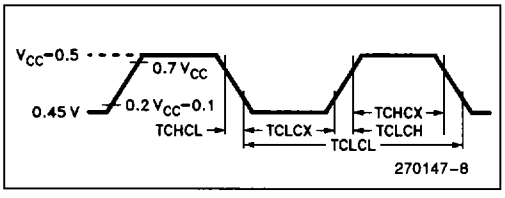
EXTERNAL DATA MEMORY WRITE CYCLE



EXTERNAL CLOCK DRIVE

Symbol	Parameter	Min	Max	Units
1/TCLCL	Oscillator Frequency			
	87C51/BH	3.5	12	MHz
	87C51-1/BH-1	3.5	16	
	87C51-2/BH-2	0.5	12	
TCHCX	High Time	20		ns
TCLCX	Low Time	20		ns
TCLCH	Rise Time		20	ns
TCHCL	Fall Time		20	ns

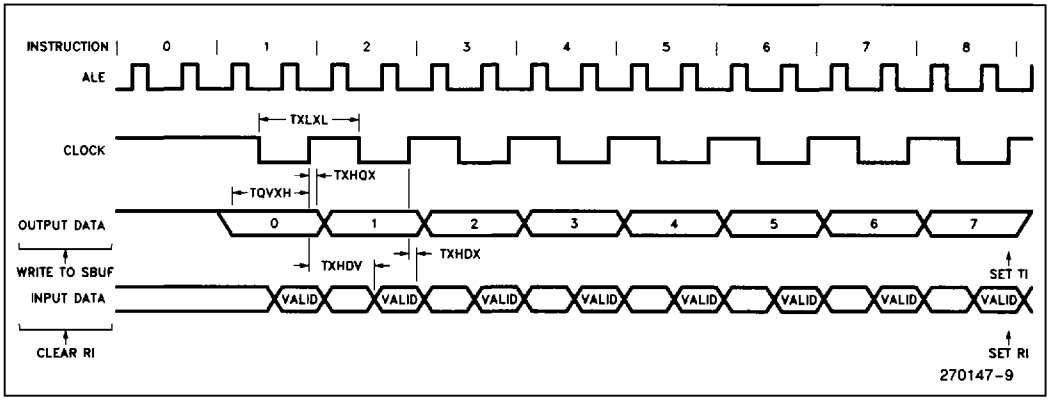
EXTERNAL CLOCK DRIVE WAVEFORM



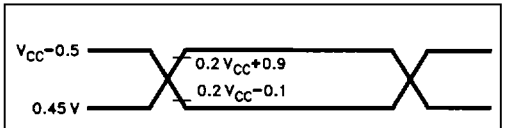
SERIAL PORT TIMING—SHIFT REGISTER MODE

Symbol	Parameter	12 MHz Oscillator		Variable Oscillator		Units
		Min	Max	Min	Max	
TXLXL	Serial Port Clock Cycle Time	1.0		12TCLCL		μs
TQVXH	Output Data Setup to Clock Rising Edge	700		10TCLCL − 133		ns
TXHQX	Output Data Hold After Clock Rising Edge	50		2TCLCL − 117		ns
TXHDX	Input Data Hold After Clock Rising Edge	0		0		ns
TXHDV	Clock Rising Edge to Input Data Valid		700		10TCLCL − 133	ns

SHIFT REGISTER MODE TIMING WAVEFORMS

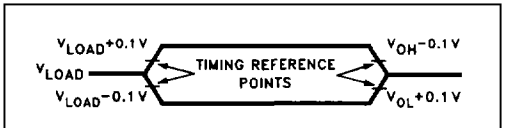


AC TESTING INPUT, OUTPUT WAVEFORMS



AC inputs during testing are driven at V_{CC} – 0.5 for a Logic "1" and 0.45V for a Logic "0." Timing measurements are made at V_{IH} min for a Logic "1" and V_{IL} max for a Logic "0".

FLOAT WAVEFORMS



For timing purposes a port pin is no longer floating when a 100 mV change from load voltage occurs, and begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs. I_{OL}/I_{OH} = ±20 mA. (-L, I_{OL}/I_{OH} = ±10 mA)

PROGRAMMING THE EPROM

The part must be running with a 4 MHz to 6 MHz oscillator. The address of an EPROM location to be programmed is applied to address lines while the code byte to be programmed in that location is applied to data lines. Control and program signals must be held at the levels indicated in Table 2. Normally $\overline{EA}/V_{PP}$ is held at logic high until just before ALE/$\overline{PROG}$ is to be pulsed. The $\overline{EA}/V_{PP}$ is raised to V_{PP}, ALE/$\overline{PROG}$ is pulsed low and then $\overline{EA}/V_{PP}$ is returned to a high (also refer to timing diagrams).

NOTE:

- Exceeding the V_{PP} maximum for any amount of time could damage the device permanently. The V_{PP} source must be well regulated and free of glitches.
- Programming specifications for the 87C51-L are the same as the standard 87C51.

DEFINITION OF TERMS

ADDRESS LINES: P1.0–P1.7, P2.0–P2.5, P3.4 respectively for A0–A14.

DATA LINES: P0.0–P0.7 for D0–D7.

CONTROL SIGNALS: RST, $\overline{PSEN}$, P2.6, P2.7, P3.6, P3.7.

PROGRAM SIGNALS: ALE/$\overline{PROG}$, $\overline{EA}/V_{PP}$.

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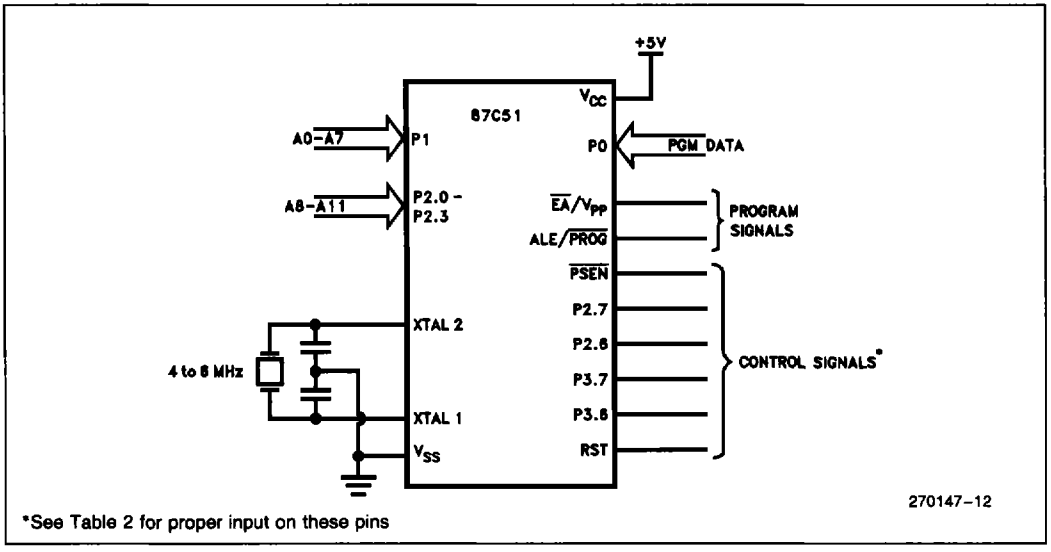
Table 2. EPROM Programming Modes

Mode		RST	$\overline{PSEN}$	ALE/$\overline{PROG}$	$\overline{EA}$/V_{PP}	P2.6	P2.7	P3.6	P3.7
Program Code Data		H	L	⎍	12.75V	L	H	H	H
Verify Code Data		H	L	H	H	L	L	H	H
Program Encryption Array Address 0–3F		H	L	⎍	12.75V	L	H	L	H
Program Lock Bits	Bit 1	H	L	⎍	12.75V	H	H	H	H
	Bit 2	H	L	⎍	12.75V	H	H	L	L
	Bit 3	H	L	⎍	12.75V	H	L	H	L
Read Signature Byte		H	L	H	H	L	L	L	L



*See Table 2 for proper input on these pins

Figure 10. Programming the EPROM

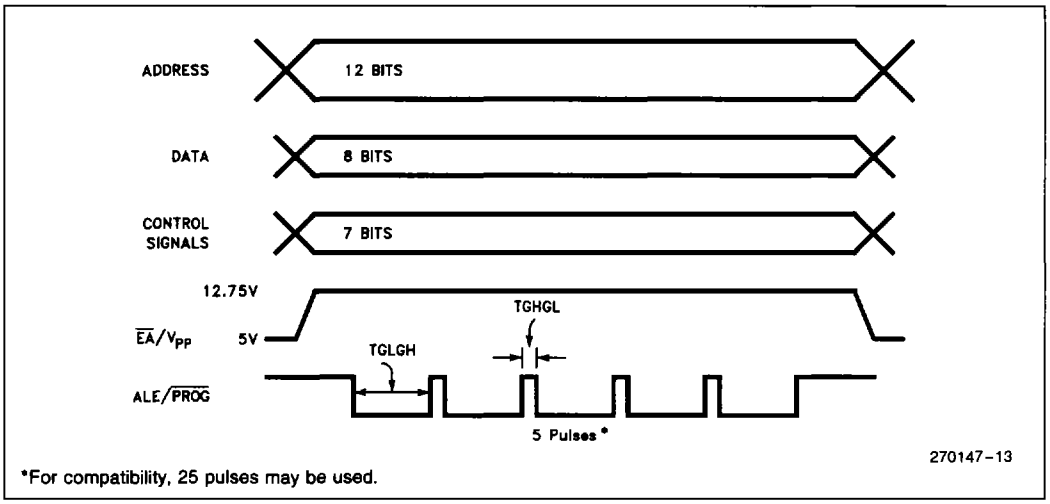


Figure 11. Programming Waveforms

PROGRAMMING ALGORITHM

Refer to Table 2 and Figures 10 and 11 for address, data, and control signals set up. To program the 87C51 the following sequence must be exercised.

1. Input the valid address on the address lines.
2. Input the appropriate data byte on the data lines.
3. Activate the correct combination of control signals.
4. Raise $\overline{EA}/V_{PP}$ from V_{CC} to 12.75V ±0.25V.
5. Pulse ALE/$\overline{PROG}$ 5 times* for the EPROM array, and 25 times for the encryption table and the lock bits.

Repeat 1 through 5 changing the address and data for the entire array or until the end of the object file is reached.

Program Verify

Verification may be done after programming either one byte or a block of bytes. In either case a complete verify of the array will ensure reliable programming of the 87C51.

The lock bits cannot be directly verified. Verification of the lock bits is done by observing that their features are enabled.

EPROM Lock System

The 87C51 program lock system, when programmed, protects the onboard program against software piracy.

The 87C51 has a 3-level program lock system and a 64-byte encryption array. Since this is an EPROM device, all locations are user-programmable. See Table 3.

Encryption Array

Within the EPROM array are 64 bytes of Encryption Array that are initially unprogrammed (all 1's). Every time that a byte is addressed during a verify, 6 address lines are used to select a byte of the Encryption Array. This byte is then exclusive-NOR'ed (XNOR) with the code byte, creating an Encryption Verify byte. The algorithm, with the array in the unprogrammed state (all 1's), will return the code in its original, unmodified form. For programming the Encryption Array, refer to Table 2 (Programming the EPROM).

When using the encryption array, one important factor needs to be considered. If a code byte has the value 0FFH, verifying the byte will produce the encryption byte value. If a large block (>64 bytes) of code is left unprogrammed, a verification routine will display the contents of the encryption array. For this reason all unused code bytes should be programmed with some value other than 0FFH, and not all of them the same value. This will ensure maximum program protection.

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Program Lock Bits

The 87C51 has 3 programmable lock bits that when programmed according to Table 3 will provide different levels of protection for the on-chip code and data.

Erasing the EPROM also erases the encryption array and the program lock bits, returning the part to full functionality.

Reading the Signature Bytes

The 87C51 has 3 signature bytes in locations 30H, 31H, and 60H. To read these bytes follow the procedure for EPROM verify, but activate the control lines provided in Table 2 for Read Signature Byte.

Location	Contents
	87C51
30H	89H
31H	58H
60H	51H

Erasure Characteristics (Windowed Devices Only)

Erasure of the EPROM begins to occur when the chip is exposed to light with wavelengths shorter than approximately 4,000 Angstroms. Since sunlight and fluorescent lighting have wavelengths in this range, exposure to these light sources over an extended time (about 1 week in sunlight, or 3 years in room level fluorescent lighting) could cause inadvertent erasure. If an application subjects the device to this type of exposure, it is suggested that an opaque label be placed over the window.

The recommended erasure procedure is exposure to ultraviolet light (at 2537 Angstroms) to an integrated dose of at least 15 W-sec/cm^2. Exposing the EPROM to an ultraviolet lamp of 12,000 μW/cm^2 rating for 30 minutes, at a distance of about 1 inch, should be sufficient.

Erasure leaves the array in an all 1's state.

Table 3. Program Lock Bits and the Features

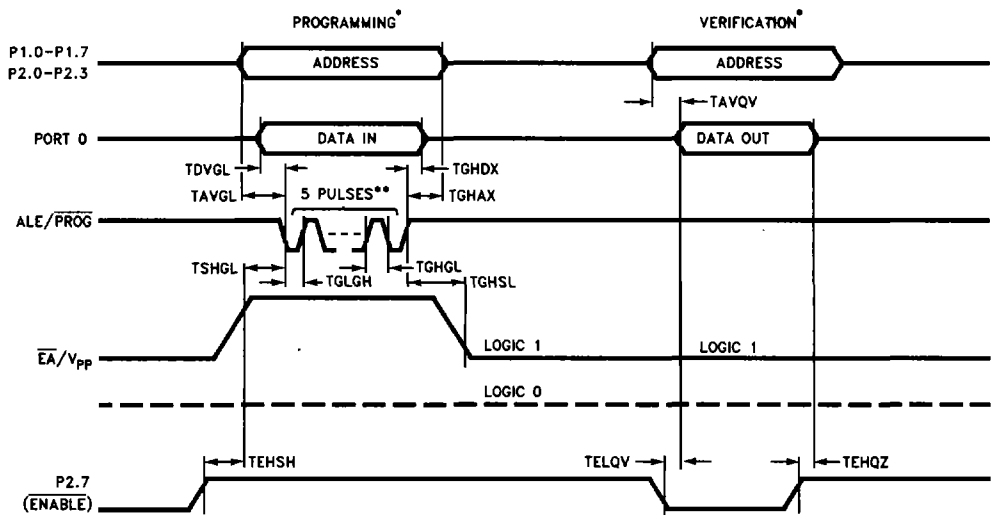
Program Lock Bits				Protection Type
	LB1	LB2	LB3	
1	U	U	U	No program lock features enabled. (Code verify will still be encrypted by the encryption array if programmed.)
2	P	U	U	MOVC instructions executed from external program memory are disabled from fetching code bytes from internal memory, EA is sampled and latched on reset, and further programming of the EPROM is disabled.
3	P	P	U	Same as 2, also verify is disabled.
4	P	P	P	Same as 3, also external execution is disabled.

EPROM PROGRAMMING AND VERIFICATION CHARACTERISTICS:

(T_A = 21°C to 27°C, V_{CC} = 5V ±10%, V_{SS} = 0V)

Symbol	Parameter	Min	Max	Units
V_{PP}	Programming Supply Voltage	12.5	13.0	V
I_{PP}	Programming Supply Current		75	mA
1/TCLCL	Oscillator Frequency	4	6	MHz
TAVGL	Address Setup to $\overline{PROG}$ Low	48TCLCL		
TGHAX	Address Hold After $\overline{PROG}$	48TCLCL		
TDVGL	Data Setup to $\overline{PROG}$ Low	48TCLCL		
TGHDX	Data Hold After $\overline{PROG}$	48TCLCL		
TEHSH	P2.7 ($\overline{ENABLE}$) High to V_{PP}	48TCLCL		
TSHGL	V_{PP} Setup to $\overline{PROG}$ Low	10		µs
TGHSL	V_{PP} Hold After $\overline{PROG}$	10		µs
TGLGH	$\overline{PROG}$ Width	90	110	µs
TAVQV	Address to Data Valid		48TCLCL	
TELQV	$\overline{ENABLE}$ Low to Data Valid		48TCLCL	
TEHQZ	Data Float After $\overline{ENABLE}$	0	48TCLCL	
TGHGL	$\overline{PROG}$ High to $\overline{PROG}$ Low	10		µs

EPROM PROGRAMMING AND VERIFICATION WAVEFORMS



*For programming conditions see Figure 10.
**5 pulses for the EPROM array, 25 pulses for the encryption table and lock bits.

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DATA SHEET REVISION HISTORY

This data sheet (271047-008) is valid for devices with an "A" at the end of the topside tracking number. Data sheets are changed as new device information becomes available. Verify with your local Intel sales office that you have the latest version before finalizing a design or ordering devices.

The following differences exist between this data sheet (271047-008) and the previous version (271047-007):

1. The 80C51BH/80C31BH CHMOS Single-Chip 8-Bit Microcomputer data sheet (270064-008) has been combined with the 87C51 CHMOS Single-Chip 8-Bit Microcontroller with 4 Kbytes of EPROM Program Memory data sheet (271047-001) to create this new data sheet.
2. 80C51BH/80C31BH specs have been added to the Package Table, DC Characteristics Table and AC Characteristics Table.
3. Added 3.3V device to data sheet.
4. EPROM Programming Information has been added.
5. The Operating Temperature Range has been changed to: 0°C to +70°C.

The following are the key differences between the -007 and the -006 versions of the 87C51 data sheet.

1. Pins labeled "NC" and "V_{SS1}" changed to "Reserved" in Figure 2.
2. θ_{ja} and θ_{jc} specifications added to "Packages" table.
3. V_{SS1} pin description deleted.
4. Capacitor values for ceramic resonators deleted from Figure 3.
5. Second paragraph added to "Encrypted Verify" under "Program Memory Lock" section.
6. All pin numbers and the P3.3 control line deleted from Figure 10.

The following differences exist between the -006 and the -005 versions of the 87C51 data sheet:

1. Technology changed from CHMOS II-E to CHMOS III-E.
2. QFP package offering added.
3. Asynchronous Reset added.
4. ALE disable added.
5. Program Memory Lock feature changes:
   - — Third lock bit added
   - — Encryption array enhanced to 64 bytes
6. Data sheet status notice and Absolute Maximum Ratings warning revised.
7. DC Characteristics changes:
   - — Additional V_{OL} entries added (0.3V @ I_{OL} = 100 μA, 1.0V @ I_{OL} = 3.5 mA).
   - — Additional V_{OL1} entries added (0.3V @ I_{OL} = 200 μA, 1.0V @ I_{OL} = 7.0 mA).
   - — V_{OH} entries changed from 2.4V @ I_{OH} = −60 μA, 0.75 V_{CC} @ I_{OH} = −25 μA, and 0.9 V_{CC} @ I_{OH} = −10 μA to the current values.
   - — V_{OH1} entries changed from 2.4V @ I_{OH} = −800 μA, 0.75 V_{CC} @ I_{OH} = −300 μA, and 0.9 V_{CC} @ I_{OH} = −80 μA to the current values.
   - — RRST changed from 50 KΩ min and 300 KΩ max to the current values.
   - — C_{IO} changed from 10 pF max to 10 pF typical
8. Note 2 reworded (ALE noise pulses).
9. Note 4 deleted (transition current sourcing).

DATA SHEET REVISION HISTORY (Continued)

10. AC Timings improved for:
    TAVLL changed from TCLCL−55 to TCLCL−40
    TLLAX changed from TCLCL−35 to TCLCL−30
    TLLPL changed from TCLCL−40 to TCLCL−30
    TRHDZ changed from 2 TCLCL−70 to 2 TCLCL−60
    TQVWX changed from TCLCL−60 to TCLCL−50
11. EPROM programming control line (P3.3) added to Figure 10.
12. Programming Algorithm paragraph reworded to describe programming changes.
13. Figure 11 changed to show 5 programming pulses rather than 25.
14. Figure 12 deleted (Program Verification).
15. Program Verification paragraph reworded.
16. Third signature byte added; location and definition included.
17. Program/Verify Algorithms paragraph deleted.
18. I_{PP} programming spec changed from 50 mA to 75 mA.

The following are the key differences between -005 and the -004 versions of the 87C51 data sheet:

1. Package table was added.
2. Note 7 on maximum current specifications added to DC Characteristics.
3. Data Sheet Revision Summary was added.