PCI Bridges

21152 Transparent PCI-to-PCI Bridge

The 21152AB transparent PCI-to-PCI Bridges is Not Recommended for new designs. For 33 MHz applications use the S21152BB.

The 21152 is designed for compliance with *PCI Local Bus Specification*, Revision 2.2. The 21152 is pin-to-pin compatible with the 21052 bridge, which is designed for compliance with *PCI Local Bus Specification*, Revision 2.0.

The 21152 provides full support for delayed transactions, which enables the buffering of memory read, I/O, and configuration transactions. The 21152 has separate posted write, read data, and delayed transaction queues with significantly more buffering capability than first-generation bridges. In addition, the 21152 supports buffering of simultaneous multiple posted write and delayed transactions in both directions. Among the features provided by the 21152 are: a programmable 2-level secondary bus arbiter, individual secondary clock software control, and enhanced address decoding. The 21152 has sufficient clock and arbitration pins to support four PCI bus master devices directly on its secondary interface.

The 21152 allows the two PCI buses to operate concurrently. This means that a master and a target on the same PCI bus can communicate while the other PCI bus is busy. This traffic isolation may increase system performance in applications such as multimedia.

Features

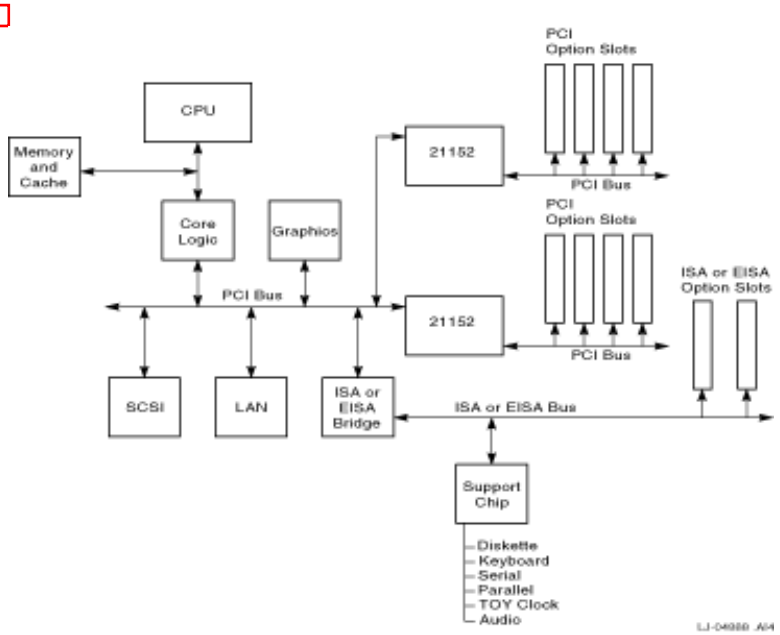
- Designed for compliance with *PCI Local Bus Specification*, Revision 2.2
- Implements delayed transactions for all PCI configuration, I/O, and memory read commands up to three transactions simultaneously in each direction
- Allows 88 bytes of buffering (data and address) for posted memory write commands in each direction up to five posted write transactions simultaneously in each direction
- Allows 72 bytes of read data buffering in each direction
- Provides concurrent primary and secondary bus operation to isolate traffic
- Provides five secondary clock outputs:
  - Low skew, permitting direct drive of option slots
  - Individual clock control through configuration space
- Provides arbitration support for four secondary bus devices:
  - A programmable 2-level arbiter
  - Hardware disable control, permitting use of an external arbiter
- Provides enhanced address decoding:
  - A 32-bit I/O address range
  - A 32-bit memory-mapped I/O address range
  - A 64-bit prefetchable memory address range
  - ISA-aware mode for legacy support in the first 64 KB of I/O address range
  - VGA addressing and VGA palette snooping support
- Supports PCI transaction forwarding for the following commands:
  - All I/O and memory commands
  - Type 1 to Type 1 configuration commands
  - Type 1 to Type 0 configuration commands (downstream only)
  - All Type 1 to special cycle configuration command
- Includes downstream lock support

- Supports both 5 V and 3.3 V signaling environments

21152 Applications

The 21152 makes it possible to extend a system's load capability limit beyond that of a single PCI bus by allowing motherboard designers to add more PCI devices, or more PCI option card slots, than a single PCI bus can support. Figure 1 illustrates the use of two 21152 PCI-to-PCI bridges on a system board. Each 21152 that is added to the board creates a new PCI bus that provides support for the additional PCI slots or devices.

Figure 1. 21152 on the System Board



Option card designers can use the 21152 to implement multiple-device PCI option cards. Without a PCI-to-PCI bridge, PCI loading rules would limit option cards to one device. The PCI Local Bus Specification loading rules limit PCI option cards to a single connection per PCI signal in the option card connector. However, the 21152 overcomes this restriction by providing, on the option card, an independent PCI bus to which up to four devices can be attached. Figure 2 shows how the 21152 enables the design of a multi-component option card.

Figure 2. 21152 with Option Cards

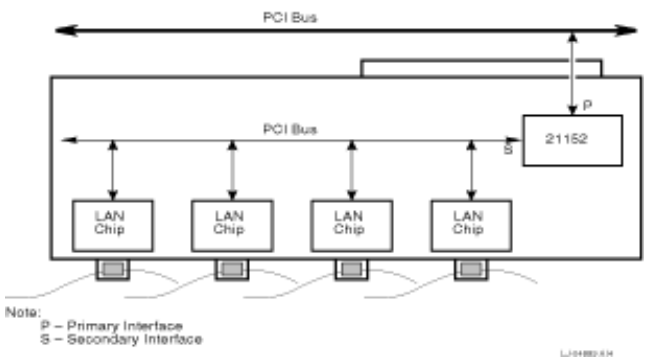


Figure 3. 21152 Characteristics Table

21152 Characteristics Table	
Characteristic	**Specification**
Power Supply	VDD = 3.3 V vdd_clamp = 5 V or 3.3 V
Operating Temperature	Tj Maximum = 125°C
Storage Temperature Range	55°C Minimum, 125°C Maximum

Power Dissipation (Typical)	1.2 W Maximum @ VDD = 3.3 V with PCI Clock = 33 MHz
Package	160-Pin PQFP

Ordering Information

Product	Order Number
PCI-to-PCI Bridge	21152-AB

To Order Now:

- Contact an Intel authorized distributor

back to top

Product Change Notification

1244-01

Change Notification #: 1244-01
Change Title: 21152AB PCI-to-PCI Bridge and 21A5203 Evaluation Board, PCN 1244-01, Product Conversion
Date of PCN Publication: October 19, 2001

Type of Change Notification: Form-Fit-Function

Key Characteristics of the Change: Design, Order Code

Forecasted Key Milestones:

Date of Sample Availability — October 19, 2001
Date of Qualification Data Availability — October 19, 2001
Date Customer must be ready to receive post-conversion material — January 19, 2002
This is determined by the projected depletion of inventory at the time of the PCN publication. The depletion of inventory may be impacted by fluctuating supply and demand, therefore, although customers should be prepared to receive the post-converted materials on this date, Intel will continue to ship and customers may continue to receive the pre-converted materials until the inventory has been depleted.
Date of first availability of post-conversion material — October 19, 2001
The date of "First Availability of post-conversion material" is the earliest date that customers may request to receive post-conversion material.

Reason for Revision:

Revision #1 announces the conversion of the 21152AB to the S21152BB and the 21A5203 Evaluation Board to the 21A5205, replacing the 21152AB product discontinuance.

Revision #0 announced the discontinuance of the 21152AB and the 21A5203 Evaluation board.

Description of Change to the Customer from Original PCN:

Intel will be converting the 21152AB PCI-to-PCI Bridge to the S21152BB. Intel will also be converting the 21A5203 Evaluation Board to 21A5205. The S21152BB is backward compatible with the 21152AB and can be used in any 21152AB application. Order codes for the new material are listed in the Component Products Table that follows. This product will be converted and unavailable for additional orders after January 19, 2002. All outstanding orders for the 21152AB and 21A5203 will be converted to S21152BB and 21A5205 at that time.

Revised Customer Impact of Change and Recommended Action:

Any customer using the 21152AB and/or 21A5203 Evaluation board in existing designs must convert to the S21152BB and/or 21A5205 by the indicated milestones for this product. The product code will change from 21152AB to S21152BB and from 21A5203 to 21A5205. Orders for the 21152AB and 21A5203 will be converted to the S21152BB and 21A5205 upon depletion of the current 21152AB and 21A5203 inventory.

The S21152BB design is pin-to-pin compatible with the 21152AB design. The S21152BB is an ASIC design using an Intel 0.35 micron CMOS process and its associated cell library. The S21152BB has a lead form profile change from the 21152AB and errata fix. These and other differences between the S21152BB and the 21152AB are fully defined in the "21152AB and

S21152BB Differences Application Note" located on http://developer.intel.com/design/bridge/applnots. It is recommended that customers perform their standard validation testing on the S21152BB.

Component Products Table

Affected Product Code	Pre-conversion S-Spec / MM#	New Product Code	Post-conversion S-Spec / MM#
21152AB	**821298**	**S21152BB**	**837092**
21A5203	**821765**	**21A5205**	**833673**

Reference Documents / Attachments:

21152AB and S21152BB Differences Application Note (278329-002).
http://developer.intel.com/design/bridge/applnots/278329.htm

PCN Revision History:

Date of Revision:	Revision Number:	Reason:
October 1, 2001	00	Initial release
October 19, 2001	01	Product conversion replacing product discontinuance