

M27512

512K (64K x 8) UV ERASABLE PROM

Military

- **Software Carrier Capability**
- **Fast Access Time**
 - M27512-20 200 ns
 - M27512-25 250 ns
 - M27512-35 350 ns
- **Two-Line Control**
- **Intelligent Identifier™ Mode**
 - Automated Programming Operations
- **TTL Compatible**
- **Industry Standard Pinout ... JEDEC Approved**
- **Low Power**
 - 150 mA max. Active
 - 40 mA max. Standby
- **Intelligent Programming™ Algorithm**
 - Fastest EPROM Programming
- **Military Temperature Range:**
 - 55°C to +125°C (T_C)

The Intel M27512 is a 5V only, 524, 288 bit ultraviolet Erasable and Electrically Programmable Read Only Memory (EPROM). Organized as 64K words by 8 bits, individual bytes are accessed in under 200 ns. This ensures compatibility with high performance microprocessors, such as the Intel 8 MHz M80186, allowing full speed operation without the addition of performance-degrading WAIT states. The M27512 is also directly compatible with Intel's M8051 family of microcontrollers.

The M27512 enables implementation of new, advanced systems with firmware intensive architectures. The combination of the M27512's high density, cost effective EPROM storage, and new advanced microprocessors having megabyte addressing capability provides designers with opportunities to engineer user friendly, high reliability, high-performance systems.

The M27512's large storage capability of 64K bytes enables it to function as a high density software carrier. Entire operating systems, diagnostics, high-level language programs and specialized application software can reside in a M27512 EPROM directly on a system's memory bus. This permits immediate microprocessor access and execution of software and eliminates the need for time consuming disk accesses and downloads.

Two advanced features have been designed into the M27512 that allow for fast and reliable programming—the intelligent identifier™ mode and the intelligent Programming™ Algorithm. Programming equipment that takes advantage of these innovations will electronically identify the M27512 and then rapidly program it using an efficient programming method.

Two-line control and JEDEC-approved, 28-pin packaging are standard features of all Intel high-density EPROMs. This assures easy microprocessor interfacing and minimum design efforts when upgrading, adding, or choosing between nonvolatile memory alternatives.

The M27512 is manufactured using Intel's advanced HMOS* II-E technology.

*HMOS is a patented process of Intel Corporation.

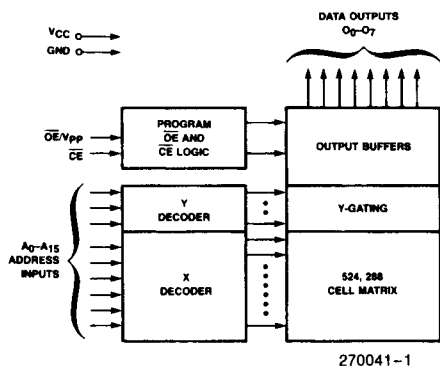
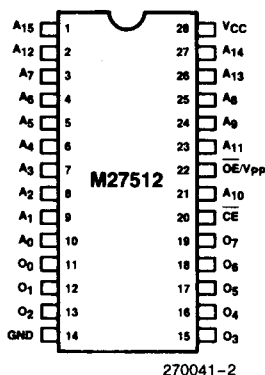


Figure 1. Block Diagram



Pin Names

A ₀ -A ₁₅	Addresses
CE	Chip Enable
OE/V _{pp}	Output Enable/V _{pp}
O ₀ -O ₇	Outputs

Figure 2. Pin Configuration

ABSOLUTE MAXIMUM RATINGS*

Case Temperature Under Bias . . . -55°C to +125°C

Storage Temperature -65°C to +150°C

All Input or Output Voltages with

Respect to Ground +6.5V to -0.6V

Voltage on Pin 24 with

Respect to Ground +13.5V to -0.6V

 \overline{OE}/V_{PP} Supply Voltage with

Respect to Ground +14.0V to -0.6V

*Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

NOTICE: Specifications contained within the following tables are subject to change.

Operating Conditions

Symbol	Parameter	Min	Max	Units
T_C	Case Temperature (Instant On)	-55	+125	°C
V_{CC}	Digital Supply Voltage	4.50	5.50	V

READ OPERATION**D.C. CHARACTERISTICS** (Over Specified Operating Conditions)

Symbol	Parameter	Limits			Units	Comments
		Min	Typ(2)	Max		
I_{LI}	Input Load Current			10	μA	$V_{IN} = 5.5V$
I_{LO}	Output Leakage Current			10	μA	$V_{OUT} = 5.5V$
I_{CC1}	V_{CC} Current Standby		20	40	mA	$\overline{CE} = V_{IH}$
I_{CC2}	V_{CC} Current Active		90	150	mA	$\overline{CE} = \overline{OE}/V_{PP} = V_{IL}$
V_{IL}	Input Low Voltage	-0.1		+0.8	V	
V_{IH}	Input High Voltage	2.0		$V_{CC} + 1$	V	
V_{OL}	Output Low Voltage			0.45	V	$I_{OL} = 2.1 \text{ mA}$
V_{OH}	Output High Voltage	2.4			V	$I_{OH} = -400 \mu A$

A.C. CHARACTERISTICS (Over Specified Operating Conditions)

Symbol	Parameter	M27512-20		M27512-25		M27512-35		Units	Comments
		Min	Max	Min	Max	Min	Max		
t_{ACC}	Address to Output Delay		200		250		350	ns	$\overline{CE} = \overline{OE}/V_{PP} = V_{IL}$
t_{CE}	\overline{CE} to Output Delay		200		250		350	ns	$\overline{OE}/V_{PP} = V_{IL}$
t_{OE}	\overline{OE}/V_{PP} High to Output Delay		75		100		120	ns	$\overline{CE} = V_{IL}$
$t_{DF}^{(3)}$	\overline{OE}/V_{PP} High to Output Float	0	55	0	60	0	105	ns	$\overline{CE} = V_{IL}$
$t_{OH}^{(3)}$	Output Hold from Addresses \overline{CE} or \overline{OE} Whichever Occurred First	0		0		0		ns	$\overline{CE} = \overline{OE}/V_{PP} = V_{IL}$

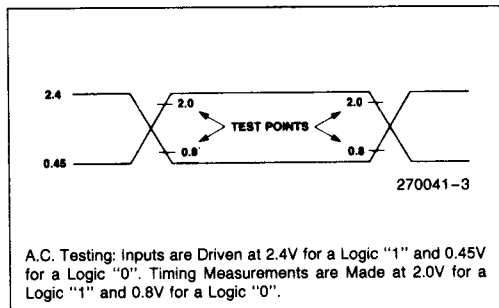
NOTES:

- V_{CC} must be applied simultaneously or before \overline{OE}/V_{PP} and removed simultaneously or after \overline{OE}/V_{PP} .
- Typical values are for $T_C = 25^\circ C$ and nominal supply voltages.
- Output Float is defined as the point where data is no longer driven—see timing diagram.

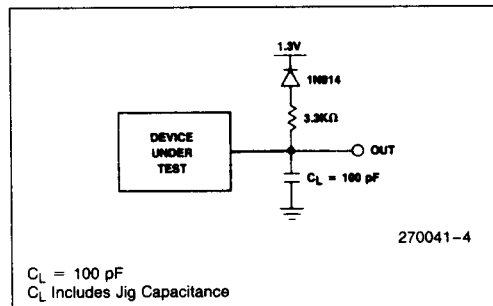
CAPACITANCE $T_C = 25^\circ\text{C}$, $f = 1.0\text{ MHz}$

Symbol	Parameter	Typ ⁽¹⁾	Max	Units	Conditions
C_{IN1}	Input Capacitance Except \overline{OE}/V_{PP}	4	6	pF	$V_{IN} = 0V$
C_{OUT}	Output Capacitance	8	12	pF	$V_{OUT} = 0V$
C_{IN2}	\overline{OE}/V_{PP} Input Capacitance	8	20	pF	$V_{OUT} = 0V$

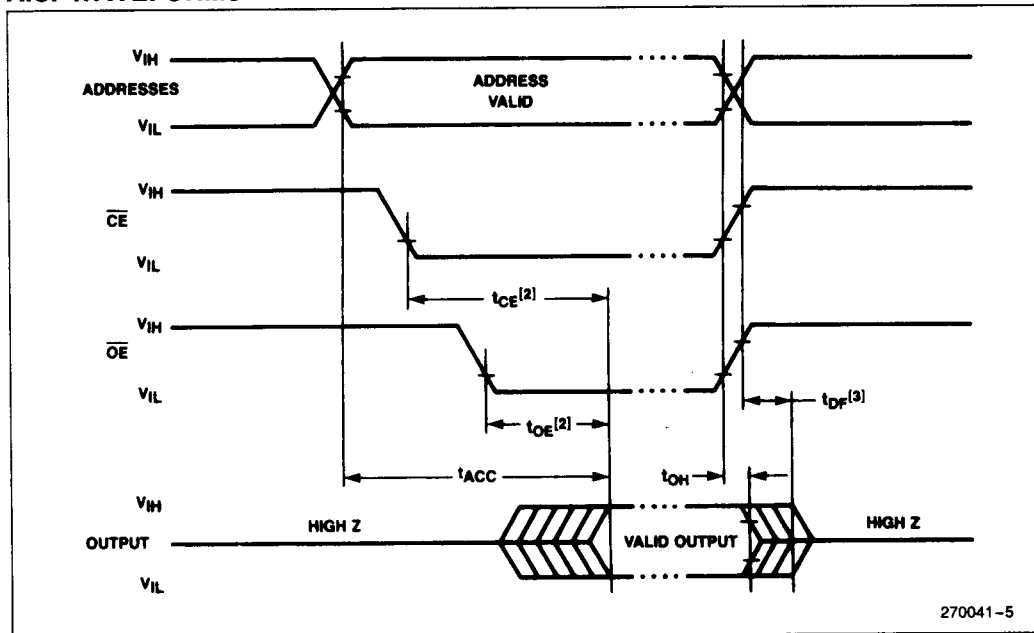
A.C. TESTING INPUT/OUTPUT WAVEFORM



A.C. TESTING LOAD CIRCUIT



A.C. WAVEFORMS



NOTES:

1. Typical values are for $T_C = 25^\circ\text{C}$ and nominal supply voltages.
2. \overline{OE}/V_{PP} may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of \overline{CE} without impact on t_{ACC} .
3. Output float is defined as the point where data is no longer driven.

DEVICE OPERATION

The six modes of operation of the M27512 are listed in Table 1. A single 5V power supply is required in the read mode. All inputs are TTL levels except for \overline{OE}/V_{PP} and 12V on A₉ for intelligent identifier mode.

Table 1. Operating Modes

Mode	Pins \overline{CE} (20)	\overline{OE}/V_{PP} (22)	A ₉ (24)	V _{CC} (28)	Outputs (11–13, 15–19)
Read	V _{IL}	V _{IL}	X	V _{CC}	D _{OUT}
Output Disable	V _{IL}	V _{IH}	X	V _{CC}	High Z
Standby	V _{IH}	X	X	V _{CC}	High Z
intelligent Programming	V _{IL}	V _{PP}	X	V _{CC}	D _{IN}
Verify	V _{IH}	V _{IL}	X	V _{CC}	D _{OUT}
Program Inhibit	V _{IH}	V _{PP}	X	V _{CC}	High Z
intelligent Identifier	V _{IL}	V _{IL}	V _H	V _{CC}	Code

NOTES:

1. X can be V_{IH} or V_{IL}
2. V_H = 12.0V ± 0.5V

READ MODE

The M27512 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable (\overline{CE}) is the power control and should be used for device selection. Output Enable (\overline{OE}/V_{PP}) is the output control and should be used to gate data from the output pins, independent of device selection. Assuming that addresses are stable, the address access time (t_{ACC}) is equal to the delay from \overline{CE} to output (t_{CE}). Data is available at the outputs after a delay of t_{OE} from the falling edge of \overline{OE} , assuming that \overline{CE} has been low and addresses have been stable for at least t_{ACC}–t_{OE}.

STANDBY MODE

The M27512 has a standby mode which reduces the maximum active current from 150 mA to 40 mA. The M27512 is placed in the standby mode by applying a TTL-high signal to the \overline{CE} input. When in standby mode, the outputs are in a high impedance state, independent of the \overline{OE}/V_{PP} input.

Two Line Output Control

Because EPROMs are usually used in larger memory arrays, Intel has provided 2 control lines which accommodate this multiple memory connection. The two control lines allow for:

- a) the lowest possible memory power dissipation, and
- b) complete assurance that output bus contention will not occur.

To use these two control lines most efficiently, \overline{CE} (pin 20) should be decoded and used as the primary device selecting function, while \overline{OE}/V_{PP} (pin 22) should be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low power standby mode and that the output pins are active only when data is desired from a particular memory device.

System Considerations

The power switching characteristics of HMOS II-EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer—the standby current level, the active current level, and the transient current peaks that are produced by the falling and rising edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitive and inductive loading of the device. The associated transient voltage peaks can be suppressed by complying with Intel's Two-Line Control and by properly selected decoupling capacitors. It is recommended that a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance and should be placed as close to the device as possible. In addition, a 4.7 μF bulk electrolytic capacitor should be used between V_{CC} and GND for every eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage droop caused by the inductive effects of PC board traces. This inductive effect should be further minimized through special layout considerations such as larger traces and gridding (refer to High Speed Memory System Design Using the 2147H, AP-74). In particular, the V_{SS} (Ground) plane should be stable as possible.

PROGRAMMING

Caution: Exceeding 14.0V on pin 22 (\overline{OE}/V_{PP}) will permanently damage the M27512.

Initially, and after each erasure, all bits of the M27512 are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" can be present in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The M27512 is in the programming mode when the \overline{OE}/V_{PP} input is at 12.5V and \overline{CE} is at TTL-low. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

intelligent Programming™ Algorithm

The M27512 intelligent Programming Algorithm rapidly programs Intel M27512 EPROMs using an efficient and reliable method particularly suited to the production programming environment. Typical programming times for individual devices are on the order of six minutes. Actual programming times may vary due to differences in programming equipment. Programming reliability is also ensured as the incremental program margin of each byte is continually monitored to determine when it has been successfully programmed. A flowchart of the M27512 intelligent Programming Algorithm is shown in Figure 3.

The intelligent Programming Algorithm utilizes two different pulse types: initial and overprogram. The duration of the initial \overline{CE} pulse(s) is one millisecond, which will then be followed by a longer overprogram pulse of length $3X$ msec. X is an iteration counter and is equal to the number of the initial one millisecond pulses applied to a particular M27512 location, before a correct verify occurs. Up to 25 one-millisecond pulses per byte are provided for before the overprogram pulse is applied. **The entire sequence of program pulses and byte verifications is performed at $V_{CC} = 6.0V$ and $\overline{OE}/V_{PP} = 12.5V$.** When the intelligent Programming cycle has been completed, all bytes should be compared to the original data with $V_{CC} = 5.0V$.

Program Inhibit

Programming of multiple M27512s in parallel with different data is easily accomplished by using the Program Inhibit mode. A high-level \overline{CE} input inhibits the other M27512s from being programmed.

Except for \overline{CE} and \overline{OE}/V_{PP} all inputs of the parallel M27512s may be common. A TTL low-level pulse applied to the \overline{CE} input with \overline{OE}/V_{PP} at 12.5V will program the selected M27512.

Verify

A verify (read) should be performed on the programmed bits to determine that they have been correctly programmed. The verify is performed with \overline{OE}/V_{PP} and \overline{CE} at V_{IL} . Data should be verified t_{DV} after the falling edge of \overline{CE} .

intelligent Identifier™ Mode

The intelligent Identifier Mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional in the $25^{\circ}C \pm 5^{\circ}C$ ambient temperature range that is required when programming the M27512.

To activate this mode, the programming equipment must force 11.5V to 12.5V on address line A9 (pin 24) of the M27512. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 (pin 10) from V_{IL} to V_{IH} . All other address lines must be held at V_{IL} during intelligent Identifier Mode, except for A14 and A15 which should be held high.

Byte 0 ($A0 = V_{IL}$) represents the manufacturer code and byte 1 ($A0 = V_{IH}$) the device identifier code. For the Intel M27512, these two identifier bytes are given in Table 2. All identifiers for manufacturer and device codes will possess odd parity, with the MSB (07) defined as the parity bit.

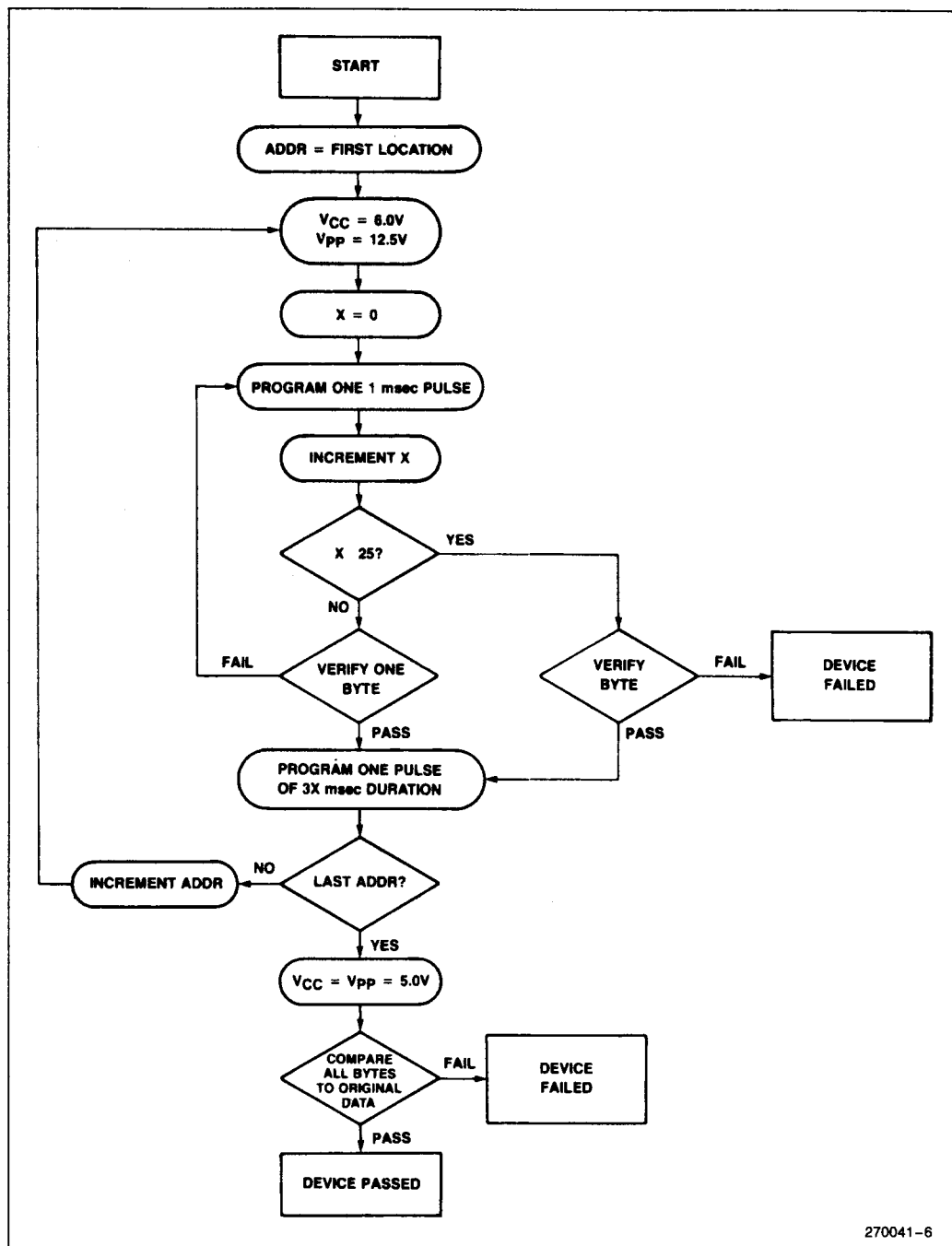
Table 2. M27512 intelligent Identifier™ Bytes

Identifier	Pins	A ₀ (10)	O ₇ (19)	O ₆ (18)	O ₅ (17)	O ₄ (16)	O ₃ (15)	O ₂ (13)	O ₁ (12)	O ₀ (11)	Hex Data
Manufacturer Code		V_{IL}	1	0	0	0	1	0	0	1	89
Device Code		V_{IH}	0	0	0	0	1	1	0	1	0D

NOTES:

1. $A_9 = 12.0V \times 0.5V$

2. $A_1-A_8, A_{10}-A_{13}, \overline{CE}, \overline{OE}/V_{PP} = V_{IL}$ $A_{14}, A_{15} = V_{IH}$



270041-6

Figure 3. M27512 Intelligent Programming™ Flowchart

ERASURE CHARACTERISTICS

The erasure characteristics of the M27512 are such that erasure begins to occur upon exposure to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000–4000 Å range. Data shows that constant exposure to room level fluorescent lighting could erase the typical M27512 in approximately 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the M27512 is to be exposed to these types of lighting conditions for extended periods of time, opaque labels should be placed over the M27512 window to prevent unintentional erasure.

The recommended erasure procedure for the M27512 is exposure to shortwave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity \times exposure time) for erasure should be a minimum of 15 Wsec/cm². The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with a 1200 μ W/cm² power rating. The M27512 should be placed within 1 inch of the lamp tubes during erasure. The maximum integrated dose a M27512 can be exposed to without damage is 7258 Wsec/cm² (1 week @ 12000 μ W/cm²). Exposure of the M27512 to high intensity UV light for long periods may cause permanent damage.

intelligent Programming™ Algorithm

D.C. PROGRAMMING CHARACTERISTICS

$T_C = 25 \pm 5^\circ\text{C}$, $V_{CC} = 6.0\text{V} \pm 0.25\text{V}$, $\overline{OE}/V_{PP} = 12.5\text{V} \pm 0.5\text{V}$

Symbol	Parameter	Limits		Units	Comments (Note 1)
		Min	Max		
I_{LI}	Input Current (All Inputs)		10	μA	$V_{IN} = V_{IL} \text{ or } V_{IH}$
V_{IL}	Input Low Level (All Inputs)	−0.1	0.8	V	
V_{IH}	Input High Level	2.0	$V_{CC} + 1$	V	
V_{OL}	Output Low Voltage During Verify		0.45	V	$I_{OL} = 2.1 \text{ mA}$
V_{OH}	Output High Voltage During Verify	2.4		V	$I_{OH} = -400 \mu\text{A}$
I_{CC2}	V_{CC} Supply Current		150	mA	
I_{PP2}	V_{PP} Supply Current (Program)		50	mA	$\overline{OE} = V_{IL}$
V_{ID}	A_9 intelligent Identifier Voltage	11.5	12.5	V	

NOTE:

1. V_{CC} must be applied simultaneously or before \overline{OE}/V_{PP} and removed simultaneously or after \overline{OE}/V_{PP} .

A.C. PROGRAMMING CHARACTERISTICS
 $T_C = 25 \pm 5^\circ\text{C}$, $V_{CC} = 6.0\text{V} \pm 0.25\text{V}$, $V_{PP} = 12.5\text{V} \pm 0.5\text{V}$

Symbol	Parameter	Limits			Units
		Min	Typ	Max	
t_{AS}	Address Setup Time	2			μs
t_{OES}	\overline{OE}/V_{PP} Setup Time	2			μs
$t_{OE H}$	\overline{OE}/V_{PP} Hold Time	2			μs
t_{DS}	Data Setup Time	2			μs
t_{AH}	Address Hold Time	0			μs
t_{DH}	Data Hold Time	2			μs
$t_{DFP}^{(4)}$	Output Enable to Output Float Delay	0		130	ns
t_{VCS}	V_{CC} Setup Time	2			μs
$t_{PW}^{(3)}$	\overline{CE} Initial Program Pulse Width	0.95	1.0	1.05	ms
$t_{OPW}^{(2)}$	\overline{CE} Overprogram Pulse Width	2.85		78.75	ms
t_{DV}	Data Valid from \overline{CE}			1	μs
t_{VR}	\overline{OE}/V_{PP} Recovery Time	2			μs
t_{PRT}	\overline{OE}/V_{PP} Pulse Rise Time During Programming	50			ns

***A.C. CONDITIONS OF TEST**

Input Rise and Fall Times (10% to 90%) 20 ns

Input Pulse Levels 0.45V to 2.4V

Input Timing Reference Level 0.8V and 2.0V

Output Timing Reference Level 0.8V and 2.0V

NOTES:

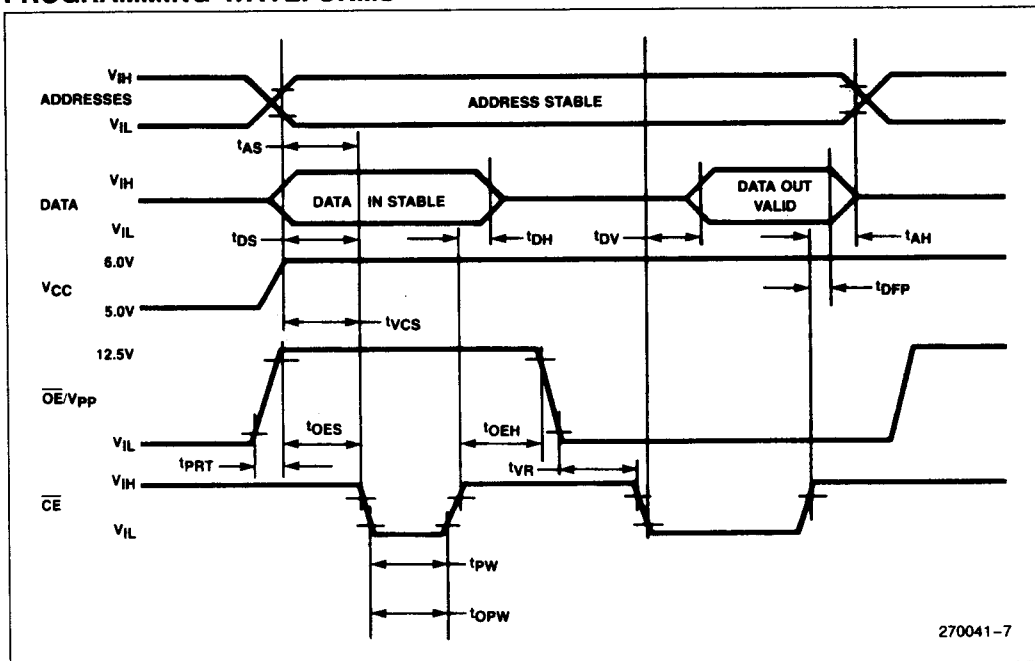
1. V_{CC} must be applied simultaneously or before \overline{OE}/V_{PP} and removed simultaneously or after \overline{OE}/V_{PP} .

2. The length of the overprogram pulse may vary from 2.85 ms to 78.75 ms as a function of the iteration counter value X.

3. Initial Program Pulse width tolerance is 1 ms $\pm 5\%$.

4. Output Float is defined as the point where data is no longer driven—see timing diagram on the following page.

PROGRAMMING WAVEFORMS



NOTES:

1. The Input Timing Reference Level is 0.8V for a V_{IL} and 2.0V for a V_{IH} .
2. t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.