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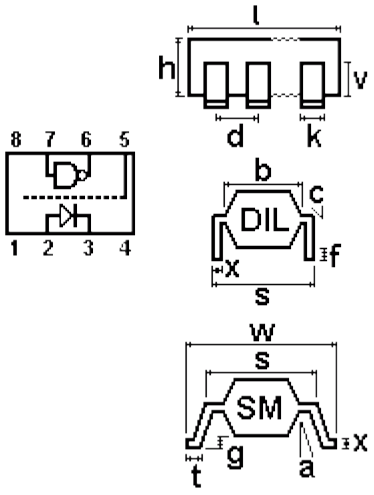
6N137
LSTTL/TTL Compatible High Speed Opto-Isolator

Circuit and Package
Features
Description
Recommended Operating Conditions
Absolute Maximum Ratings
Electrical Characteristics
Switching Characteristics

Similar Optocouplers
Home Page

Circuit and Package

Units: mm



	DIL
a	0-13 degrees
b	6.10-6.60
d	2.54 Typ
f	3.29 min
h	3.25-3.75
k	0.48-0.56 (tip), 1.1-1.4 (shoulder)
l	9.40-9.90
s	7.62 typ (shoulder)
x	0.20-0.30

Features

LSTTL/TTL Compatible: 5V Supply
Ultra High Speed
Low Input Current Required
High Common Mode Rejection
Guaranteed Performance over Temperature

3000 Vdc Withstand Test Voltage

Description

The 6N137 consists of a GaAsP emitting diode and a unique integrated detector. The photons are collected in the detector by the photodiode and then amplified by a high gain linear amplifier that drives a Schottky clamped open collector output transistor. The circuit is temperature, current and voltage compensated.
This unique isolator design provides maximum DC and AC circuit isolation between input and output while achieving LSTTL/TTL circuit compatibility. The isolator operational parameters are guaranteed from 0°C to 70°C, such that a minimum input current of 5mA will sink an eight gate fan-out (13mA) at the output with 5 volt Vcc applied to the detector. This isolation and coupling is achieved with a typical propagation delay of 45ns. The enable input provides gating of the detector with input sinking and sourcing requirements compatible with LSTTL/TTL interfacing and a propagation delay of 25ns typical. Surface Mount Option Available.
All electrical parameters are 100% tested. Specifications are guaranteed to a cumulative 0.65% AQL.

Absolute Maximum Ratings (25°C)

Storage Temperature:	-55°C to +125°C
Operating Temperature:	0°C to +70°C
Lead Soldering:	260°C for 10s, 1.6mm below seating plane

Input Diode

Peak Forward Current I_F:	40mA (duration <= 1ms)
Average Forward Current I_F:	20mA
Reverse Voltage V_R:	5V
Enable Voltage:	5.5V (not to exceed Vcc by more than 500mV)

Output Transistor

Supply Voltage V_{CC}	7V (1 minute max)
Current I_O:	50mA
Voltage V_O	7V
Collector Power Dissipation:	85mW

Recommended Operating Conditions

PARAMETER	SYMBOL	MIN	MAX	UNIT
Input Current, Low Level (each channel)	I_{FL}	0	250	µA
Input Current, High Level (each channel)	I_{FH}	6.3 (*)	15	mA
High Level Enable Voltage	V_{EH}	2.0	V_{CC}	V
Low Level Enable Voltage (output high)	V_{EL}	0	0.8	V
Supply Voltage, Output	V_{CC}	4.5	5.5	V
Fan Out (TTL Load)	N		8	
Operating Temperature	T_A	-55	70	°C

* 6.3mA condition permits at least 20% CTR degradation guardband. Initial switching threshold is 5mA or less.

Electrical Characteristics

(Over recommended temperature Ta= 0°C to 70°C u.o.s.; all typical values at Vcc=5V, Ta=25°C u.o.s.)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT	NOTES
I_{OH}	High Level Output Current	$V_{CC}=V_O=5.5V$, $V_E=2.0V$, $I_F=250\mu A$		50	250	µA	
V_{OL}	Low Level Output Voltage	$V_{CC}=5.5V$, $I_F=5mA$, $V_{EH}=2.0V$, $I_{OL(SINKING)}=13mA$		0.5	0.6	V	
I_{EH}	High Level Enable Current	$V_{CC}=5.5V$, $V_E=2.0V$		-1		mA	
I_{EL}	Low Level Enable Current	$V_{CC}=5.5V$, $V_E=0.5V$		-1.6		mA	
I_{CCH}	High Level Supply Current	$V_{CC}=5.5V$, $V_E=0.5V$, $I_F=0mA$		7	15	mA	
I_{CCL}	Low Level Supply Current	$V_{CC}=5.5V$, $V_E=0.5V$, $I_F=10mA$		13	18	mA	
I_{IO}	Input-Output Insulation Leakage Current	$T_A=25°C$, RH=45%, t=5s, $V_{IO}=3000Vdc$			1.0	µA	3
R_{IO}	Resistance	$T_A=25°C$, $V_{IO}=500V$		1000		Gohm	3
C_{IO}	Capacitance	$T_A=25°C$, f=1MHz		0.6		pF	3
V_F	Input Forward Voltage	$T_A=25°C$, $I_F=10mA$		1.5	1.75	V	6
BV_R	Input Reverse Breakdown Voltage	$T_A=25°C$, $I_R=10\mu A$	5			V	
C_{IN}	Input Capacitance	$V_F=0$, f=1MHz		60		pF	
CTR	Current Transfer Ratio	$I_F=5mA$, $R_L=100ohm$		700		%	5

Switching Characteristics (Ta=25°C, Vcc=5V)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT	NOTES
t_{PLH}	Propagation Delay Time to High Output Level	$R_L=350ohm$, $I_F=7.5mA$, $C_L=15pF$		45	75	µs	1
t_{PHL}	Propagation Delay Time to Low Output Level	$R_L=350ohm$, $I_F=7.5mA$, $C_L=15pF$		45	75	µs	1
t_R-t_F	Output Rise-Fall Time (10-90%)	$R_L=350ohm$, $I_F=7.5mA$, $C_L=15pF$		25		ns	

t_{ELH}	Propagation Delay Time of Enable from V_{EH} to V_{EL}	R_L=350ohm, I_F=7.5mA, C_L=15pF, V_{EH}=3.0V, V_{EL}=0.5V		65		ns	2
t_{EHL}	Propagation Delay Time of Enable from V_{EL} to V_{EH}			15		ns	2
CM_H	Common Mode Transient Immunity at Logic High Output Level	R_L=350ohm, I_F=0mA, V_{CM}=10V, $V_{O(MIN)}$=2V		50		V/µs	4
CM_L	Common Mode Transient Immunity at Logic Low Output Level	R_L=350ohm, I_F=5mA, V_{CM}=10V, $V_{O(MAX)}$=0.8V		-150		V/µs	4

Notes

1. The tPLH (tPHL) propagation delay is measured from the 3.75mA point on the trailing (leading) edge of the input pulse to the 1.5V point on the trailing (leading) edge of the output pulse.
2. The tELH (tEHL) enable propagation delay is measured from the 3.75mA point on the trailing (leading) edge of the input pulse to the 1.5V point on the trailing (leading) edge of the output pulse.
3. Device considered as two-terminaled: pins 2,3 shorted together and pins 5,6,7,8 shorted together.
4. Common mode transient immunity in Logic High (Low) Level is the maximum tolerable, positive (negative), dVcm/dt on the leading (trailing) edge of the common mode pulse signal, Vcm, to ensure that the output will remain in a Logic High (Low) state, ie. Vo>2.0V (Vo<0.8V).
5. DC Current Transfer Ratio is defined as the ratio of the output collector current to the forward bias input current times 100%.
6. At 10mA, Vf decreases with increasing temperature at the rate of 1.6mV/°C.