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ICPL2601
High CMR, High Speed Optoisolator

Circuit and Package

Units: mm	DIL
a	0-13 degrees
b	6.10-6.60
d	2.54 Typ
f	3.29 Min
h	3.25-3.75
k	0.48-0.56 tip,1.1-1.4 shoulder
l	9.40-9.90
s	7.62 Typ
x	0.20-0.30

Features

LSTTL/TTL Compatible
High Speed
Low Input Current Required
Guaranteed Performance over Temperature
Withstand Test Voltage 3000Vdc
Internal Shield for High Common Mode Rejection

Description

The ICPL2601 consists of a GaAsP emitting diode and a unique integrated detector. The photons are collected in the detector by a photodiode and then amplified by a high gain linear amplifer that drives a Schottky clamped open detector output transistor. The circuit is temperature, current and voltage compensated. This unique isolator design provides maximum DC and AC circuit isolation between input and output while achieving LSTTL/TTL circuit compatibility. The isolator operational parameters are guaranteed from 0°C to 70°C, such that a minimum input current of 5mA will sink an eight gate fan-out (13mA) at the output with 5 volt Vcc applied to the detector. This isolation and coupling is achieved with a typical propagation delay of 39ns. The enable input provides gating of the detector with input sinking and sourcing requirements compatible with LSTTL/TTL interfacing and a propagation delay of 35ns typical. Surface Mount Option Available.
All electrical parameters are 100% tested. Specifications are guaranteed to a cumulative 0.65% AQL.

Absolute Maximum Ratings (25°C)

Storage Temperature:	-55°C to +125°C
Operating Temperature:	0°C to +70°C
Lead Soldering:	260°C for 10s, 1.6mm below seating plane

Input Diode

Forward Current:	20mA (note 2)
Reverse Voltage:	5V
Enable Voltage:	5.5V (not to exceed Vcc by more than 500mV)

Output Transistor

Supply Voltage V_{CC}:	7V (1 minute max)
Current I_O:	25mA
Collector Voltage V_O:	7V
Collector Power Dissipation:	40mW

Recommended Operating Conditions

PARAMETER	SYMBOL	MIN	MAX	UNIT
Input Current, Low Level	I_{FL}	0	250	µA
Input Current, High Level	I_{FH}	6.3 (*)	15	mA
High Level Enable Voltage	V_{EH}	2.0	Vcc	V
Low Level Enable Voltage (Output High)	V_{EL}	0	0.8	V
Supply Voltage, Output	V_{CC}	4.5	5.5	V
Fan Out (TTL Load)	N		8	
Operating Temperature	T_A	0	70	°C

* 6.3mA condition permits at least 20% CTR degradation guardband. Initial switching threshold is 5mA or less.

Electrical Characteristics

(Over recommended temperature Ta= 0°C to 70°C u.o.s.; all typical values at Vcc=5V, Ta=25°C u.o.s.)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT	NOTES
I_{OH}	High Level Output Current	V_{CC}=V_O=5.5V, V_E=2.0V, I_F=250µA		7	250	µA	
V_{OL}	Low Level Output Voltage	V_{CC}=5.5V, V_E=2.0V, I_F=5mA, I_{OL}(sinking)=13mA		0.4	0.6	V	
I_{EH}	High Level Enable Current	V_{CC}=5.5V, V_E=2.0V		-1.0		mA	
I_{EL}	Low Level Enable Current	V_{CC}=5.5V, V_E=0.5V		-1.6	-2.0	mA	
I_{CCH}	High Level Supply Current	V_{CC}=5.5V, V_E=0.5V, I_F=0		10	15	mA	
I_{CCL}	Low Level Supply Current	V_{CC}=5.5V, V_E=0.5V, I_F=10mA		15	19	mA	
I_{IO}	Input-Output Insulation Leakage Current	RH=45%, T_A=25°C, t=5s, V_{IO}=3000Vdc			1.0	µA	3
R_{IO}	Resistance	T_A=25°C, V_{IO}=500V		1000		Gohm	3
C_{IO}	Capacitance	T_A=25°C, f=1MHz		0.6		pF	3
V_F	Input Forward Voltage	T_A=25°C, I_F=10mA		1.5	1.75	V	
BV_R	Input Reverse Breakdown Voltage	T_A=25°C, I_R=10µA	5			V	
C_{IN}	Input Capacitance	V_F=0, f=1MHz		60		pF	
CTR	Current Transfer Ratio	I_F=5mA, R_L=100ohm		700		%	5
V_{EH}	High Level Enable Voltage		2.0			V	8
V_{EL}	Low Level Enable Voltage				0.8	V	
dV_F/dT_A	Input Diode Temperature Coefficient	I_F=10mA		-1.6		mV/°C	

Switching Characteristics (Ta=25°C, Vcc=5V)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT	NOTES
t_{PLH}	Propagation Delay Time to High Output Level	R_L=350ohm, C_L=15pF, I_F=7.5mA		35	75	ns	4
t_{PHL}	Propagation Delay Time to Low Output Level			39	75	ns	4
t_R	Output Rise Time (10-90%)			27		ns	
t_F	Output Fall Time (90-10%)			16		ns	
t_{ELH}	Propagation Delay Time of Enable from V_{EH} to V_{EL}	R_L=350ohm, C_L=15pF, I_F=7.5mA, V_{EH}=3.0V, V_{EL}=0		27		ns	5
t_{EHL}	Propagation Delay Time of Enable from V_{EL} to V_{EH}			16		ns	5
CM_H	Common Mode Transient Immunity at High Output Level	V_{CM}=50Vpeak, R_L=350ohm, I_F=0mA, V_O(min)=2V	1000	10000		V/µs	6,7
CM_L	Common Mode Transient Immunity at Low Output Level	V_{CM}=50Vpeak, R_L=350ohm, I_F=7.5mA, V_O(max)=0.8V	-1000	-10000		V/µs	6,7

Notes

1. Bypassing the power supply line is required, with a 0.01µF ceramic disc capacitor adjacent to each isolator. The power supply bus for the isolator(s) should be separate from the bus for any active loads otherwise a larger value of bypass capacitor (up to 0.1µF) may be needed to suppress regenerative feedback via the power supply.
2. Peaking circuits may produce transient input currents up to 50mA, 50ns maximum pulse width, provided average current does not exceed 20mA.
3. Device considered two-terminaled: pins 1,2,3,4 shorted together and pins 5,6,7,8 shorted together.
4. The tPLH (tPHL) propagation delay is measured from the 3.75mA point on the trailing (leading) edge of the input pulse to the 1.5V point on the trailing (leading) edge of the output pulse.
5. The tELH (tEHL) enable propagation delay is measured from the 3.75mA point on the trailing (leading) edge of the input pulse to the 1.5V point on the trailing (leading) edge of the output pulse.
6. CMh (CMl) is the maximum tolerable rate of rise (fall) of the common mode voltage to assure that the output will remain in a high (low) logic state, Vo > 2.0V (Vo < 0.8V).
7. For sinusoidal voltages, $(dVcm/dt)max=pi*f_{CM}*V_{CMp-p}$.
8. No external pull-up is required for a high logic state on the enable input.

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