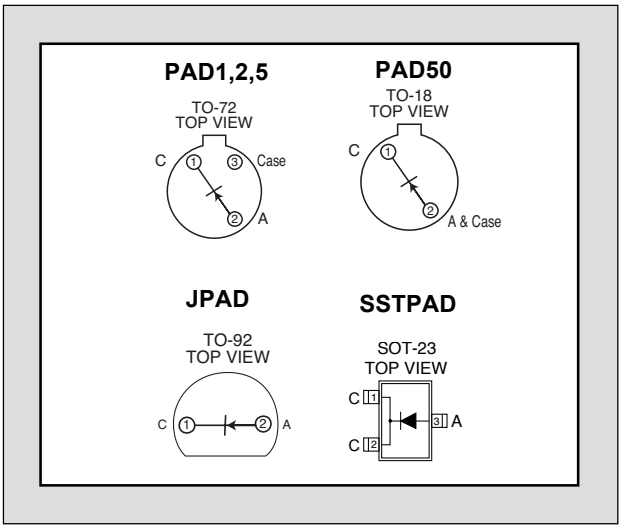
LINEAR SYSTEMS

*Twenty-Five Years Of Quality Through Innovation*

# PAD SERIES

## PICO AMPERE DIODES

| FEATURES | |
|---|---|
| DIRECT REPLACEMENT FOR SILICONIX PAD SERIES | |
| REVERSE BREAKDOWN VOLTAGE | $BV_R \geq -30V$ |
| REVERSE CAPACITANCE | $C_{rss} \leq 2.0pF$ |
| **ABSOLUTE MAXIMUM RATINGS**[1] @ 25 °C (unless otherwise stated) | |
| **Maximum Temperatures** | |
| Storage Temperature | -55 to +150 °C |
| Operating Junction Temperature | -55 to +150 °C |
| **Maximum Power Dissipation** | |
| Continuous Power Dissipation (PAD) | 300mW |
| Continuous Power Dissipation (J/SSTPAD) | 350mW |
| **Maximum Currents** | |
| Forward Current (PAD) | 50mA |
| Forward Current (J/SSTPAD) | 10mA |




**COMMON ELECTRICAL CHARACTERISTICS @ 25 °C (unless otherwise stated)**

| SYMBOL | CHARACTERISTIC | | MIN | TYP | MAX | UNITS | CONDITIONS |
|---|---|---|---|---|---|---|---|
| $BV_R$ | Reverse Breakdown Voltage | ALL PAD | -45 | | | V | $I_R$ = -1µA |
| | | ALL SSTPAD | -30 | | | | |
| | | ALL JPAD | -35 | | | | |
| $V_F$ | Forward Voltage | | | 0.8 | 1.5 | | $I_F$ = 1mA |
| $C_{rss}$ | Total Reverse Capacitance | PAD1,5 | | 0.5 | 0.8 | pF | $V_R$ = -5V, *f* = 1MHz |
| | | All Others | | 1.5 | 2 | | |

**SPECIFIC ELECTRICAL CHARACTERISTICS @ 25 °C (unless otherwise stated)**

| SYMBOL | CHARACTERISTIC | | PAD | JPAD | SSTPAD | UNITS | CONDITIONS |
|---|---|---|---|---|---|---|---|
| $I_R$ | Maximum Reverse Leakage Current | PAD1 | -1 | | | pA | $V_R$ = -20V |
| | | PAD2 | -2 | | | | |
| | | (SST/J)PAD5 | -5 | -5 | -5 | | |
| | | (SST/J)PAD10 | -10 | -10 | -10 | | |
| | | (SST/J)PAD20 | -20 | -20 | -20 | | |
| | | (SST/J)PAD50 | -50 | -50 | -50 | | |
| | | (SST/J)PAD100 | -100 | -100 | | | |
| | | (SST/J)PAD200 | | -200 | | | |
| | | (SST/J)PAD500 | | -500 | | | |

1. Derate 2mW/°C above 25°C
2. Derate 2.8mW/°C above 25°C

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2/13/12 Rev#A5 ECN# PAD SERIES

**Figure 1. Operational Amplifier Protection**
Input Differential Voltage limited to 0.8V (typ) by JPADs $D_1$ and $D_2$. Common Mode Input voltage limited by JPADs $D_3$ and $D_4$ to ±15V.

**Figure 2. Sample and Hold Circuit**
Typical Sample and Hold circuit with clipping. JPAD diodes reduce offset voltages fed capacitively from the JFET switch gate.

**FIGURE 1**

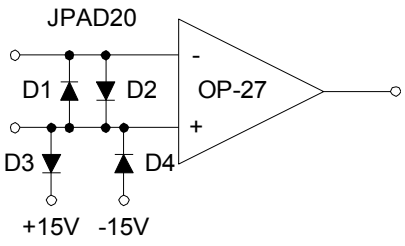
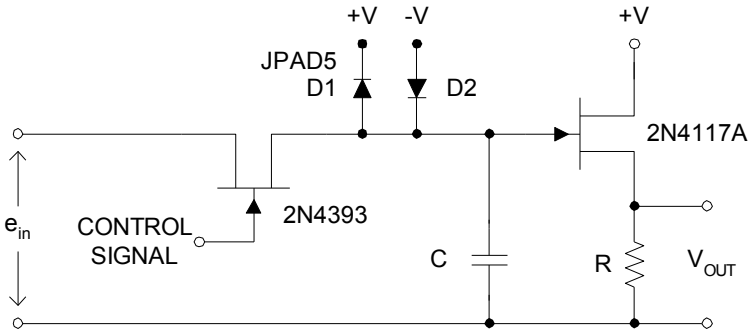
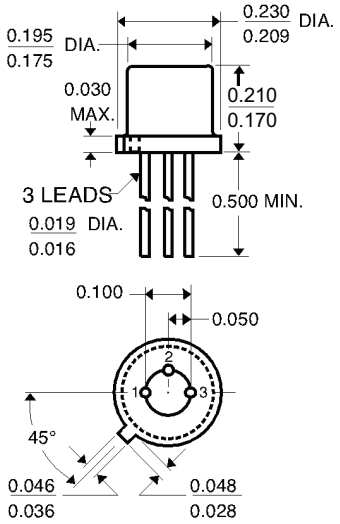


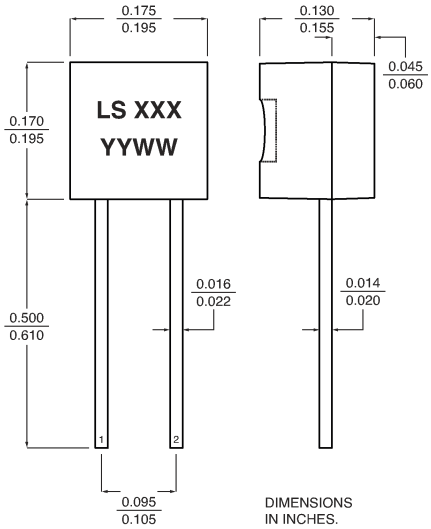

**FIGURE 2**



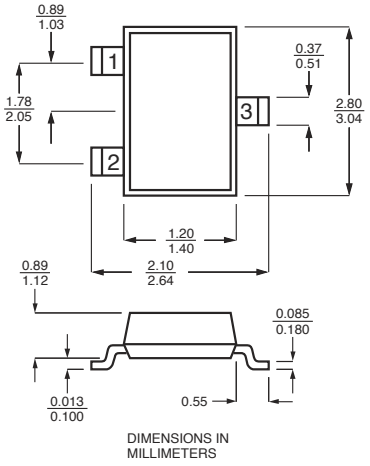

## TO-72
Three Lead




## TO-92




## SOT-23




1. Absolute maximum ratings are limiting values above which serviceability may be impaired.
2. The PAD type number denotes its maximum reverse current value in pico amperes. Devices with $I_R$ values intermediate to those shown are available upon request.



**Linear Integrated Systems (LIS) is a 25-year-old, third-generation precision semiconductor company providing high-quality discrete components. Expertise brought to LIS is based on processes and products developed at Amelco, Union Carbide, Intersil and Micro Power Systems by company President John H. Hall. Hall, a protégé of Silicon Valley legend Dr. Jean Hoerni, was the director of IC Development at Union Carbide, co-founder and vice president of R&D at Intersil, and founder/president of Micro Power Systems.**

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