

LSK389 **ULTRA LOW NOISE** MONOLITHIC DUAL N-CHANNEL JFET



Linear Systems replaces discontinued Toshiba 2SK389 with LSK389

The 2SK389 / LSK389 is a monolithic matched dual JFET on a single chip

Why use On-Chip Dual JFET instead of 2 single JFETS?

Save Cost

2SK389 / LSK389 removes significant cost for test screening time needed to match loss on 2 individual JFETS and offers ZERO yield loss.

Improve Performance

2SK389 / LSK389 On-Chip loss matching gives closest possible synchronous electrical performance and also offers better matched performance when the chip is subjected to temperature.

2SK389 / LSK389 Applications:

End audio microphone, Audio Amplifier and audio effects box manufacturers

Instrumentation-input stages of various instruments The acoustic sensor market -sonoboys / antisubmarine, military personnel and vehicle detectors, sonar makers. Radiation detectors.

FEATURES					
ULTRA LOW NOISE	en	= 0.9nV/√Hz (typ)			
TIGHT MATCHING	Vc	$ S_{S1-2} = 20 \text{mV max}$			
HIGH BREAKDOWN VOLTAGE	В	V_{GSS} = 40V max			
HIGH GAIN	AIN $Y_{fs} = 20mS (typ)$				
LOW CAPACITANCE	TANCE 25pF typ				
IMPROVED SECOND SOURCE REPLACEMENT FOR 2SK389					
ABSOLUTE MAXIMUM RATINGS ¹					
@ 25 °C (unless otherwise stated)					
Maximum Temperatures					
Storage Temperature	-65 to +150 °C				
Operating Junction Temperature	-55 to +135 °C				
Maximum Power Dissipation					
Continuous Power Dissipation @ +125 °C	;	400mW			
Maximum Currents					
Gate Forward Current		$I_{G(F)} = 10mA$			
Maximum Voltages					
Gate to Source		$V_{GSS} = 40V$			
Gate to Drain		$V_{GDS} = 40V$			

MATCHING CHARACTERISTICS @ 25 °C (unless otherwise stated)

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNIT	CONDITIONS
$\left V_{\text{GS1}} - V_{\text{GS2}}\right $	Differential Gate to Source Cutoff Voltage			20	mV	V _{DS} = 10V, I _D = 1mA
IDSS1 IDSS2	Gate to Source Saturation Current Ratio	0.9			ı	V _{DS} = 10V, V _{GS} = 0V

ELECTRICAL CHARACTERISTICS @ 25 °C (unless otherwise stated)

SYMBOL	CHARACTERISTIC		MIN	TYP	MAX	UNITS	CONDITIONS
BV _{GSS}	Gate to Source Breakdown Voltage		40			٧	$V_{DS} = 0$, $I_{D} = 100 \mu A$
V _{GS(OFF)}	Gate to Source Pinch-off Voltage		0.15		2	٧	$V_{DS} = 10V, I_D = 0.1\mu A$
	I _{DSS} Drain to Source Saturation Current	LSK389A	2.6		6.5	mA	V _{DS} = 10V, V _{GS} = 0
I _{DSS}		LSK389B	6		12		
		LSK389C	10		20		
I _{GSS}	Gate to Source Leakage Current				200	рА	$V_{GS} = -30V, V_{DS} = 0$
Y _{fs}	Full Conduction Transconductance Noise Voltage Noise Voltage		8	20		mS	$V_{DS} = 10V, V_{GS} = 0, I_{DSS} = 3mA,$ f = 1kHz
e _n				0.9	1.9	nV/√Hz	V_{DS} = 10V, I_{D} = 2mA, f = 1kHz, NBW = 1Hz
e _n				2.5	4	nV/√Hz	V_{DS} = 10V, I_{D} = 2mA, f = 10Hz, NBW = 1Hz
C _{ISS}	Common Source Input Capacitance			25		pF	$V_{DS} = 10V, V_{GS} = 0, f = 1MHz,$
C _{RSS}	Common Source Reverse Transfer Cap.			5.5		рF	$V_{DG} = 10V$, $I_{D} = 0$, $f = 1MHz$,

Available Packages:

2SK389 / LSK389 in SOIC-8 Lead

2SK389 / LSK389 in Thru-hole TO-71 6 Lead

2SK389 / LSK389 Toshiba footprint, SO8 / TO-71 with socket adaptor

2SK389 / LSK389 available as bare die

2SK389 / LSK389 available as wafer form

Please contact Micross for package and die dimensions



