

Linear Systems replaces discontinued Siliconix U421

The LSU421 is a high input impedance Monolithic Dual N-Channel JFET

The LSU421 monolithic dual n-channel JFET is designed to provide very high input impedance for differential amplification and impedance matching. Among its many unique features, this series offers operating gate current specified at -250 fA. The LSU421 is a direct replacement for discontinued Siliconix U421.

The hermetically sealed TO-71 & TO-78 packages are well suited for military applications. The 8 Pin P-DIP and 8 Pin SOIC provide ease of manufacturing, and the symmetrical pinout prevents improper orientation.

(See Packaging Information).

LSU421 Applications:

- Ultra Low Input Current Differential Amps
- High-Speed Comparators
- Impedance Converters

FEATURES

HIGH INPUT IMPEDANCE	$I_G = 0.25\text{pA MAX}$
HIGH GAIN	$g_{fs} = 120\mu\text{mho MIN}$
LOW POWER OPERATION	$V_{GS(OFF)} = 2\text{V MAX}$

ABSOLUTE MAXIMUM RATINGS

@ 25°C (unless otherwise noted)

Maximum Temperatures

Storage Temperature	-65°C to +150°C
Operating Junction Temperature	+150°C

Maximum Voltage and Current for Each Transistor – Note 1

$-V_{GSS}$	Gate Voltage to Drain or Source	40V
$-V_{DSO}$	Drain to Source Voltage	40V
$-I_{G(f)}$	Gate Forward Current	10mA

Maximum Power Dissipation

Device Dissipation @ Free Air – Total 400mW @ +125°C

MATCHING CHARACTERISTICS @ 25°C UNLESS OTHERWISE NOTED

SYMBOL	CHARACTERISTICS	VALUE	UNITS	CONDITIONS
$ \Delta V_{GS1-2}/\Delta T _{\text{max}}$	DRIFT VS. TEMPERATURE	10	$\mu\text{V}/^\circ\text{C}$	$V_{DG}=10\text{V}, I_D=30\mu\text{A}$ $T_A=-55^\circ\text{C to }+125^\circ\text{C}$
$ V_{GS1-2} _{\text{max}}$	OFFSET VOLTAGE	10	mV	$V_{DG}=10\text{V}, I_D=30\mu\text{A}$

ELECTRICAL CHARACTERISTICS @ 25°C (unless otherwise noted)

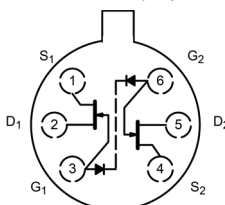
SYMBOL	CHARACTERISTICS	MIN.	TYP.	MAX.	UNITS	CONDITIONS
BV_{GSS}	Breakdown Voltage	40	60	--	V	$V_{DS} = 0$ $I_G = 1\text{nA}$
BV_{GGO}	Gate-To-Gate Breakdown	40	--	--	V	$I_G = 1\mu\text{A}$ $I_D = 0$ $I_S = 0$
TRANSCONDUCTANCE						
Y_{fss}	Full Conduction	300	--	1500	μmho	$V_{DS} = 10\text{V}$ $V_{GS} = 0\text{V}$ $f = 1\text{kHz}$
Y_{fs}	Typical Operation	120	200	350	μmho	$V_{DG} = 10\text{V}$ $I_D = 30\mu\text{A}$ $f = 1\text{kHz}$
DRAIN CURRENT						
I_{DSS}	Full Conduction	60	--	1000	μA	$V_{DS} = 10\text{V}$ $V_{GS} = 0\text{V}$
GATE VOLTAGE						
$V_{GS(off)}$	Pinchoff voltage	--	--	2.0	V	$V_{DS} = 10\text{V}$ $I_D = 1\text{nA}$
V_{GS}	Operating Range	--	--	1.8	V	$V_{DG} = 10\text{V}$ $I_D = 30\mu\text{A}$
GATE CURRENT						
$I_{Gmax.}$	Operating	--	--	.25	μA	$V_{DG} = 10\text{V}$ $I_D = 30\mu\text{A}$
$-I_{Gmax.}$	High Temperature	--	--	250	μA	$T_A = +125^\circ\text{C}$
$I_{GSSmax.}$	At Full Conduction	--	--	1.0	μA	$V_{DS} = 0\text{V}$ $V_{GS} = 20\text{V}$
$-I_{GSSmax.}$	High Temperature	--	--	1.0	μA	$T_A = +125^\circ\text{C}$
OUTPUT CONDUCTANCE						
Y_{OSS}	Full Conduction	--	--	10	μmho	$V_{DS} = 10\text{V}$ $V_{GS} = 0\text{V}$
Y_{OS}	Operating	--	0.1	3.0	μmho	$V_{DG} = 10\text{V}$ $I_D = 30\mu\text{A}$
COMMON MODE REJECTION						
CMR	$-20 \log \Delta V_{GS1-2}/\Delta V_{DS} $	--	90	--	dB	$\Delta V_{DS} = 10 \text{ to } 20\text{V}$ $I_D = 30\mu\text{A}$
	$-20 \log \Delta V_{GS1-2}/\Delta V_{DS} $	--	90	--	dB	$\Delta V_{DS} = 5 \text{ to } 10\text{V}$ $I_D = 30\mu\text{A}$
NOISE						
NF	Figure	--	--	1	dB	$V_{DG} = 10\text{V}$ $I_D = 30\mu\text{A}$ $R_G = 10\text{M}\Omega$ $f = 10\text{Hz}$
e_n	Voltage	--	20	70	$\text{nV}/\sqrt{\text{Hz}}$	$V_{DG} = 10\text{V}$ $I_D = 30\mu\text{A}$ $f = 10\text{Hz}$
		--	10	--		$V_{DG} = 10\text{V}$ $I_D = 30\mu\text{A}$ $f = 1\text{kHz}$
CAPACITANCE						
C_{ISS}	Input	--	--	3.0	pF	$V_{DS} = 10\text{V}$ $V_{GS} = 0$ $f = 1\text{MHz}$
C_{RSS}	Reverse Transfer	--	--	1.5	pF	

Note 1 – These ratings are limiting values above which the serviceability of any semiconductor may be impaired

Available Packages:

LSU421 in TO-71 & TO-78
LSU421 in PDIP & SOIC
LSU421 available as bare die
Please contact [Micross](http://micross.com) for full package and die dimensions
Email: chipcomponents@micross.com

TO-71 / TO-78 (Top View)



P-DIP / SOIC (Top View)

