ADVANCE

MICRON SEMICONDUCTOR PRODUCTS, INC.

16, 32, 64 MEG x 72 REGISTERED SDRAM DIMMs

SYNCHRONOUS DRAM MODULE

MT18LSDT1672, MT18LSDT3272, MT18LSDT6472

For the latest data sheet revisions, please refer to the Micron Web site: www.micron.com/mti/msp/html/datasheet.html

FEATURES

- JEDEC-standard 168-pin, dual in-line memory module (DIMM)
- PC133- and PC100-compliant
- Registered inputs with one-clock delay
- Phase-lock loop (PLL) clock driver to reduce loading
- Utilizes 133 MHz and 125 MHz SDRAM components
- ECC-optimized pinout
- 128MB (16 Meg x 72), 256MB (32 Meg x 72), and 512MB (64 Meg x 72)
- Single +3.3V ±0.3V power supply
- Fully synchronous; all signals registered on positive edge of PLL clock
- Internal pipelined operation; column address can be changed every clock cycle
- Internal SDRAM banks for hiding row access/precharge
- Programmable burst lengths: 1, 2, 4, 8 or full page
- Auto Precharge and Auto Refresh Modes
- Self Refresh Mode
- 64ms, 4,096-cycle refresh
- LVTTL-compatible inputs and outputs
- Serial Presence-Detect (SPD)

OPTIONS / MARKING

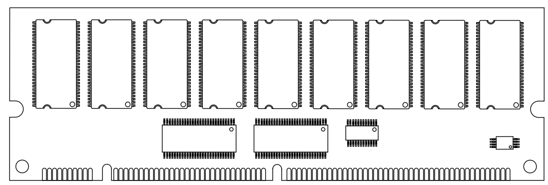
OPTIONS	MARKING
• Package	
168-pin DIMM (gold)	G
• Frequency/CAS Latency*	
133 MHz/CL = 2 (7.5ns, 133 MHz SDRAMs)	-13E
133 MHz/CL = 3 (7.5ns, 133 MHz SDRAMs)	-133
100 MHz/CL = 2 (8ns, 125 MHz SDRAM)	-10E

*Device latency only; extra clock cycle required due to input register.

KEY SDRAM COMPONENT TIMING PARAMETERS

MODULE MARKING	SPEED GRADE	CAS LATENCY	ACCESS TIME	SETUP TIME	HOLD TIME
-13E	-7E	2	5.4ns	1.5ns	0.8ns
-133	-75	3	5.4ns	1.5ns	0.8ns
-10E	-8E	2	6ns	2ns	1ns

PIN ASSIGNMENT (FRONT VIEW) 168-PIN DIMM



PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL
1	VSS	43	VSS	85	VSS	127	VSS
2	DQ0	44	DNU	86	DQ32	128	CKE0
3	DQ1	45	S2#	87	DQ33	129	RFU (S3#)
4	DQ2	46	DQMB2	88	DQ34	130	DQMB6
5	DQ3	47	DQMB3	89	DQ35	131	DQMB7
6	VDD	48	DNU	90	VDD	132	RFU (A13)
7	DQ4	49	VDD	91	DQ36	133	VDD
8	DQ5	50	NC	92	DQ37	134	NC
9	DQ6	51	NC	93	DQ38	135	NC
10	DQ7	52	CB2	94	DQ39	136	CB6
11	DQ8	53	CB3	95	DQ40	137	CB7
12	VSS	54	VSS	96	VSS	138	VSS
13	DQ9	55	DQ16	97	DQ41	139	DQ48
14	DQ10	56	DQ17	98	DQ42	140	DQ49
15	DQ11	57	DQ18	99	DQ43	141	DQ50
16	DQ12	58	DQ19	100	DQ44	142	DQ51
17	DQ13	59	VDD	101	DQ45	143	VDD
18	VDD	60	DQ20	102	VDD	144	DQ52
19	DQ14	61	NC	103	DQ46	145	NC
20	DQ15	62	NC	104	DQ47	146	NC
21	CB0	63	RFU (CKE1)	105	CB4	147	REGE
22	CB1	64	VSS	106	CB5	148	VSS
23	VSS	65	DQ21	107	VSS	149	DQ53
24	NC	66	DQ22	108	NC	150	DQ54
25	NC	67	DQ23	109	NC	151	DQ55
26	VDD	68	VSS	110	VDD	152	VSS
27	WE#	69	DQ24	111	CAS#	153	DQ56
28	DQMB0	70	DQ25	112	DQMB4	154	DQ57
29	DQMB1	71	DQ26	113	DQMB5	155	DQ58
30	S0#	72	DQ27	114	RFU (S1#)	156	DQ59
31	DNU	73	VDD	115	RAS#	157	VDD
32	VSS	74	DQ28	116	VSS	158	DQ60
33	A0	75	DQ29	117	A1	159	DQ61
34	A2	76	DQ30	118	A3	160	DQ62
35	A4	77	DQ31	119	A5	161	DQ63
36	A6	78	VSS	120	A7	162	VSS
37	A8	79	CK2	121	A9	163	CK3
38	A10	80	NC	122	BA0	164	NC
39	BA1	81	WP	123	A11	165	SA0
40	VDD	82	SDA	124	VDD	166	SA1
41	VDD	83	SCL	125	CK1	167	SA2
42	CK0	84	VDD	126	RFU	168	VDD

NOTE: Symbols in parentheses are not used on these modules but may be used for other modules in this product family. They are for reference only.

PART NUMBERS

PART NUMBER	CONFIGURATION	SYSTEM BUS SPEED
MT18LSDT1672G-13E__	16 Meg x 72	133 MHz
MT18LSDT1672G-133__	16 Meg x 72	133 MHz
MT18LSDT1672G-10E__	16 Meg x 72	100 MHz
MT18LSDT3272G-133__	32 Meg x 72	133 MHz
MT18LSDT3272G-13E__	32 Meg x 72	133 MHz
MT18LSDT3272G-10E__	32 Meg x 72	100 MHz
MT18LSDT6472G-133__	64 Meg x 72	133 MHz
MT18LSDT6472G-13E__	64 Meg x 72	133 MHz
MT18LSDT6472G-10E__	64 Meg x 72	100 MHz

NOTE: All part numbers end with a two-place code (not shown), designating component and PCB revisions. Consult factory for current revision codes. Example: MT18LSDT1672G-133B1

GENERAL DESCRIPTION

The MT18LSDT1672, MT18LSDT3272 and MT18LSDT6472 are high-speed CMOS, dynamic random-access, 128MB, 256MB, and 512MB memories organized in a x72 configuration. These modules use internally configured quad-bank SDRAMs with a synchronous interface (all signals are registered on the positive edge of clock signals CK0).

Read and write accesses to the SDRAM modules are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed (BA0, BA1 select the bank, A0-A11 select the row). The address bits registered coincident with the READ or WRITE command are used to select the starting column location for the burst access.

These modules provide for programmable READ or WRITE burst lengths of 1, 2, 4, or 8 locations, or full page, with a burst terminate option. An auto precharge function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst sequence.

These modules use an internal pipelined architecture to achieve high-speed operation. This architecture is compatible with the *2n* rule of prefetch architectures, but it also allows the column address to be changed on every clock cycle to achieve a high-speed, fully random access. Precharging one bank while accessing one of the other three banks will hide the PRECHARGE cycles and provide seamless, high-speed, random-access operation.

These modules are designed to operate in 3.3V, low-power memory systems. An auto refresh mode is provided, along with a power-saving, power-down mode. All inputs and outputs are LVTTL-compatible.

SDRAM modules offer substantial advances in DRAM operating performance, including the ability to synchronously burst data at a high data rate with automatic column-address generation, the ability to interleave between internal banks in order to hide precharge time, and the capability to randomly change column addresses on each clock cycle during a burst access. For more information regarding SDRAM operation, refer to the 64Mb, 128Mb, 256Mb x4, x8, x16 SDRAM data sheets.

PLL AND REGISTER OPERATION

These modules can be operated in either registered mode (REGE pin HIGH), where the control/address input signals are latched in the register on one rising clock edge and sent to the SDRAM devices on the following rising clock edge (data access is delayed by one clock), or in buffered mode (REGE pin LOW) where the input signals pass through the register/buffer to the SDRAM devices on the same clock. A phase-lock loop (PLL) on the modules is used to redrive the clock signals to the SDRAM devices to minimize system clock loading (CK0 is connected to the PLL, and CK1, CK2, and CK3 are terminated).

SERIAL PRESENCE-DETECT OPERATION

These modules incorporate serial presence-detect (SPD). The SPD function is implemented using a 2,048-bit EEPROM. This nonvolatile storage device contains 256 bytes. The first 128 bytes can be programmed by Micron to identify the module type and various SDRAM organizations and timing parameters. The remaining 128 bytes of storage are available for use by the customer. System READ/WRITE operations between the master (system logic) and the slave EEPROM device (DIMM) occur via a standard IIC bus using the DIMM's SCL (clock) and SDA (data) signals, together with SA(2:0), which provide eight unique DIMM/EEPROM addresses.

SPD CLOCK AND DATA CONVENTIONS

Data states on the SDA line can change only during SCL LOW. SDA state changes during SCL HIGH are reserved for indicating start and stop conditions (Figures 1 and 2).

SPD START CONDITION

All commands are preceded by the start condition, which is a HIGH-to-LOW transition of SDA when SCL is HIGH. The SPD device continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition has been met.

SPD STOP CONDITION

All communications are terminated by a stop condition, which is a LOW-to-HIGH transition of SDA when SCL is HIGH. The stop condition is also used to place the SPD device into standby power mode.

SPD ACKNOWLEDGE

Acknowledge is a software convention used to indicate successful data transfers. The transmitting device, either master or slave, will release the bus after transmitting eight bits. During the ninth clock cycle, the receiver will pull the SDA line LOW to acknowledge that it received the eight bits of data (Figure 3).

The SPD device will always respond with an acknowledge after recognition of a start condition and its slave address. If both the device and a WRITE operation have been selected, the SPD device will respond with an acknowledge after the receipt of each subsequent eight-bit word. In the read mode the SPD device will transmit eight bits of data, release the SDA line and monitor the line for an acknowledge. If an acknowledge is detected and no stop condition is generated by the master, the slave will continue to transmit data. If an acknowledge is not detected, the slave will terminate further data transmissions and await the stop condition to return to standby power mode.

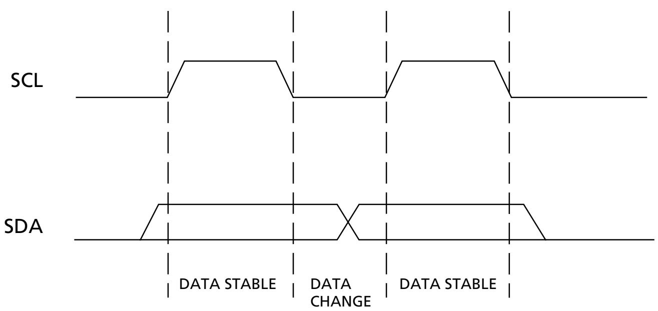


Figure 1
Data Validity

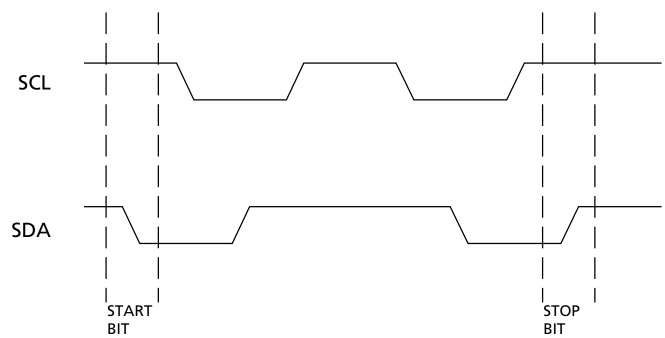


Figure 2
Definition of Start and Stop

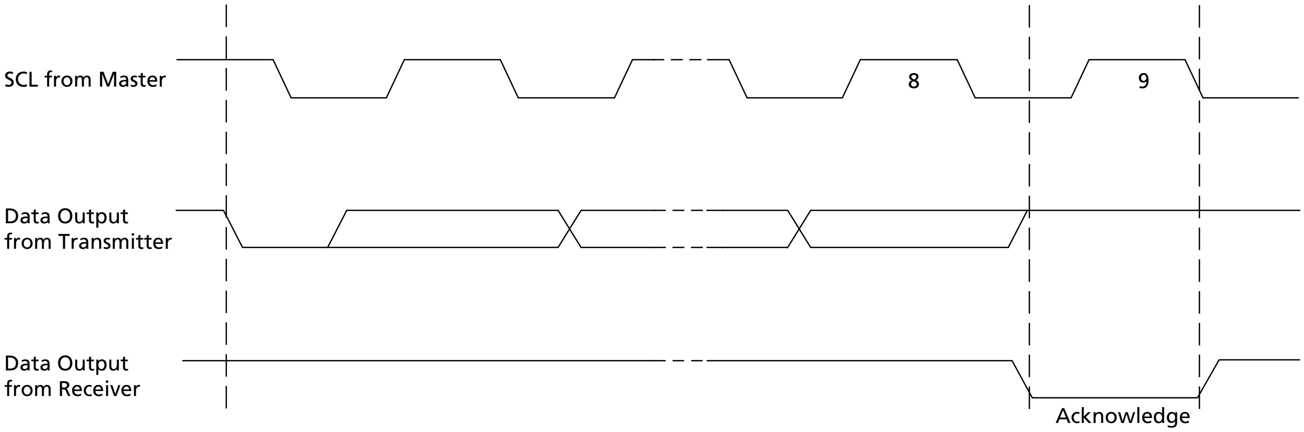
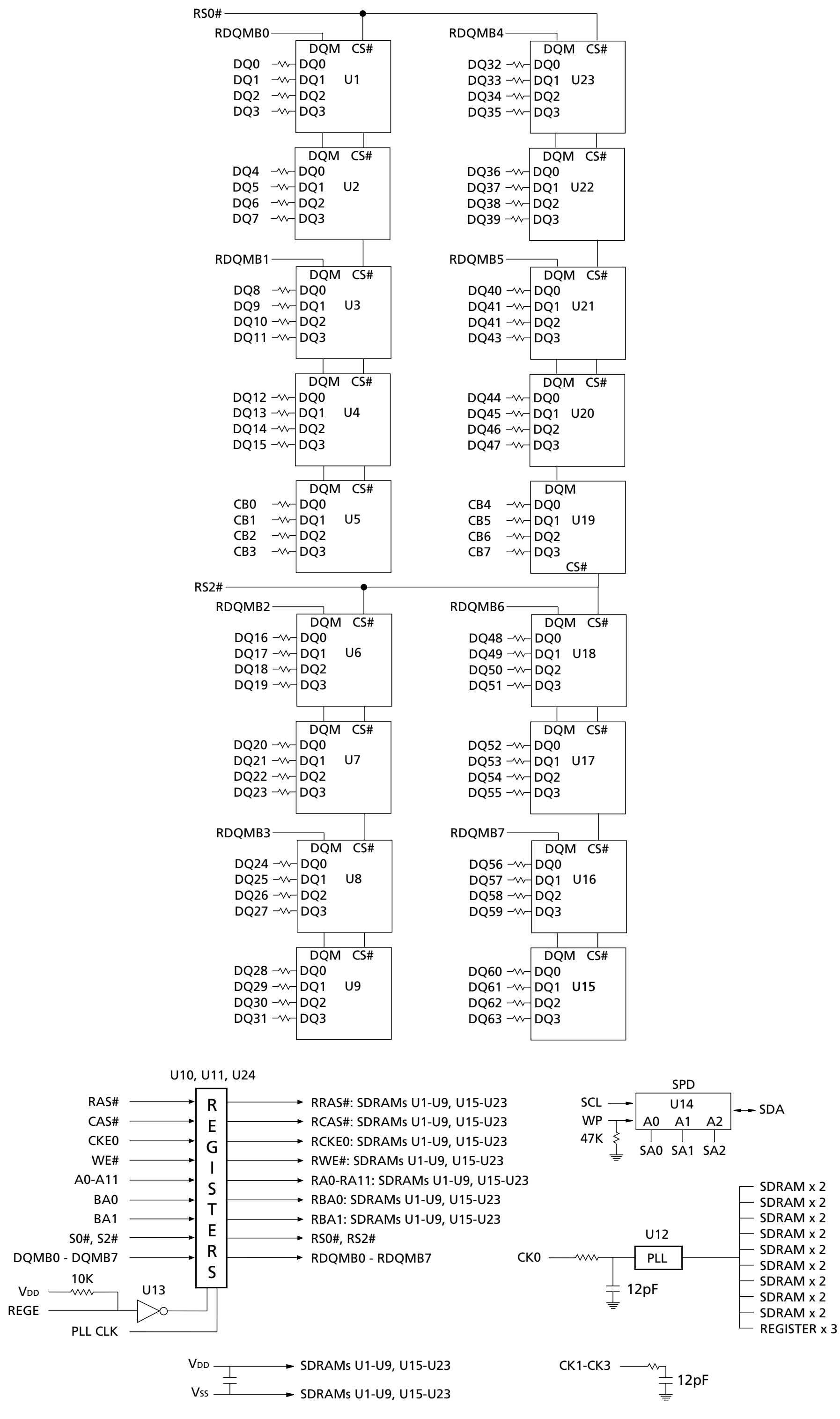


Figure 3
Acknowledge Response From Receiver

FUNCTIONAL BLOCK DIAGRAM
MT18LSDT1672 (128MB), MT18LSDT3272 (256MB), MT18LSDT6472 (512MB)



NOTE: 1. All resistor values are 10 ohms unless otherwise specified.

U1-U9, U15-U23 = MT48LC16M4A2TG SDRAMs for 128MB
U1-U9, U15-U23 = MT48LC32M4A2TG SDRAMS for 256MB
U1-U9, U15-U23 = MT48LC64M4A2TG SDRAMS for 512MB

PIN DESCRIPTIONS

PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
27, 111, 115	WE#, CAS#, RAS#	Input	Command Inputs: WE#, CAS#, and RAS# (along with S0#, S2#) define the command being entered.
42, 79, 125, 163	CK0-CK3	Input	Clock: CK0 is distributed through an on-board PLL to all devices. CK1-CK3 are terminated.
128	CKE0	Input	Clock Enable: CKE0 activates (HIGH) and deactivates (LOW) the CK0 signal. Deactivating the clock provides POWER-DOWN and SELF REFRESH operation (all banks idle) or CLOCK SUSPEND operation (burst access in progress). CKE0 is synchronous except after the device enters power-down and self refresh modes, where CKE0 becomes asynchronous until after exiting the same mode. The input buffers, including CK0, are disabled during power-down and self refresh modes, providing low standby power.
30, 45	S0#, S2#	Input	Chip Select: S0#, S2# enable (registered LOW) and disable (registered HIGH) the command decoder. All commands are masked when S0#, S2# are registered HIGH. S0#, S2# are considered part of the command code.
28-29, 46-47, 112-113, 130-131	DQMB0-DQMB7	Input	Input/Output Mask: DQMB is an input mask signal for write accesses and an output enable signal for read accesses. Input data is masked when DQMB is sampled HIGH during a WRITE cycle. The output buffers are placed in a High-Z state (two-clock latency) when DQMB is sampled HIGH during a READ cycle.
122, 39	BA0, BA1	Input	Bank Address: BA0 and BA1 define to which bank the ACTIVE, READ, WRITE or PRECHARGE command is being applied.
33, 34, 35, 36, 37, 38, 117, 118, 119, 120, 121, 123	A0-A11	Input	Address Inputs: A0-A12 are sampled during the ACTIVE command (row-address A0-A12) and READ/WRITE command (column-address A0-A9/A11, with A10 defining auto precharge) to select one location out of the memory array in the respective bank. A10 is sampled during a PRECHARGE command to determine if both banks are to be precharged (A10 HIGH). The address inputs also provide the op-code during a LOAD MODE REGISTER command.
81	WP	Input	Write Protect: Serial presence-detect hardware write protect.
83	SCL	Input	Serial Clock for Presence-Detect: SCL is used to synchronize the presence-detect data transfer to and from the module.
165-167	SA0-SA2	Input	Presence-Detect Address Inputs: These pins are used to configure the presence-detect device.
147	REGE	Input	Register Enable.
2-5, 7-11, 13-17, 19-20, 55-58, 60, 65-67, 69-72, 74-77, 86-89, 91-95, 97-101, 103-104, 139-142, 144, 149-151, 153-156, 158-161	DQ0-DQ63	Input/ Output	Data I/Os: Data bus.
21-22, 52-53, 105-106, 136-137	CB0-CB7	Input/ Output	Check Bits.

PIN DESCRIPTIONS (continued)

PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
82	SDA	Input/ Output	Serial Presence-Detect Data: SDA is a bidirectional pin used to transfer addresses and data into and data out of the presence-detect portion of the module.
6, 18, 26, 40-41, 49, 59, 73, 84, 90, 102, 110, 124, 133, 143, 157, 168	V_{DD}	Supply	Power Supply: +3.3V ±0.3V.
1, 12, 23, 32, 43, 54, 64, 68, 78, 85, 96, 107, 116, 127, 138, 148, 152, 162	V_{SS}	Supply	Ground.
63, 114, 126, 129, 132	RFU	–	Reserved for Future Use: These pins are not connected on this module but are assigned pins on other SDRAM versions.
31, 44, 48	DNU	–	Do Not Use: These pins are not connected on this module but are assigned pins on the compatible DRAM version.

SERIAL PRESENCE-DETECT MATRIX

BYTE	DESCRIPTION	ENTRY (VERSION)	MT18LSDT1672	MT18LSDT3272	MT18LSDT6472
0	NUMBER OF BYTES USED BY MICRON	128	80	80	80
1	TOTAL NUMBER OF SPD MEMORY BYTES	256	08	08	08
2	MEMORY TYPE	SDRAM	04	04	04
3	NUMBER OF ROW ADDRESSES	12 or 13	0C	0C	0D
4	NUMBER OF COLUMN ADDRESSES	10 or 11	0A	0B	0B
5	NUMBER OF BANKS	1	01	01	01
6	MODULE DATA WIDTH	72	48	48	48
7	MODULE DATA WIDTH (continued)	0	00	00	00
8	MODULE VOLTAGE INTERFACE LEVELS	LVTTL	01	01	01
9	SDRAM CYCLE TIME, ^{t}CK (CAS LATENCY = 3)	7 (-13E) 7.5 (-133) 8 (-10E)	70 75 80	70 75 80	70 75 80
10	SDRAM ACCESS FROM CLOCK, ^{t}AC (CAS LATENCY = 3)	5.4 (-13E/-133) 6 (-10E)	54 60	54 60	54 60
11	MODULE CONFIGURATION TYPE	ECC	02	02	02
12	REFRESH RATE/TYPE	15.6µs/SELF	80	80	80
13	SDRAM WIDTH (PRIMARY SDRAM)	4	04	04	04
14	ERROR-CHECKING SDRAM DATA WIDTH	4	04	04	04
15	MIN. CLOCK DELAY FROM BACK-TO-BACK RANDOM COLUMN ADDRESSES, ^{t}CCD	1	01	01	01
16	BURST LENGTHS SUPPORTED	1, 2, 4, 8, PAGE	8F	8F	8F
17	NUMBER OF BANKS ON SDRAM DEVICE	4	04	04	04
18	CAS LATENCIES SUPPORTED	2, 3	06	06	06
19	CS LATENCY	0	01	01	01
20	WE LATENCY	0	01	01	01
21	SDRAM MODULE ATTRIBUTES	-13E/-133 -10E	1F 16	1F 16	1F 16
22	SDRAM DEVICE ATTRIBUTES: GENERAL	0E	0E	0E	0E
23	SDRAM CYCLE TIME, ^{t}CK (CAS LATENCY = 2)	7.5 (-13E) 10 (-133/-10E)	75 A0	75 A0	75 A0
24	SDRAM ACCESS FROM CLK, ^{t}AC (CAS LATENCY = 2)	5.4 (-13E) 6 (-10E)	75 60	75 60	75 60
25	SDRAM CYCLE TIME, ^{t}CK (CAS LATENCY = 1)	–	00	00	00
26	SDRAM ACCESS FROM CLK, ^{t}AC (CAS LATENCY = 1)	–	00	00	00
27	MINIMUM ROW PRECHARGE TIME, ^{t}RP	15 (-13E) 20 (-133/-10E)	0F 14	0F 14	0F 14
28	MINIMUM ROW ACTIVE TO ROW ACTIVE, ^{t}RRD	14 (-13E) 15 (-133) 20 (-10E)	0E 0F 14	0E 0F 14	0E 0F 14
29	MINIMUM RAS# TO CAS# DELAY, ^{t}RCD	15 (-13E) 20 (-133/-10E)	0F 14	0F 14	0F 14
30	MINIMUM RAS# PULSE WIDTH, ^{t}RAS	37 (-13E) 44 (-133) 50 (-10E)	25 2C 32	25 2C 32	25 2C 32
31	MODULE BANK DENSITY	128MB/256MB/512MB	20	40	80

NOTE: 1. "1"/"0": Serial Data, "driven to HIGH"/"driven to LOW."

SERIAL PRESENCE-DETECT MATRIX (continued)

BYTE	DESCRIPTION	ENTRY (VERSION)	MT18LSDT1672	MT18LSDT3272	MT18LSDT6472
32	COMMAND AND ADDRESS SETUP TIME, ^{t}AS, ^{t}CMS	1.5 (-13E/-133) 2 (-10E)	15 20	15 20	15 20
33	COMMAND AND ADDRESS HOLD TIME, ^{t}AH, ^{t}CMH	0.8 (--13E/133) 1 (-10E)	08 10	08 10	08 10
34	DATA SIGNAL INPUT SETUP TIME, ^{t}DS	1.5 (-13E/-133) 2 (-10E)	15 20	15 20	15 20
35	DATA SIGNAL INPUT HOLD TIME, ^{t}DH	0.8 (-13E/-133) 1 (-10E)	08 10	08 10	08 10
36-61	RESERVED		00	00	00
62	SPD REVISION	REV. 1.2	12	12	12
63	CHECKSUM FOR BYTES 0-62	-13E -133 -10E	80 CE 16	A1 EF 37	0C 39 78
64	MANUFACTURER'S JEDEC ID CODE	MICRON	2C	2C	2C
65-71	MANUFACTURER'S JEDEC ID CODE (CONT.)		FF	FF	FF
72	MANUFACTURING LOCATION		01 02 03 04 05 06 07 08 09	01 02 03 04 05 06 07 08 09	01 02 03 04 05 06 07 08 09
73-90	MODULE PART NUMBER (ASCII)		xx	xx	xx
91	PCB IDENTIFICATION CODE	1 2 3 4 5 6 7 8 9	01 02 03 04 05 06 07 08 09	01 02 03 04 05 06 07 08 09	01 02 03 04 05 06 07 08 09
92	IDENTIFICATION CODE (CONT.)	0	00	00	00
93	YEAR OF MANUFACTURE IN BCD		xx	xx	xx
94	WEEK OF MANUFACTURE IN BCD		xx	xx	xx
95-98	MODULE SERIAL NUMBER		xx	xx	xx
99-125	MANUFACTURER-SPECIFIC DATA (RSVD)		–	–	–
126	SYSTEM FREQUENCY	100/133 MHz	64	64	64
127	SDRAM COMPONENT AND CLOCK DETAIL		8F	8F	8F

NOTE: 1. "1"/"0": Serial Data, "driven to HIGH"/"driven to LOW."
2. x = Variable Data.

Commands

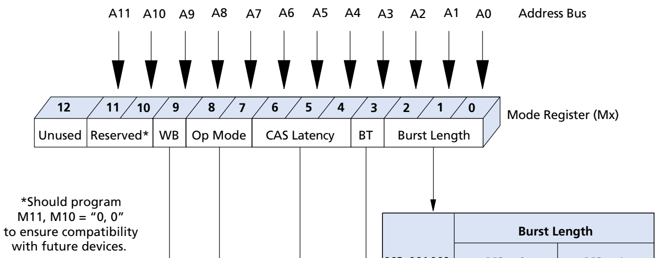
Truth Table 1 provides a quick reference of available commands. This is followed by a written description of each command. For a more detailed description of commands and operations refer to the 64Mb, 128Mb, 256Mb x4, x8, x16 SDRAM datasheets.

TRUTH TABLE 1 – COMMANDS AND DQMB OPERATION

(Note: 1)

NAME (FUNCTION)	CS#	RAS#	CAS#	WE#	DQMB	ADDR	DQs	NOTES
COMMAND INHIBIT (NOP)	H	X	X	X	X	X	X	
NO OPERATION (NOP)	L	H	H	H	X	X	X	
ACTIVE (Select bank and activate row)	L	L	H	H	X	Bank/Row	X	3
READ (Select bank and column, and start READ burst)	L	H	L	H	L/H[8]	Bank/Col	X	4
WRITE (Select bank and column, and start WRITE burst)	L	H	L	L	L/H[8]	Bank/Col	Valid	4
BURST TERMINATE	L	H	H	L	X	X	Active	
PRECHARGE (Deactivate row in bank or banks)	L	L	H	L	X	Code	X	5
AUTO REFRESH or SELF REFRESH (Enter self refresh mode)	L	L	L	H	X	X	X	6, 7
LOAD MODE REGISTER	L	L	L	L	X	Op-Code	X	2
Write Enable/Output Enable	–	–	–	–	L	–	Active	8
Write Inhibit/Output High-Z	–	–	–	–	H	–	High-Z	8

NOTE:
1. CKE is HIGH for all commands shown except SELF REFRESH.
2. A0-A12 define the op-code written to the Mode Register.
3. A0-A12 provide row address, and BA0, BA1 determine which bank is made active.
4. A0-A9/A11 provide column address; A10 HIGH enables the auto precharge feature (nonpersistent), while A10 LOW disables the auto precharge feature; BA0, BA1 determine which bank is being read from or written to.
5. A10 LOW: BA0, BA1 determine which bank is being precharged. A10 HIGH: both banks are precharged and BA0, BA1 are "Don't Care."
6. This command is AUTO REFRESH if CKE is HIGH, SELF REFRESH if CKE is LOW.
7. Internal refresh counter controls row addressing; all inputs and I/Os are "Don't Care" except for CKE.
8. Activates or deactivates the DQs during WRITEs (zero-clock delay) and READs (two-clock delay).



M2 M1 M0	Burst Length M3 = 0	Burst Length M3 = 1
0 0 0	1	1
0 0 1	2	2
0 1 0	4	4
0 1 1	8	8
1 0 0	Reserved	Reserved
1 0 1	Reserved	Reserved
1 1 0	Reserved	Reserved
1 1 1	Full Page	Reserved

M3	Burst Type
0	Sequential
1	Interleaved

M6 M5 M4	CAS Latency
0 0 0	Reserved
0 1 0	2
0 1 1	3
1 0 0	Reserved
1 0 1	Reserved
1 1 0	Reserved
1 1 1	Reserved

M8	M7	M6-M0	Operating Mode
0	0	Defined	Standard Operation
-	-	-	All other states reserved

M9	Write Burst Mode
0	Programmed Burst Length
1	Single Location Access

Figure 4
Mode Register Definition

Table 1
Burst Definition

Burst Length	Starting Column Address	Order of Accesses Within a Burst Type=Sequential	Order of Accesses Within a Burst Type=Interleaved
2	A0		
	0	0-1	0-1
	1	1-0	1-0
4	A1 A0		
	0 0	0-1-2-3	0-1-2-3
	0 1	1-2-3-0	1-0-3-2
	1 0	2-3-0-1	2-3-0-1
	1 1	3-0-1-2	3-2-1-0
8	A2 A1 A0		
	0 0 0	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7
	0 0 1	1-2-3-4-5-6-7-0	1-0-3-2-5-4-7-6
	0 1 0	2-3-4-5-6-7-0-1	2-3-0-1-6-7-4-5
	0 1 1	3-4-5-6-7-0-1-2	3-2-1-0-7-6-5-4
	1 0 0	4-5-6-7-0-1-2-3	4-5-6-7-0-1-2-3
	1 0 1	5-6-7-0-1-2-3-4	5-4-7-6-1-0-3-2
	1 1 0	6-7-0-1-2-3-4-5	6-7-4-5-2-3-0-1
	1 1 1	7-0-1-2-3-4-5-6	7-6-5-4-3-2-1-0
Full Page (y)	n = A0-A9/A11 (location 0-y)	Cn, Cn+1, Cn+2 Cn+3, Cn+4... ...Cn-1, Cn...	Not supported

NOTE:
1. For full-page accesses: y= 2048 (256MB/512MB), y = 1,024 (128MB).
2. For a burst length of two, A1-A9/A11 select the block of two burst; A0 selects the starting column within the block.
3. For a burst length of four, A2-A9/A11 select the block of four burst; A0-A1 select the starting column within the block.
4. For a burst length of eight, A3-A9/A11 select the block of eight burst; A0-A2 select the starting column within the block.
5. For a full-page burst, the full row is selected and A0-/A9/A11 select the starting column.
6. Whenever a boundary of the block is reached within a given sequence above, the following access wraps within the block.
7. For a burst length of one, A0-A9/A11 select the unique column to be accessed, and Mode Register bit M3 is ignored.

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{DD} Supply Relative to V_{SS} . -1V to +4.6V
Voltage on Inputs, NC or I/O Pins
Relative to V_{SS} .... -1V to +4.6V
Operating Temperature, T_A (ambient) ... 0°C to +70°C
Storage Temperature (plastic) .... -55°C to +125°C
Power Dissipation 18W

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS AND OPERATING CONDITIONS

(Notes: 1, 2) (V_{DD} = +3.3V ±0.3V)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
SUPPLY VOLTAGE	V_{DD}	3	3.6	V	
INPUT HIGH VOLTAGE: Logic 1; All inputs	V_{IH}	2	V_{DD} + 0.3	V	3
INPUT LOW VOLTAGE: Logic 0; All inputs	V_{IL}	-0.5	0.8	V	3
INPUT LEAKAGE CURRENT: Any input 0V ≤ V_{IN} ≤ V_{DD} (All other pins not under test = 0V)	I_{I1}	-5	5	µA	4
OUTPUT LEAKAGE CURRENT: DQs are disabled; 0V ≤ V_{OUT} ≤ V_{DD}	I_{OZ}	-5	5	µA	
OUTPUT LEVELS: Output High Voltage (I_{OUT} = -4mA)	V_{OH}	2.4	–	V	
Output Low Voltage (I_{OUT} = 4mA)	V_{OL}	–	0.4	V	

NOTE:
1. All voltages referenced to V_{SS}.
2. An initial pause of 100µs is required after power-up, followed by two AUTO REFRESH commands, before proper device operation is ensured. The two AUTO REFRESH command wake-ups should be repeated any time the ^{t}REF refresh requirement is exceeded.
3. V_{IH} overshoot: V_{IH} (MAX) = V_{DD} + 2V for a pulse width ≤ 10ns, and the pulse width cannot be greater than one third of the cycle rate. V_{IL} undershoot: V_{IL} (MIN) = -2V for a pulse width ≤ 10ns, and the pulse width cannot be greater than one third of the cycle rate.
4. Input leakage values based on register electrical characteristics, V_{DD} = 3.6V.

I_{DD} SPECIFICATIONS AND CONDITIONS

(Notes: 1, 2, 3, 4) (V_{DD} = +3.3V ±0.3V)

PARAMETER/CONDITION		SYMBOL	SIZE	MAX -13E	MAX -133	MAX -10E	UNITS	NOTES
OPERATING CURRENT: Active Mode; Burst = 2; READ or WRITE; ${}^tRC$ = ${}^tRC$ (MIN); CAS latency = 3		I_{DD1}	128MB	2,250	2,070	1,710	mA	5, 6, 7, 8
			256MB	2,880	2,700	2,520		
			512MB	TBD	TBD	TBD		
STANDBY CURRENT: Power-Down Mode; CKE = LOW; All banks idle		I_{DD2}	128MB	36	36	36	mA	8
			256MB	36	36	36		
			512MB	36	36	36		
STANDBY CURRENT: Active Mode; S0#, S2# = HIGH; CKE = HIGH;All banks active after ${}^tRCD$ met; No accesses in progress		I_{DD3}	128MB	810	810	630	mA	5, 7, 8, 9
			256MB	900	900	720		
			512MB	990	900	720		
OPERATING CURRENT: Burst Mode; Continuous burst; READ or WRITE; All banks active; CAS latency = 3		I_{DD4}	128MB	2,700	2,520	2,160	mA	5, 6, 7, 8
			256MB	2,970	2,700	2,520		
			512MB	TBD	TBD	TBD		
AUTO REFRESH CURRENT: CKE = HIGH; S0#, S2# = HIGH	${}^tRC$ = ${}^tRC$ (MIN); CL = 3	I_{DD5}	128MB	4,140	3,780	3,420	mA	5, 6, 7, 8, 9, 11
			256MB	5,940	5,580	4,860		
			512MB	TBD	TBD	TBD		
	${}^tRC$ = 15.625µs; CL = 3	I_{DD6}	128MB	54	54	54	mA	
			256MB	54	54	54		
			512MB	72	72	72		
SELF REFRESH CURRENT: CKE ≤ 0.2V		I_{DD7}	128MB	18	18	18	mA	10
			256MB	36	36	36		
			512MB	TBD	72	72		

NOTE:
1. All voltages referenced to V_{SS}.
2. An initial pause of 100µs is required after power-up, followed by two AUTO REFRESH commands, before proper device operation is ensured. The two AUTO REFRESH command wake-ups should be repeated any time the ${}^tREF$ refresh requirement is exceeded.
3. AC timing and I_{DD} test have V_{IL} = 0V and V_{IH} = 3V, with timing referenced to 1.5V crossover point. If the input transition time is longer than 1ns, then the timing is referenced at V_{IL} (MAX) and V_{IL} (MIN) and no longer at the 1.5V crossover point.
4. I_{DD} specifications are tested after the device is properly initialized.
5. I_{DD} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
6. The I_{DD} current will decrease as the CAS latency is reduced. This is due to the fact that the maximum cycle rate is slower as the CAS latency is reduced.
7. Address transitions average one transition every two clocks.
8. ${}^tCK$ = 7ns for -13E; ${}^tCK$ = 7.5ns for -133; ${}^tCK$ = 10ns for -10E.
9. Other input signals are allowed to transition no more than once every two clocks and are otherwise at valid V_{IH} or V_{IL} levels.
10. Enables on-chip refresh and address counters.
11. CKE is HIGH during refresh command period ${}^tRFC$ [MIN] else CKE is LOW. The I_{DD6} limit is actually a nominal value and does not result in a fail value.

CAPACITANCE

(Note: 1; notes appear on next page)

PARAMETER	SYMBOL	MAX	UNITS
Input Capacitance: A0-A11, BA0, BA1, RAS#, CAS#, WE#	C_{I1}	8	pF
Input Capacitance: S0#, S2#, CKE0, DQMB0#-DQMB7#	C_{I2}	8	pF
Input Capacitance: CK0	C_{I3}	6	pF
Input Capacitance: REGE	C_{I4}	5	pF
Input Capacitance: SCL, SA0-SA2, WP	C_{I5}	12	pF
Input/Output Capacitance: DQ0-DQ63, CB0-CB7, SDA	C_{IO}	8	pF

SDRAM COMPONENT* AC ELECTRICAL CHARACTERISTICS

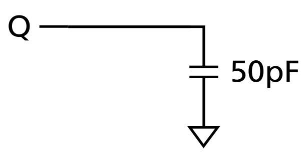
(Notes: 2, 3, 4, 5, 6, 7)

AC CHARACTERISTICS			-13E		-133		-10E			
PARAMETER		SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Access time from CLK	CL = 3	^{t}AC		5.4		5.4		6	ns	8
(positive edge)	CL = 2	^{t}AC		5.4		6		6	ns	
Address hold time		^{t}AH	0.8		0.8		1		ns	
Address setup time		^{t}AS	1.5		1.5		2		ns	
CLK high level width		^{t}CH	2.5		2.5		3		ns	
CLK low level width		^{t}CL	2.5		2.5		3		ns	
Clock cycle time	CL = 3	^{t}CK	7		7.5		8		ns	9
	CL = 2	^{t}CK	7.5		10		10		ns	9
CKE hold time		^{t}CKH	0.8		0.8		1		ns	
CKE setup time		^{t}CKS	1.5		1.5		2		ns	
CS#, RAS#, CAS#, WE#, DQM hold time			^{t}CMH	0.8		0.8		1	ns	
CS#, RAS#, CAS#, WE#, DQM setup time			^{t}CMS	1.5		1.5		2	ns	
Data-in hold time		^{t}DH	0.8		0.8		1		ns	
Data-in setup time		^{t}DS	1.5		1.5		2		ns	
Data-out high-impedance time	CL = 3	^{t}HZ		5.4		5.4		6	ns	10
	CL = 2	^{t}HZ		5.4		6		6	ns	10
Data-out low-impedance time		^{t}LZ	1		1		1		ns	
Data-out hold time (load)		^{t}OH	2.7		2.7		3		ns	
Data-out hold time (no load)		$^{t}OH_{N}$	1.8		1.8		1.8		ns	11
ACTIVE to PRECHARGE command		^{t}RAS	37	120,000	44	120,000	50	120,000	ns	
ACTIVE to ACTIVE command period		^{t}RC	60		66		70		ns	
ACTIVE to READ or WRITE delay		^{t}RCD	15		20		20		ns	
Refresh period (4,096 cycles)		^{t}REF		64		64		64	ms	
AUTO REFRESH PERIOD		^{t}RFC	66		66		70		ns	
PRECHARGE command period		^{t}RP	15		20		20		ns	
ACTIVE bank A to ACTIVE bank B command			^{t}RRD	14		15		20	ns	
Transition time		^{t}T	0.3	1.2	0.3	1.2	0.3	1.2	ns	12
WRITE recovery time		^{t}WR	1 CLK + 7ns		1 CLK + 7.5ns		1 CLK + 7ns		–	13
			14		15		15		ns	14
Exit SELF REFRESH to ACTIVE command			^{t}XSR	67		75		80	ns	

*Specifications for the SDRAM components used on the module.

NOTE:

1. This parameter is sampled. V_{DD} = +3.3V; f = 1 MHz.
2. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ +70°C) is ensured.
3. An initial pause of 100µs is required after power-up, followed by two AUTO REFRESH commands, before proper device operation is ensured. The two AUTO REFRESH command wake-ups should be repeated any time the ^{t}REF refresh requirement is exceeded.
4. AC characteristics assume ^{t}T = 1ns.
5. In addition to meeting the transition rate specification, the clock and CKE must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
6. Outputs measured at 1.5V with equivalent load:



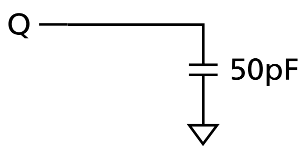
7. ^{t}HZ defines the time at which the output achieves the open circuit condition; it is not a reference to V_{OH} or V_{OL}. The last valid data element will meet ^{t}OH before going High-Z.
8. AC timing and I_{DD} test have V_{IL} = 0V and V_{IH} = 3V, with timing referenced to 1.5V crossover point. If the input transition time is longer than 1ns, then the timing is referenced at V_{IL} (MAX) and V_{IL} (MIN) and no longer at the 1.5V crossover point.
9. There will be an added one-clock latency at the system level due to the register requiring an added clock cycle.
10. Auto precharge mode only. The precharge timing budget (^{t}RP) begins 7.5ns/7ns after the first clock delay, after the last WRITE is executed.
11. Precharge mode only.
12. The clock frequency must remain constant (stable clock is defined as a signal cycling within timing constraints specified for the clock pin) during access or precharge states (READ, WRITE, including ^{t}WR, and PRECHARGE commands). CKE may be used to reduce the data rate.
13. ^{t}AC for -133 at CL = 3 with no load is 4.6ns and is guaranteed by design.
14. Parameter guaranteed by design.

AC FUNCTIONAL CHARACTERISTICS

(Notes: 1, 2, 3, 4, 5, 6, 7)

PARAMETER		SYMBOL	-133	-13E/-10E	UNITS	NOTES
READ/WRITE command to READ/WRITE command		^{t}CCD	1	1	^{t}CK	8
CKE to clock disable or power-down entry mode		^{t}CKED	1	1	^{t}CK	9
CKE to clock enable or power-down exit setup mode		^{t}PED	1	1	^{t}CK	9
DQM to input data delay		^{t}DQD	0	0	^{t}CK	8
DQM to data mask during WRITEs		^{t}DQM	0	0	^{t}CK	8
DQM to data high-impedance during READs		^{t}DQZ	2	2	^{t}CK	8
WRITE command to input data delay		^{t}DWD	0	0	^{t}CK	8
Data-in to ACTIVE command		^{t}DAL	5	4	^{t}CK	10, 11
Data-in to PRECHARGE command		^{t}DPL	2	2	^{t}CK	11, 12
Last data-in to burst STOP command		^{t}BDL	1	1	^{t}CK	8
Last data-in to new READ/WRITE command		^{t}CDL	1	1	^{t}CK	8
Last data-in to PRECHARGE command		^{t}RDL	2	2	^{t}CK	11, 12
LOAD MODE REGISTER command to ACTIVE or REFRESH command		^{t}MRD	2	2	^{t}CK	13
Data-out to high-impedance from PRECHARGE command	CL = 3	^{t}ROH	3	3	^{t}CK	8
	CL = 2	^{t}ROH	2	2	^{t}CK	8

NOTE:
1. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \le T_A \le +70°C$) is ensured.
2. An initial pause of 100µs is required after power-up, followed by two AUTO REFRESH commands, before proper device operation is ensured. The two AUTO REFRESH command wake-ups should be repeated any time the ^{t}REF refresh requirement is exceeded.
3. AC characteristics assume ^{t}T = 1ns.
4. In addition to meeting the transition rate specification, the clock and CKE must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
5. Outputs measured at 1.5V with equivalent load:



6. AC timing and I_{DD} test have V_{IL} = 0V and V_{IH} = 3V, with timing referenced to 1.5V crossover point. If the input transition time is longer than 1ns, then the timing is referenced at V_{IL} (MAX) and V_{IL} (MIN) and no longer at the 1.5V crossover point.
7. There will be an added one-clock latency at the system level due to the register requiring an added clock cycle.
8. Required clocks are specified by JEDEC functionality and are not dependent on any timing parameter.
9. Timing actually specified by ^{t}CKS; clock(s) specified as a reference only at minimum cycle rate.
10. Timing actually specified by ^{t}WR plus ^{t}RP; clock(s) specified as a reference only at minimum cycle rate.
11. Based on ^{t}CK = 143 MHz for -13E, ^{t}CK = 133 MHz for -133, 100 MHz for -10E.
12. Timing actually specified by ^{t}WR.
13. JEDEC and PC100 specify three clocks.

SERIAL PRESENCE-DETECT EEPROM DC OPERATING CONDITIONS

(Note: 1) (V_{DD} = +3.3V ±0.3V)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS
SUPPLY VOLTAGE	V_{DD}	3	3.6	V
INPUT HIGH VOLTAGE: Logic 1; All inputs	V_{IH}	V_{DD} x 0.7	V_{DD} + 0.5	V
INPUT LOW VOLTAGE: Logic 0; All inputs	V_{IL}	-1	V_{DD} x 0.3	V
OUTPUT LOW VOLTAGE: I_{OUT} = 3mA	V_{OL}	–	0.4	V
INPUT LEAKAGE CURRENT: V_{IN} = GND to V_{DD}	I_{LI}	–	10	µA
OUTPUT LEAKAGE CURRENT: V_{OUT} = GND to V_{DD}	I_{LO}	–	10	µA
STANDBY CURRENT: SCL = SDA = V_{DD} - 0.3V; All other inputs = GND or 3.3V +10%	I_{SB}	–	30	µA
POWER SUPPLY CURRENT: SCL clock frequency = 100 KHz	I_{DD}	–	2	mA

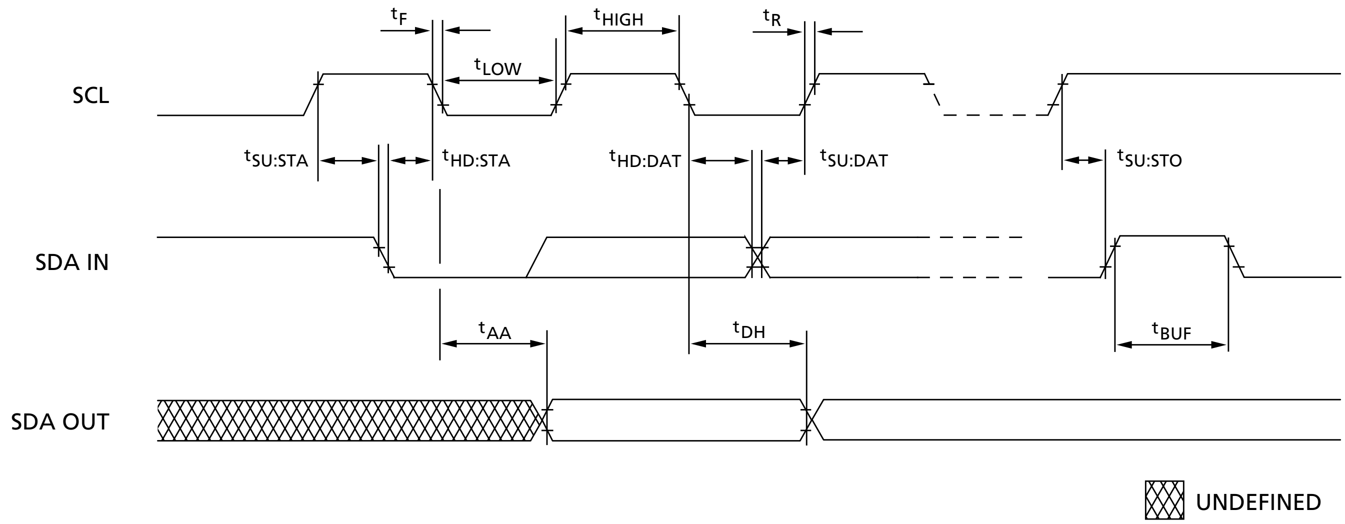
SERIAL PRESENCE-DETECT EEPROM AC OPERATING CONDITIONS

(Note: 1) (V_{DD} = +3.3V ±0.3V)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
SCL LOW to SDA data-out valid	^tAA	0.3	3.5	µs	
Time the bus must be free before a new transition can start	^tBUF	4.7		µs	
Data-out hold time	^tDH	300		ns	
SDA and SCL fall time	^tF		300	ns	
Data-in hold time	$^tHD:DAT$	0		µs	
Start condition hold time	$^tHD:STA$	4		µs	
Clock HIGH period	^tHIGH	4		µs	
Noise suppression time constant at SCL, SDA inputs	^tI		100	ns	
Clock LOW period	^tLOW	4.7		µs	
SDA and SCL rise time	^tR		1	µs	
SCL clock frequency	^tSCL		100	KHz	
Data-in setup time	$^tSU:DAT$	250		ns	
Start condition setup time	$^tSU:STA$	4.7		µs	
Stop condition setup time	$^tSU:STO$	4.7		µs	
WRITE cycle time	^tWRC		10	ms	2

NOTE:
1. All voltages referenced to V_{SS}.
2. The SPD EEPROM WRITE cycle time (^tWRC) is the time from a valid stop condition of a write sequence to the end of the EEPROM internal erase/program cycle. During the WRITE cycle, the EEPROM bus interface circuit is disabled, SDA remains HIGH due to pull-up resistor, and the EEPROM does not respond to its slave address.

SPD EEPROM



SERIAL PRESENCE-DETECT EEPROM TIMING PARAMETERS

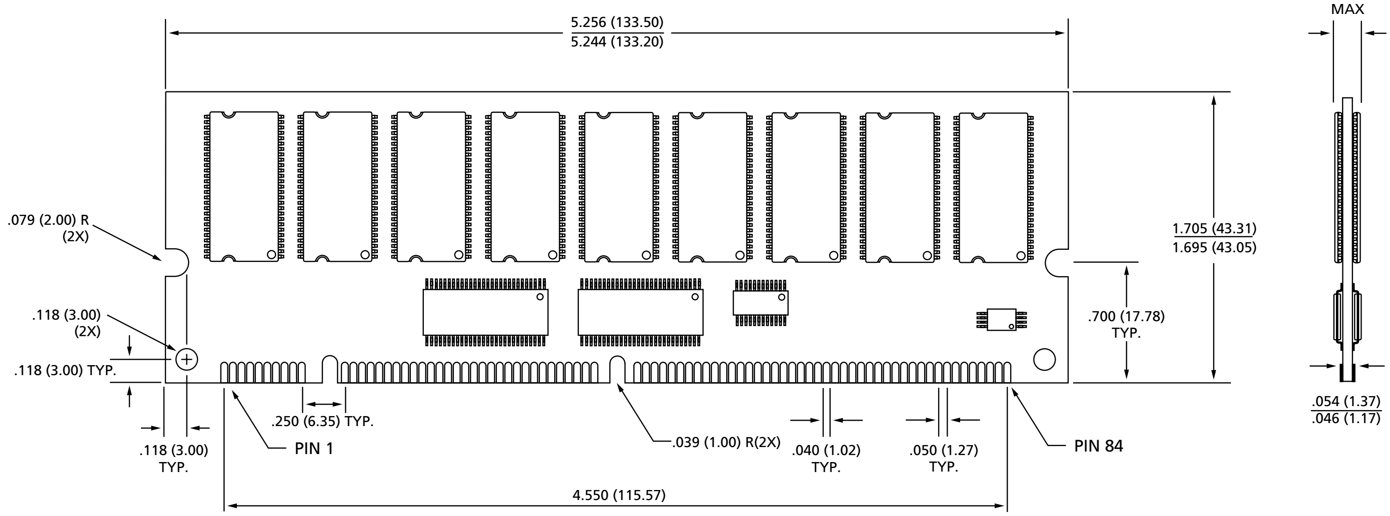
SYMBOL	MIN	MAX	UNITS
^{t}AA	0.3	3.5	µs
^{t}BUF	4.7		µs
^{t}DH	300		ns
^{t}F		300	ns
^{t}HD:DAT	0		µs
^{t}HD:STA	4		µs

SYMBOL	MIN	MAX	UNITS
^{t}HIGH	4		µs
^{t}LOW	4.7		µs
^{t}R		1	µs
^{t}SU:DAT	250		ns
^{t}SU:STA	4.7		µs
^{t}SU:STO	4.7		µs

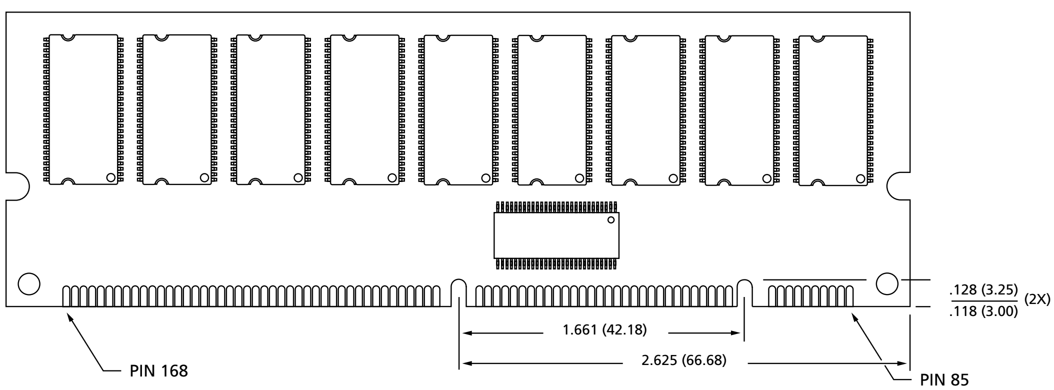
168-PIN DIMM

(128MB/256MB/512MB)

FRONT VIEW



BACK VIEW



NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

8000 S. Federal Way, P.O. Box 6, Boise, ID 83707-0006, Tel: 208-368-3900
E-mail: prodmktg@micron.com, Internet: http://www.micron.com, Customer Comment Line: 800-932-4992

Micron Memory DRAM Module Reference Guide

Density	Description		Pins	Components on Module			Part Number	Speed	Height	Availability	
										Samples	Prod.
4MB	SS	1 Meg x 32 Gold SIMM/Tin SIMM	72	(2)	1 Meg x 16		MT2D132G/M (X)	50,60	.800"	Now	Now
4MB	SS	1 Meg x 32 3.3V Gold SODIMM	72	(2)	1 Meg x 16	3.3V TSOP	MT2LDT132HG (X)	60	1.000"	Now	Now
4MB	SS	1 Meg x 32 3.3V Gold DIMM	100	(2)	1 Meg x 16	3.3V TSOP	MT2LD132UG (X)	60	1.000"	Now	Now
8MB	DS	2 Meg x 32 Gold SIMM/Tin SIMM	72	(4)	1 Meg x 16		MT4D232DG/M (X)	50,60	.800"	Now	Now
8MB	SS	2 Meg x 32 3.3V Gold SODIMM	72	(4)	1 Meg x 16	3.3V TSOP	MT4LDT232HG (X)	60	1.000"	Now	Now
8MB	SS	2 Meg x 32 3.3V Gold DIMM	100	(4)	1 Meg x 16	3.3V	MT4LD232UG (X)	60	1.000"	Now	Now
8MB	SS	1 Meg x 64 3.3V Gold SODIMM	144	(4)	1 Meg x 16	3.3V TSOP	MT4LDT164HG (X)	60	1.000"	Now	Now
8MB	DS	1 Meg x 64 3.3V Gold DIMM	168	(4)	1 Meg x 16	3.3V TSOP	MT4LDT164AG (X)	60	1.000"	Now	Now
16MB	SS	4 Meg x 32 Gold SIMM/Tin SIMM	72	(8)	4 Meg x 4		MT8D432G/M (X)	50, 60	1.000"	Now	Now
16MB	SS	4 Meg x 36 ECC Gold SIMM/Tin SIMM	72	(9)	4 Meg x 4		MT9D436G/M (X)	50, 60	1.000"	Now	Now
16MB	DS	4 Meg x 32 3.3V Gold SODIMM	72	(8)	4 Meg x 4	3.3V TSOP	MT8LDT432HG (X)	60	1.000"	Now	Now
16MB	SS	4 Meg x 32 3.3V Gold SODIMM	72	(2)	4 Meg x 16	3.3V TSOP	MT2LDT432HG (X)	60	1.000"	Now	Now
16MB	SS	4 Meg x 32 3.3V Gold DIMM	100	(2)	4 Meg x 16	3.3V TSOP	MT2LDT432UG (X)	60	1.000"	Now	Now
32MB	DS	8 Meg x 32 Gold SIMM/Tin SIMM	72	(16)	4 Meg x 4		MT16D832G/M (X)	50, 60	1.000"	Now	Now
32MB	DS	8 Meg x 36 ECC Gold SIMM/Tin SIMM	72	(18)	4 Meg x 4		MT18D836G/M (X)	50, 60	1.000"	Now	Now
32MB	DS	8 Meg x 32 3.3V Gold SODIMM	72	(4)	4 Meg x 16	3.3V TSOP	MT4LDT832HG (X)	60	1.000"	Now	Now
32MB	DS	8 Meg x 32 3.3V Gold DIMM	100	(4)	4 Meg x 16	3.3V TSOP	MT4LDT832UG (X)	60	1.000"	Now	Now
32MB	DS	4 Meg x 64 3.3V Gold SODIMM	144	(4)	4 Meg x 16	3.3V TSOP	MT4LDT464HG (X)(S)	50,60	1.000"	Now	Now
32MB	SS	4 Meg x 64 3.3V Gold DIMM	168	(4)	4 Meg x 16	3.3V TSOP	MT4LDT464AG (X)	50,60	1.000"	Now	Now
32MB	DS	4 Meg x 64 3.3V Gold DIMM	168	(16)	4 Meg x 4	3.3V	MT16LD464AG (X)	60	1.000"	Now	Now
32MB	DS	4 Meg x 72 3.3V ECC Gold DIMM	168	(18)	4 Meg x 4	3.3V	MT18LD472(A)G (X)	60	Unbuff = 1.000", Buff = 1.000"	Now	Now
32MB	SS	4 Meg x 72 3.3V ECC Gold DIMM	168	(5)	4 Meg x 16	3.3V TSOP	MT5LDT472(A)G (X)	60	Unbuff = 1.000", Buff = 1.050"	Now	Now
64MB	DS	8 Meg x 64 3.3V Gold SODIMM	144	(8)	8 Meg x 8	3.3V TSOP	MT8LDT864HG (X)(S)	60	1.050"	Now	Now
64MB	DS	8 Meg x 64 3.3V Gold DIMM	168	(32)	4 Meg x 4	3.3V	MT32LD864AG (X)	60	1.500"	Now	Now
64MB	SS	8 Meg x 64 3.3V Gold DIMM	168	(8)	8 Meg x 8	3.3V	MT8LD864AG (X)	50, 60	1.100"	Now	Now
64MB	DS	8 Meg x 72 3.3V ECC Gold DIMM	168	(36)	4 Meg x 4	3.3V	MT36LD872(A)G (X)	60	Unbuff = 1.500", Buff = 1.500"	Now	Now
64MB	SS	8 Meg x 72 3.3V ECC Gold DIMM	168	(9)	8 Meg x 8	3.3V	MT9LD872(A)G (X)	50, 60	Unbuff = 1.100", Buff = 1.250"	Now	Now
64MB	SS	8 Meg x 72 3.3V ECC Gold DIMM	168	(9)	8 Meg x 8	3.3V TSOP	MT9LDT872G (X)	50, 60	1.350"	Now	Now
128MB	DS	16 Meg x 64 3.3V Gold DIMM	168	(16)	16 Meg x 4	3.3V	MT16LD1664AG (X)	50,60	1.250"	Now	Now
128MB	DS	16 Meg x 72 3.3V ECC Gold DIMM	168	(18)	16 Meg x 4	3.3V	MT18LD1672(A)G (X)	50,60	Unbuff = 1.250", Buff = 1.100"	Now	Now
128MB	DS	16 Meg x 72 3.3V ECC Gold DIMM	168	(18)	16 Meg x 4	3.3V TSOP	MT18LDT1672G (X)	50,60	2.000"	Now	Now
256MB	DS	32 Meg x 72 3.3V ECC Gold DIMM	168	(36)	16 Meg x 4	3.3V	MT36LD3272G (X)	50, 60	2.000"	Now	Now
256MB	DS	32 Meg x 72 3.3V ECC Gold DIMM	168	(36)	16 Meg x 4	3.3V TSOP	MT36LDT3272G (X)	50, 60	2.000"	Now	Now

Rev. 3/26/01

SS - Single Sided **DS** - Double Sided **G** - Gold Plated **M** - Tin Plated **U** - 100-pin DIMM **(H)** - Small-Outline DIMM (SODIMM)
(X) - EDO; no "X" denotes FPM version **(A)** - 8-CAS; SPD version; unbuffered (no "A" denotes buffered version for x72 DIMMs) **(S)** - Self Refresh

Micron Memory SDRAM Module Reference Guide

												Availability		
Density	Description		Pins	Components on Module			Base Part Number	Speed	Die Rev.	PCB (height)	MHz*	Samples	Production	Notes
4MB	SS	1 Meg x 32 3.3V Gold DIMM	100	(2)	1 Meg x 16	3.3V TSOP	MT2LSDT132UG	-10E1	E = Y72G	1 = 6649 (1.000")	100	Now	Now	
								-8E1			125	Now	Now	
	SS	1 Meg x 32 AIMM		(2)	1 Meg x 16	3.3V TSOP	MT2LSDT132AGP	-6E2	E = Y72G	2 = 0164B (1.4")	133	Now	Now	AIMM
	SS	1 Meg x 32 AIMM		(1)	2 Meg x 32	3.3V TSOP	MT1LSDT132AGP	-6E1	E = Y84W	1 = 0178 (1.4")	133	Now	Now	AIMM
8MB	DS	2 Meg x 32 3.3V Gold DIMM	100	(4)	1 Meg x 16	3.3V TSOP	MT4LSDT232UDG	-10E1	E = Y72G	1 = 6649 (1.000")	100	Now	Now	
								-8E1			125	Now	Now	
16MB	SS	4 Meg x 32 3.3V Gold DIMM	100	(2)	4 Meg x 16	3.3V TSOP	MT2LSDT432UG	-10C1	C = Y84	1 = 6660 (1.000")	100	Now	Now	
								-8C1			125	Now	Now	
32MB	DS	8 Meg x 32 3.3V Gold DIMM	100	(4)	4 Meg x 16	3.3V TSOP	MT4LSDT832UDG	-10C1	C = Y84	1 = 6660 (1.000")	100	Now	Now	
								-8C1			125	Now	Now	
32MB	DS	4 Meg x 64 3.3V Gold SODIMM	144*	(4)	4 Meg x 16	3.3V TSOP	MT4LSDT464HG	-662C1	C = Y84	1 = 6645 (1.150")	66	Now	Now	
								-662C2		2 = 6669 (1.000")	66	Now	Now	
								-10EC3		3 = 0118B (1.000")	100	Now	Now	PC100
								-10EC4		4 = 0180 (1.000")	100	Now	Now	PC100
								-133C4			133	Now	Now	PC133 rev 1.0
								-13EC4			133	Now	Now	PC133 rev 1.0
32MB	SS	4 Meg x 64 3.3V Gold DIMM	168	(4)	4 Meg x 16	3.3V TSOP	MT4LSDT464AG	-662C6	C = Y84	6 = 0134B (1.000")	66	Now	Now	
								-10CC6			100	Now	Now	
								-10EC6			100	Now	Now	
								-133C6			133	Now	Now	CL3
								-13EC6			133	Now	Now	CL2
32MB	SS	4 Meg x 72 3.3V ECC Gold DIMM	168*	(5)	4 Meg x 16	3.3V TSOP	MT5LSDT472AG	-662C6	C = Y84	6 = 0134B (1.000")	66	Now	Now	
								-10CC6			100	Now	Now	
								-10EC6			100	Now	Now	
								-133C6			133	Now	Now	CL3
								-13EC6			133	Now	Now	CL2
64MB	DS	16 Meg x 32 3.3V Gold DIMM	100	(4)	16 Meg x 8	3.3V TSOP	MT4LSDT1632UG	-10B1	B = Y85B	1 = 6692(1.15")	100	Now	Now	
								-8B1	E = Y95C		125	Now	Now	
								-10E1			100	Now	Now	
								-8E1			125	Now	Now	
				(4)	8 Meg x 16	3.3V TSOP	MT4LSDT1632UDG	-10B1	B = Y85B	1 = 6660(1.00")	100	Now	Now	
								-8B1	F = Y95W		125	Now	Now	
								-10F1			100	2Q01	3Q01	
								-8F1			125	2Q01	3Q01	
64MB	DS	8 Meg x 64 3.3V Gold SODIMM	144*	(8)	8 Meg x 8	3.3V TSOP	MT8LSDT864HG	-662C3	C = Y84	3 = 6678 (1.050")	66	Now	Now	
				(8)	4 Meg x 16	3.3V TSOP		-10EC5		5 = 0115C (1.250")	100	Now	Now	PC100
64MB	DS	8 Meg x 64 3.3V Gold SODIMM	144*	(4)	8 Meg x 16	3.3V TSOP	MT4LSDT864HG	-662B1	B = Y85B	1 = 0118B (1.000")	66	Now	Now	
								-10EB1	F = Y95W	2 = 0180 (1.000")	100	Now	Now	PC100
								-10EB2			100	Now	Now	PC100
								-133B2			133	Now	Now	PC133 rev 1.0
								-13EB2			133	Now	Now	PC133 rev 1.0
								-10EF2			100	2Q01	3Q01	
								-133F2			133	2Q01	3Q01	
								-13EF2			133	2Q01	3Q01	
64MB	SS	8 Meg x 64 3.3V Gold DIMM	168	(8)	8 Meg x 8	3.3V TSOP	MT8LSDT864AG	-662C7	C = Y84	7 = 0104B (1.375")	66	Now	Now	
								-10CC7			100	Now	Now	
								-10EC7			100	Now	Now	
								-133C7			133	Now	Now	CL3
								-13EC7			133	Now	Now	CL2
64MB	SS	8 Meg x 64 3.3V Gold DIMM	168	(4)	8 Meg x 16	3.3V TSOP	MT4LSDT864AG	-662B1	B = Y85B	1 = 0134B (1.00")	66	Now	Now	
								-10CB1	F = Y95W		100	Now	Now	
								-10EB1			100	Now	Now	
								-133B1			133	Now	Now	CL3
								-13EB1			133	Now	Now	CL2
								-10EF1			100	2Q01	3Q01	
								-133F1			133	2Q01	3Q01	
								-13EF1			133	2Q01	3Q01	
	DS	8 Meg x 64 3.3V Gold DIMM	144	(4)	8 Meg x 16	3.3V TSOP	MT4LSDT864WG	-133F1	F = Y95W	1 = 0182 (1.18")	133	2Q01	3Q01	Micro DIMM
64MB	SS	8 Meg x 72 3.3V Gold DIMM	168	(5)	8 Meg x 16	3.3V TSOP	MT5LSDT872AG	-10EB1	B = Y85B	1 = 0134B (1.00")	100	Now	Now	
								-133B1	F = Y95W		133	Now	Now	CL3
								-13EB1			133	Now	Now	CL2
								-10EF1			100	2Q01	3Q01	
								-133F1			133	2Q01	3Q01	
								-13EF1			133	2Q01	3Q01	
64MB	SS	8 Meg x 72 3.3V ECC Gold DIMM	168	(9)	8 Meg x 8	3.3V TSOP	MT9LSDT872AG	-662C7	C = Y84	7 = 0104B (1.375")	66	Now	Now	
								-10CC7			100	Now	Now	
								-10EC7			100	Now	Now	
								-133C7			133	Now	Now	CL3
								-13EC7			133	Now	Now	CL2
64MB	SS	8 Meg x 72 3.3V ECC Gold DIMM	168	(9)	8 Meg x 8	3.3V TSOP	MT9LSDT872G	-10CC3	C = Y84	3 = 0144 (1.500")	100	Now	Now	
								-10EC3			100	Now	Now	
								-133C3			133	Now	Now	CL3
								-13EC3			133	Now	Now	CL2
128MB	DS	32 Meg x 32 3.3V Gold DIMM	100	(8)	16 Meg x 8	3.3V TSOP	MT8LSDT3232UG	-10B1	B = Y85B	1 = 6692 (1.15")	100	Now	Now	
								-8B1	E = Y95C		125	Now	Now	
								-10E1			100	Now	Now	
								-8E1			125	Now	Now	
				(8)	8 Meg x 16	3.3V TSOP	MT8LSDT3232UDG	-10B1	B = Y85B	1 = TBD (1.15")	100	TBD	TBD	
								-8B1	F = Y95W		125	TBD	TBD	
								-10F1			100	TBD	TBD	
								-8F1			125	TBD	TBD	
128MB	DS	16 Meg x 64 3.3V Gold SODIMM	144	(8)	8 Meg x 16	3.3V TSOP	MT8LSDT1664HG	-10CB1	B = Y85B	1 = 0115C (1.25")	100	Now	Now	PC100
								-10EB1	F = Y95W	2 = 6678 (1.050")	100	Now	Now	PC100
					16 Meg x 8	3.3V TSOP		-662B2		3 = 0179 (1.25")	66	Now	Now	
					8 Meg x 16	3.3V TSOP		-10EB3			100	Now	Now	PC100
								-133B3			133	Now	Now	PC133 rev 1.0
								-13EB3			133	Now	Now	PC133 rev 1.0
								-10EF3			100	2Q01	3Q01	
								-133F3			133	2Q01	3Q01	
								-13EF3			133	2Q01	3Q01	
128MB	DS	16 Meg x 64 3.3V Gold DIMM	168	(16)	8 Meg x 8	3.3V TSOP	MT16LSDT1664AG	-662C7	C = Y84	7 = 0104B(1.375")	66	Now	Now	
								-10CC7			100	Now	Now	
								-10EC7			100	Now	Now	
								-133C7			133	Now	Now	CL3
								-13EC7			133	Now	Now	CL2
128MB	DS	16 Meg x 64 3.3V Gold DIMM	168	(8)	16 Meg x 8	3.3V TSOP	MT8LSDT1664AG	-10CB1	B = Y85B	1 = 0104B(1.375")	100	Now	Now	
								-10EB1	E = Y95C		100	Now	Now	
								-133B1			133	Now	Now	CL3
								-13EB1			133	Now	Now	CL2
								-10EE1			100	Now	Now	
								-133E1			133	Now	Now	CL3
								-13EE1			133	Now	Now	CL2
	SS	16 Meg x 64 3.3V Gold DIMM	168	(4)	16 Meg x 16	3.3V TSOP	MT4LSDT1664AG	-10EB1	B = Y96	1 = TBD (1.00")	100	2Q01	3Q01	
								-133B1			133	2Q01	3Q01	
								-13EB1			133	TBD	TBD	
	DS	16 Meg x 64 3.3V Gold DIMM	144	(4)	16 Meg x 16	3.3V TSOP	MT4LSDT1664WG	-133B1	B = Y96	1 = 0182 (1.18")	133	2Q01	3Q01	Micro DIMM
	DS	16 Meg x 64 3.3V Gold DIMM	144	(4)	16 Meg x 16	3.3V TSOP	MT4LSDT1664HG	-10EB1	B = Y96	1 = 0180 (1.00")	100	2Q01	3Q01	
								-133B1			133	2Q01	3Q01	
								-13EB1			133	TBD	TBD	
128MB	DS	16 Meg x 72 3.3V ECC Gold DIMM	168	(18)	8 Meg x 8	3.3V TSOP	MT18LSDT1672AG	-662C7	C = Y84	7 = 0104B(1.375")	66	Now	Now	
								-10CC7			100	Now	Now	
								-10EC7			100	Now	Now	
								-133C7			133	Now	Now	CL3
								-13EC7			133	Now	Now	CL2
128MB	SS	16 Meg x 72 3.3V ECC Gold DIMM	168	(9)	16 Meg x 8	3.3V TSOP	MT9LSDT1672AG	-10CB1	B = Y85B	1 = 0104B(1.375")	100	Now	Now	
								-10EB1	E = Y95C		100	Now	Now	
								-133B1			133	Now	Now	CL3
								-13EB1			133	Now	Now	CL2
								-10EE1			100	Now	Now	
								-133E1			133	Now	Now	CL3
								-13EE1			133	Now	Now	CL2
	SS	16 Meg x 72 3.3V ECC Gold DIMM	168	(5)	32 Meg x 8	3.3V TSOP	MT5LSDT1672AG	-10EB1	B = Y96	1 = TBD (1.00")	100	2Q01	3Q01	
								-133B1			133	2Q01	3Q01	
								-13EB1			133	TBD	TBD	
			168	(9)	16 Meg x 8	3.3V TSOP	MT9LSDT1672G	-10CB1	B = Y85B	1 = 0144(1.500")	100	Now	Now	
								-10EB1	E = Y95C		100	Now	Now	
								-133B1		2 = 0198(1.125")	133	Now	Now	CL3

								-13EB1			133	Now	Now	CL2
								-10EE1			100	Now	Now	
								-133E1			133	Now	Now	CL3
								-13EE1			133	Now	Now	CL2
	DS							-10EE2			100	2Q01	3Q01	1U
								-133E2			133	2Q01	3Q01	1U
								-13EE2			133	2Q01	3Q01	1U
128MB	DS	16 Meg x 72 3.3V ECC Gold DIMM	168	(18)	16 Meg x 4	3.3V TSOP	MT18LSDT1672G	-10CC2	C = Y84	2 = 0129 (1.700")	100	Now	Now	
								-10EC2			100	Now	Now	
								-133C2			133	Now	Now	CL3
								-13EC2			133	Now	Now	CL2
256MB	DS	32 Meg x 64 3.3V Gold DIMM	168	(16)	16 Meg x 8	3.3V TSOP	MT16LSDT3264AG	-10CB1	B = Y85B	1 = 0104B (1.375")	100	Now	Now	
								-10EB1	E = Y95C		100	Now	Now	
								-133B1			133	Now	Now	CL3
								-13EB1			133	Now	Now	CL2
								-10EE1			100	Now	Now	
								-133E1			133	Now	Now	CL3
								-13EE1			133	Now	Now	CL2
	DS	32 Meg x 64 3.3V Gold SODIMM	144	(8)	16 Meg x 16	3.3V TSOP	MT8LSDT3264HG	-10EB1	B = Y96	1 = 0179 (1.25")	100	Now	Now	PC100
								-133B1			133	Now	Now	PC133 rev 1.0
	SS	32 Meg x 64 3.3V Gold DIMM	168	(8)	32 Meg x 8	3.3V TSOP	MT8LSDT3264AG	-10EB1	B = Y96	1 = TBD (1.375")	100	2Q01	3Q01	
								-133B1			133	2Q01	3Q01	
								-13EB1			133	TBD	TBD	
	DS	32 Meg x 64 3.3V Gold SODIMM	144	(8)	32 Meg x 8	3.3V fBGA	MT8LSDF3264WG	-133B1	B = Y96	1 = 0189 (1.25")	133	3Q01	4Q01	Micro DIMM
	DS	32 Meg x 64 3.3V Gold SODIMM	144	(16)	16 Meg x 8	3.3V fBGA	MT16LSDF3264HG	-10EB2	B = Y85B	2 = 0155 (1.25")	100	Now	Now	
								-133B2	E = Y95C	3 = 0185 (1.25")	133	Now	Now	
								-10EE3			100	2Q01	3Q01	
								-133E3			133	2Q01	3Q01	
256MB	DS	32 Meg x 72 3.3V ECC Gold DIMM	168	(18)	16 Meg x 8	3.3V TSOP	MT18LSDT3272AG	-10CB1	B = Y85B	1 = 0104B (1.375")	100	Now	Now	
								-10EB1	E = Y95C		100	Now	Now	
								-133B1			133	Now	Now	CL3
								-13EB1			133	Now	Now	CL2
								-10EE1			100	Now	Now	
								-133E1			133	Now	Now	CL3
								-13EE1			133	Now	Now	CL2
256MB	DS	32 Meg x 72 3.3V ECC Gold DIMM	168	(18)	32 Meg x 4	3.3V TSOP	MT18LSDT3272G	-10EB1	B = Y85B	1 = 0129 (1.700")	100	Now	Now	
								-133B1	E = Y95C		133	Now	Now	CL3
								-13EB1			133	Now	Now	CL2
								-10EE1			100	Now	Now	
								-133E1			133	Now	Now	CL3
								-13EE1			133	Now	Now	CL2
	DS	32 Meg x 72 3.3V ECC Gold DIMM	168	(18)	16 Meg x 8	3.3V TSOP	MT18LSDT3272DG	-10EB1	B = Y85B	1 = 0156 (1.7")	100	Now	Now	
								-133B1	E = Y95C		133	Now	Now	CL3
								-13EB1			133	Now	Now	CL2
								-10EE1			100	Now	Now	
								-133E1			133	Now	Now	CL3
								-13EE1			133	Now	Now	CL2
	SS	32 Meg x 72 3.3V ECC Gold DIMM	168	(9)	32 Meg x 8	3.3V TSOP	MT9LSDT3272AG	-10EB1	B = Y96	1 = TBD (1.375")	100	2Q01	3Q01	
								-133B1			133	2Q01	3Q01	
								-13EB1			133	TBD	TBD	
	SS	32 Meg x 72 3.3V ECC Gold DIMM	168	(9)	32 Meg x 8	3.3V TSOP	MT9LSDT3272G	-10EB1	B = Y96	1 = TBD (1.70")	100	2Q01	3Q01	
								-133B1		2 = 0198(1.125")	133	2Q01	3Q01	
								-13EB1			133	TBD	TBD	
	DS							-10EB2			100	2Q01	3Q01	1U
								-133B2			133	2Q01	3Q01	1U
								-13EB2			133	TBD	TBD	1U
512MB	DS	64 Meg x 72 3.3V ECC Gold DIMM	168	(36)	32 Meg x 4	3.3V FBGA	MT36LSDF6472G	-10EB1	B = Y85B	1 = 0123(1.70")	100	Now	Now	11x13pkg
								-133B2		2 = 0142(1.70")	133	Now	Now	CL3
	DS	64 Meg x 64 3.3V Gold DIMM	168	(16)	32 Meg x 8	3.3V TSOP	MT16LSDT6464AG	-10EB1	B = Y96	1 = TBD (1.375")	100	2Q01	3Q01	
								-133B1			133	2Q01	3Q01	CL3
								-13EB1			133	TBD	TBD	CL2
	DS	64 Meg x 64 3.3V Gold DIMM	144	(16)	32 Meg x 8	3.3V FBGA	MT16LSDF6464HG	-10EB1	B = Y96	1 = 0185 (1.25")	100	2Q01	3Q01	
								-133B1			133	2Q01	3Q01	
	DS	64 Meg x 72 3.3V ECC Gold DIMM	168	(18)	32 Meg x 8	3.3V TSOP	MT18LSDT6472AG	-10EB1	B = Y96	1 =TBD (1.375")	100	2Q01	3Q01	
								-133B1			133	2Q01	3Q01	CL3
								-13EB1			133	TBD	TBD	CL2
	DS	64 Meg x 72 3.3V ECC Gold DIMM	168	(18)	64 Meg x 4	3.3V TSOP	MT18LSDT6472G	-10EB1	B = Y96	1 = 0129 (1.700")	100	2Q01	3Q01	
								-133B1			133	2Q01	3Q01	CL3
								-13EB1			133	TBD	TBD	CL2
	DS	64 Meg x 72 3.3V ECC Gold DIMM	168	(18)	32 Meg x 8	3.3V TSOP	MT18LSDT6472DG	-10EB1	B = Y96	1 =0156 (1.70")	100	2Q01	3Q01	
								-133B1		2 =0198 (1.125")	133	2Q01	3Q01	
								-13EB1			133	TBD	TBD	
								-10EB2			100	2Q01	3Q01	1U
								-133B2			133	2Q01	3Q01	1U
								-13EB2			133	TBD	TBD	1U
	DS	64 Meg x 72 3.3V ECC Gold DIMM	168	(18)	64 Meg x 4	3.3V FBGA	MT18LSDF6472G	-10EB1	B = Y96	1 = 0187 (1.05")	100	2Q01	3Q01	1U
								-133B1			133	2Q01	3Q01	1U
								-13EB1			133	TBD	TBD	1U
1GB	DS	128 Meg x 72 3.3V ECC Gold DIMM	168	(36)	64 Meg x 4	3.3V fBGA	MT36LSDF12872G	-10EB1	B = Y96	1 = TBD (1.700")	100	2Q01	3Q01	
								-133B1			133	2Q01	3Q01	CL3
								-13EB1			133	TBD	TBD	CL2
							a	b						Rev. 3/26/01

Part Number = a + b
Example: MT36LSDF12872G-13EB1

*For 168-pin DIMMs (66 MHz/100 MHz), adheres to Intel's 4-Clock SDRAM module specs (66 MHz will use -10 components; 100 MHz will use -8 components). For 100-pin DIMMs, 100 MHz uses -10 components; adheres to JEDEC standard.

SS - Single Sided **DS** - Double Sided **G** - Gold Plated **U** - 100-pin DIMM **UDG** - Double-sided, dual-bank 100-pin DIMM
(H) - Small-Outline DIMM (SODIMM) **LP** - Low Power **(A)** - 8-CAS; SPD version; unbuffered (no "A" denotes registered version for x72 DIMMs)
(W) - Micro DIMM

Micron Memory DDR SDRAM Module Reference Guide

												Availability	
Density	Description		Pins	Components on Module			Base Part Number	Speed	Die Rev.	PCB (height)	MHz	Samples	Production
64MB	SS	8 Meg x 64 2.5V Gold SODIMM	200	(4)	8 Meg x 16	TSOP	MT4VDDT864HG	-202B1	B = T95	1 = 0175 (1.25")	200	2Q01	3Q01
								-265B1			266	2Q01	3Q01
								-262B1			266	TBD	TBD
	SS	8 Meg x 64 2.5V Gold DIMM	184	(4)	8 Meg x 16	TSOP	MT4VDDT864AG	-202B1	B = T95	1 = 0151 (1.0")	200	2Q01	3Q01
								-265B1			266	2Q01	3Q01
								-262B1			266	TBD	TBD
	DS	8 Meg x 64 2.5V Gold DIMM	172	(4)	8 Meg x 16	TSOP	MT4VDDT864WG	-202B1	B = T95	1 = 0207 (1.25")	200	2Q01	3Q01
								-265B1			266	2Q01	3Q01
128MB	SS	16 Meg x64 2.5V Gold DIMM	184	(8)	16 Meg x 8	TSOP	MT8VDDT1664AG	-202A1	A = T85	1 = 0161 (1.25")	200	Now	Now
								-265A1	B = T95		266	Now	Now
								-202B1			200	2Q01	3Q01
								-265B1			266	2Q01	3Q01
								-262B1			266	TBD	TBD
	DS	16 Meg x64 2.5V Gold SODIMM	200	(8)	16 Meg x 8	TSOP	MT8VDDT1664HG	-202A1	A = T85	1 = 0168(1.25")	200	Contact Mktg	Contact Mktg
								-265A1			266	Contact Mktg	Contact Mktg
	DS	16 Meg x64 2.5V Gold SODIMM	200	(8)	8 Meg x 16	TSOP	MT8VDDT1664HG	-202B2	B = T95	2 = 0174 (1.25")	200	2Q01	3Q01
								-265B2			266	2Q01	3Q01
								-262B2			266	TBD	TBD
	SS	16 Meg x 64 2.5V Gold SODIMM	200	(4)	16 Meg x 16	TSOP	MT4VDDT1664HG	-202A1	A = T96	1 = 0175 (1.25")	200	2Q01	3Q01
								-265A1			266	2Q01	3Q01
								-262A1			266	TBD	TBD
	SS	16 Meg x 64 2.5V Gold SODIMM	184	(4)	16 Meg x 16	TSOP	MT4VDDT1664AG	-202A1	A = T96	1 = 0151 (1.25")	200	2Q01	3Q01
								-265A1			266	2Q01	3Q01
								-262A1			266	TBD	TBD
	DS	16 Meg x 64 2.5V Gold SODIMM	172	(4)	16 Meg x 16	TSOP	MT4VDDT1664WG	-202A1	A = T96	1 = 0207 (1.25")	200	2Q01	3Q01
								-265A1			266	2Q01	3Q01
	SS	16 Meg x72 ECC 2.5V Gold DIMM	184	(9)	16 Meg x 8	TSOP	MT9VDDT1672AG	-202A1	A = T85	1 = 0161 (1.25")	200	Now	Now
								-265A1	B = T95		266	Now	Now
								-202B1			200	2Q01	3Q01
								-265B1			266	2Q01	3Q01
								-262B1			266	TBD	TBD
	SS	16 Meg x72 ECC 2.5V Gold DIMM	184	(5)	16 Meg x 16	TSOP	MT5VDDT1672AG	-202A1	A = T96	1 = 0151 (1.25")	200	2Q01	3Q01
								-265A1			266	2Q01	3Q01
								-262A1			266	TBD	TBD
	SS	16 Meg x72 ECC 2.5V Gold DIMM	184	(9)	16 Meg x 8	TSOP	MT9VDDT1672G	-202A1	A = T85	1 = 0162 (1.70")	200	Now	Now
								-265A1	B = T95	2 = TBD (1.2")	266	Now	Now
								-202B1			200	2Q01	3Q01
								-265B1			266	2Q01	3Q01
								-262B1			266	TBD	TBD
	DS							-202A2			200	2Q01	3Q01
								-265A2			266	2Q01	3Q01
								-202B2			200	2Q01	3Q01
								-265B2			266	2Q01	3Q01
256MB	DS	32 Meg x64 2.5V Gold DIMM	184	(16)	16 Meg x 8	TSOP	MT16VDDT3264AG	-202A1	A = T85	1 = 0116B (1.25")	200	Now	Now
								-265A1	B = T95		266	Now	Now
								-202B1			200	2Q01	3Q01
								-265B1			266	2Q01	3Q01
								-262B1			266	TBD	TBD
	DS	32 Meg x64 2.5V Gold SODIMM	200	(8)	16 Meg x 16	TSOP	MT8VDDT3264HG	-202A1	A = T96	1 = 0174 (1.25")	200	2Q01	3Q01
								-265A1			266	2Q01	3Q01
								-262A1			266	TBD	TBD
	SS	32 Meg x64 2.5V Gold SODIMM	184	(8)	32 Meg x 8	TSOP	MT8VDDT3264AG	-202A1	A = T96	1 = 0161 (1.25")	200	2Q01	3Q01
								-265A1			266	2Q01	3Q01
								-262A1			266	TBD	TBD
256MB	DS	32 Meg 72 ECC 2.5V Gold DIMM	184	(18)	16 Meg x 8	TSOP	MT18VDDT3272AG	-202A1	A = T85	1 = 0116B (1.25")	200	Now	Now
								-265A1	B = T95		266	Now	Now
								-202B1			200	2Q01	3Q01
								-265B1			266	2Q01	3Q01
								-262B1			266	TBD	TBD
	DS	32 Meg 72 ECC 2.5V Gold DIMM	184	(18)	32 Meg x 4	TSOP	MT18VDDT3272G	-202A1	A = T85	1 = 0163 (1.70")	200	Now	Now
								-265A1	B = T95		266	Now	Now
								-202B1			200	2Q01	3Q01
								-265B1			266	2Q01	3Q01
								-262B1			266	TBD	TBD
	DS	32 Meg 72 ECC 2.5V Gold DIMM	184	(18)	16 Meg x 8	TSOP	MT18VDDT3272DG	-202A1	A = T85	1 = 0162 (1.70")	200	Now	Now
								-265A1	B = T95		266	Now	Now
								-202B1			200	2Q01	3Q01
								-265B1			266	2Q01	3Q01
								-262B1			266	TBD	TBD
	SS		184	(9)	32 Meg x 8	TSOP	MT9VDDT3272AG	-202A1	A = T96	1 = 0161 (1.25")	200	2Q01	3Q01
								-265A1			266	2Q01	3Q01
								-262A1			200	TBD	TBD
	DS		184	(9)	32 Meg x 8	TSOP	MT9VDDT3272G	-202A1	A = T96	1 = TBD (1.2")	200	2Q01	3Q01
								-265A1			266	2Q01	3Q01
								-262A1			200	TBD	TBD
512MB	DS	64 Meg 64 2.5V Gold DIMM	184	(16)	32 Meg x 8	TSOP	MT16VDDT6464AG	-202A1	A = T96	1 = 0116B (1.25")	200	2Q01	3Q01
								-265A1			266	2Q01	3Q01
								-262A1			266	TBD	TBD
	DS	64 Meg 72 ECC 2.5V Gold DIMM	184	(18)	32 Meg x 8	TSOP	MT18VDDT6472AG	-202A1	A = T96	1 = 0116B (1.25")	200	2Q01	3Q01
								-265A1			266	2Q01	3Q01
								-262A1			266	TBD	TBD
	DS	64 Meg 72 ECC 2.5V Gold DIMM	184	(18)	32 Meg x 8	TSOP	MT18VDDT6472DG	-202A1	A = T96	1 = 0162 (1.70")	200	2Q01	3Q01
								-265A1		2 = TBD (1.2")	266	2Q01	3Q01
								-262A1			266	TBD	TBD
								-202A2			200	2Q01	3Q01
								-265A2			266	2Q01	3Q01
	DS	64 Meg 72 ECC 2.5V Gold DIMM	184	(18)	64 Meg x 4	TSOP	MT18VDDT6472G	-202A1	A = T96	1 = 0163 (1.70")	200	2Q01	3Q01
								-265A1			266	2Q01	3Q01
								-262A1			266	TBD	TBD
	DS		184	(18)	64 Meg x 4	FBGA	MT18VDDF6472G	-202A1	A = T96	1 = TBD (1.125")	200	2Q01	3Q01
								-265A1			266	2Q01	3Q01
1GB	DS	128 Meg 72 ECC 2.5V Gold DIMM	184	(36)	64 Meg x 4	FBGA	MT36VDDF12872G	-202A1	A = T96	1 = 0173 (1.70")	200	2Q01	3Q01
								-265A1			266	2Q01	3Q01
								-262A1			266	TBD	TBD
							a	b					

Part Number = a + b
Example MT36VDDT6472G-262B1

SS - Single Sided **DS** - Double Sided **G** - Gold Plated
(H) - Small-Outline DIMM (SODIMM) **(A)** - 8-CAS; SPD version; unbuffered (no "A" denotes registered version for x72 DIMMs)

Micron Memory Rambus® RIMM™ Module Reference Guide

Density	Description		Pins	Components on Module		Base Part Number	Speed	Die Rev.	PCB (height)	MHz	Availability	
											Samples	Production
128MB	SS	64 Meg x 16 non-ECC	184	(4)	16 Meg x 16	MT4VR6416AG	-653A1	A = R96A	1 = TBD (1.25")	600	TBD	TBD
							-750A1			700	TBD	TBD
							-745A1			700	TBD	TBD
							-845A1			800	TBD	TBD
							-840A1			800	TBD	TBD
128MB	SS	32 Meg x 18 ECC	184	(4)	16 Meg x 18	MT4VR6418AG	-653A1	A = R96A	1 = TBD (1.25")	600	TBD	TBD
							-750A1			700	TBD	TBD
							-745A1			700	TBD	TBD
							-845A1			800	TBD	TBD
							-840A1			800	TBD	TBD
256MB	SS	64 Meg x 16 non-ECC	184	(8)	16 Meg x 16	MT8VR12816AG	-653A1	A = R96A	1 = TBD (1.25")	600	TBD	TBD
							-750A1			700	TBD	TBD
							-745A1			700	TBD	TBD
							-845A1			800	TBD	TBD
							-840A1			800	TBD	TBD
256MB	SS	64 Meg x 18 ECC	184	(8)	16 Meg x 18	MT8VR12818AG	-653A1	A = R96A	1 =TBD (1.25")	600	TBD	TBD
							-750A1			700	TBD	TBD
							-745A1			700	TBD	TBD
							-845A1			800	TBD	TBD
							-840A1			800	TBD	TBD
512MB	DS	128 Meg x 16 non-ECC	184	(16)	16 Meg x 16	MT16VR25616AG	-653A1	A = R96A	1 = TBD (1.25")	600	TBD	TBD
							-750A1			700	TBD	TBD
							-745A1			700	TBD	TBD
							-845A1			800	TBD	TBD
							-840A1			800	TBD	TBD
512MB	DS	128 Meg x 18 ECC	184	(16)	16 Meg x 18	MT16VR25618AG	-653A1	A = R96A	1 = TBD (1.25")	600	TBD	TBD
							-750A1			700	TBD	TBD
							-745A1			700	TBD	TBD
							-845A1			800	TBD	TBD
							-840A1			800	TBD	TBD

a	b
Part Number = a + b	
Example MT16VR25618AG-840A1	

Rev. 3/26/01