MICRON QUANTUM DEVICES, INC

128K, 256K, 512K x 16
BOOT BLOCK FLASH MEMORY

NEW BOOT BLOCK FLASH MEMORY

FLASH MEMORY

MT28F200B5 ET, MT28F400B5 ET, MT28F800B5 ET

Smart 5 Extended Temperature

FEATURES

- Extended temperature range operation: -40°C to +85°C
- Boot block architecture:
  - 16KB/4K-word boot block (protected)
  - Two 8KB/4K-word parameter blocks
  - Multiple 128KB/64K-word main blocks
- Smart 5 Voltage Technology:
  - 5V ±10% Vcc
  - 5V ±10% or 12V ±5% VPP
- Address access time:
  - 80ns
- Available densities:
  - 2Mb, 4Mb, 8Mb
- Industry-standard pinouts
- Inputs and outputs are fully TTL-compatible
- Automated write and erase algorithm
- Two-cycle WRITE/ERASE sequence
- TSOP packaging option

OPTIONS — MARKING

- Timing
  - 80ns access — -8
- Boot Block Starting Address
  - Top — T
  - Bottom — B
- Operating Temperature Range
  - Extended (-40°C to +85°C) — ET
- Packages
  - Plastic 48-lead TSOP Type 1 (12mm x 20mm) — WG
  - Plastic SOP (600 mil) — SG
- Part Number Example: MT28F200B5WG-8 TET

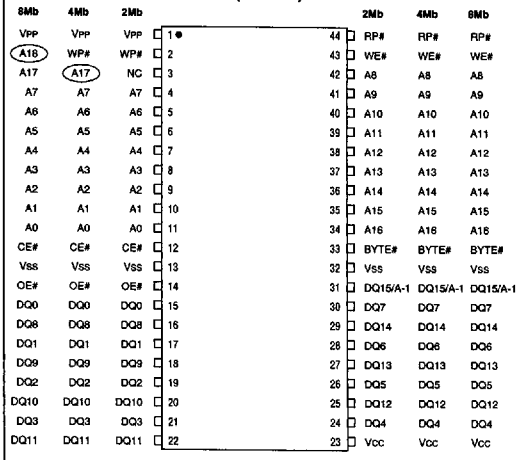
GENERAL DESCRIPTION

The Micron Smart 5 Extended Temperature flash memory family consists of 2Mb, 4Mb and 8Mb boot block, x16 flash memories. They are fabricated with Micron's advanced CMOS floating-gate process. Device operation and features of the MT28F200B5 ET, MT28F400B5 ET and MT28F800B5 ET are identical to the commercial temperature MT28F200B1, MT28F400B1 and MT28F800B1 respectively, except that extended temperature range operation is supported for all operations (-40°C to +85°C). All parameters for the MT28F200B5 ET, MT28F400B5 ET and MT28F800B5 ET are noted in this data sheet. For further information on device operation or features, refer to the MT28F200B1, MT28F400B1 or MT28F800B1 data sheets.

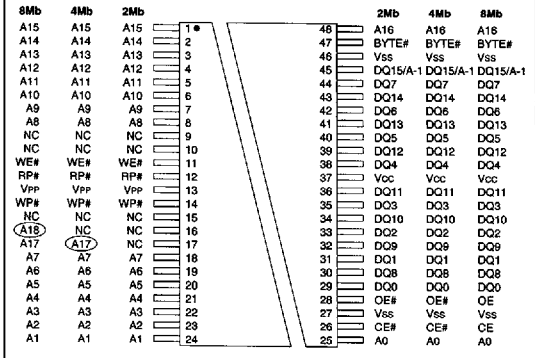
Please refer to Micron's web site (www.micron.com/flash/htmls/datasheets.html) for the latest data sheet revisions.

PIN ASSIGNMENT (Top View)

44-Pin SOP
(FA-1)



48-Pin TSOP Type I
(FB-2)



ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -0.5V to +6V**
Input Voltage Relative to V_{SS} ..... -0.5V to +6V**
V_{PP} Voltage Relative to V_{SS} ..... -0.5V to +12.6V†
RP# or A9 Pin Voltage Relative to V_{SS} .... -0.5V to +12.6V†
Temperature under Bias ..... -40°C to +85°C
Storage Temperature (plastic) ..... -55°C to +125°C
Power Dissipation 1W

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
**V_{CC}, input and I/O pins may transition to -2V for <20ns and V_{CC} + 2V for <20ns.
†Voltage may pulse to -2V for <20ns and 14V for <20ns.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC READ OPERATING CONDITIONS

(-40°C ≤ T_A ≤ +85°C)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	1
Input High (Logic 1) Voltage, all inputs	V_{IH}	2	V_{CC} + 0.5	V	1
Input Low (Logic 0) Voltage, all inputs	V_{IL}	-0.5	0.8	V	1
Device Identification Voltage, A9	V_{ID}	11.4	12.6	V	1
V_{PP} Supply Voltage	V_{PP}	-0.5	12.6	V	1

DC OPERATING CHARACTERISTICS

(-40°C ≤ T_A ≤ +85°C; V_{CC} = 5V ±10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
OUTPUT VOLTAGE LEVELS (TTL) Output High Voltage (I_{OH} = -2.5mA)	V_{OH1}	2.4		V	1
Output Low Voltage (I_{OL} = 5.8mA)	V_{OL}		0.45	V	
OUTPUT VOLTAGE LEVELS (CMOS) Output High Voltage (I_{OH} = -100µA)	V_{OH2}	V_{CC} - 0.4		V	1
INPUT LEAKAGE CURRENT Any input (0V ≤ V_{IN} ≤ V_{CC}); all other pins not under test = 0V	I_L	-1	1	µA	
INPUT LEAKAGE CURRENT: A9 INPUT (11.4V ≤ A9 ≤ 12.6 = V_{ID})	I_{ID}		500	µA	
INPUT LEAKAGE CURRENT: RP# INPUT (11.4V ≤ RP# ≤ 12.6 = V_{HH})	I_{HH}		500	µA	
OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled; 0V ≤ V_{OUT} ≤ V_{CC})	I_{OZ}	-10	10	µA	

NOTE: 1. All voltages referenced to V_{SS}.

CAPACITANCE

(T_A = 25°C; f = 1 MHz)

PARAMETER/CONDITION	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	C_I	8	pF	
Output Capacitance	C_O	12	pF	

READ AND STANDBY CURRENT DRAIN

(-40°C ≤ T_A ≤ +85°C)

PARAMETER/CONDITION	SYMBOL	MAX	UNITS	NOTES
READ CURRENT: WORD-WIDE, TTL INPUT LEVELS (CE# = V_{IL}; OE# = V_{IH}; f = 10 MHz; Other inputs = V_{IL} or V_{IH}; RP# = V_{IH})	I_{CC1}	70	mA	1, 2
READ CURRENT: WORD-WIDE, CMOS INPUT LEVELS (CE# ≤ 0.2V; OE# ≥ V_{CC} - 0.2V; f = 10 MHz; Other inputs ≤ 0.2V or ≥ V_{CC} - 0.2V; RP# ≥ V_{CC} - 0.2V)	I_{CC2}	65	mA	1, 2
READ CURRENT: BYTE-WIDE, TTL INPUT LEVELS (CE# = V_{IL}; OE# = V_{IH}; f = 10 MHz; Other inputs = V_{IL} or V_{IH}; RP# = V_{IH})	I_{CC3}	70	mA	1, 2
READ CURRENT: BYTE-WIDE, CMOS INPUT LEVELS (CE# ≤ 0.2V; OE# ≥ V_{CC} - 0.2V; f = 10 MHz; Other inputs ≤ 0.2V or ≥ V_{CC} - 0.2V; RP# = V_{CC} - 0.2V)	I_{CC4}	65	mA	1, 2
STANDBY CURRENT: TTL INPUT LEVELS V_{CC} power supply standby current (CE# = RP# = V_{IH}; Other inputs = V_{IL} or V_{IH})	I_{CC5}	2.5	mA	
STANDBY CURRENT: CMOS INPUT LEVELS V_{CC} power supply standby current (CE# = RP# = V_{CC} - 0.2V)	I_{CC6}	150	µA	
IDLE CURRENT (CE# ≤ 0.2V; f = 0Hz; Other inputs ≤ 0.2V, or ≥ V_{CC} - 0.2V; RP# = V_{CC} - 0.2V; Array read mode)	I_{CC7}	3.5	mA	
DEEP POWER-DOWN CURRENT: V_{CC} SUPPLY (RP# = V_{SS} ±0.2V)	I_{CC8}	20	µA	
STANDBY OR READ CURRENT: V_{PP} SUPPLY (V_{PP} > 5.5V)	I_{PP1}	50	µA	
STANDBY OR READ CURRENT: V_{PP} SUPPLY (V_{PP} ≤ 5.5V)	I_{PP2}	±15	µA	
DEEP POWER-DOWN CURRENT: V_{PP} SUPPLY (RP# = V_{SS} ±0.2V)	I_{PP3}	10	µA	

NOTE: 1. I_{CC} is dependent on cycle rates.
2. I_{CC} is dependent on output loading. Specified values are obtained with the outputs open.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(-40°C ≤ T_A ≤ +85°C; Vcc = +5V ±10%)

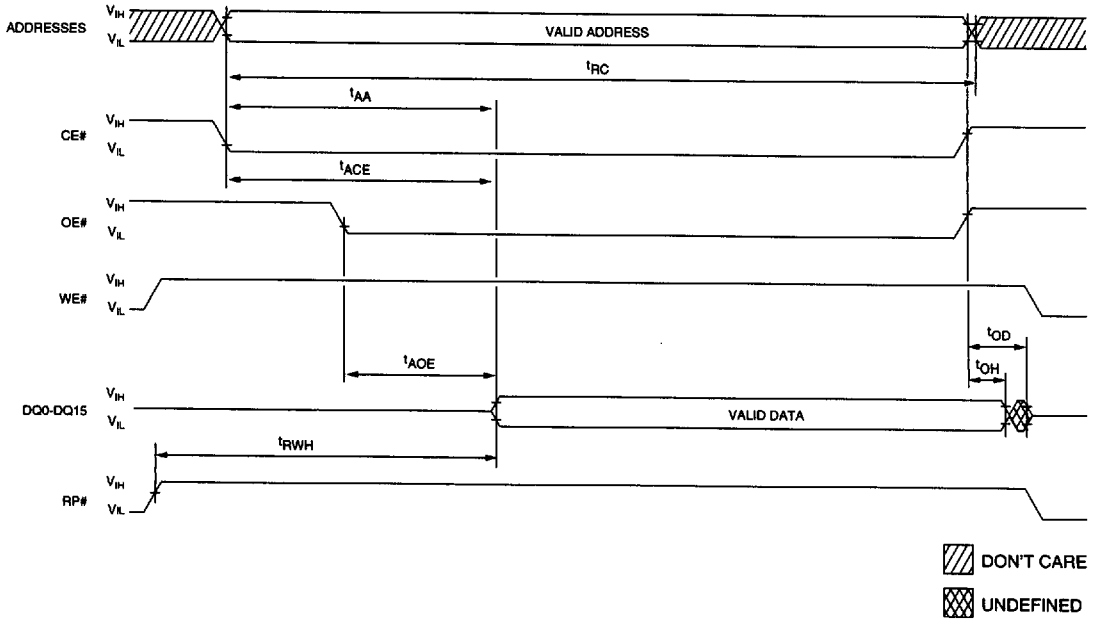
AC CHARACTERISTICS		-8			
PARAMETER	**SYMBOL**	**MIN**	**MAX**	**UNITS**	**NOTES**
READ cycle time	^tRC	80		ns	
Access time from CE#	^tACE		80	ns	1
Access time from OE#	^tAOE		40	ns	1
Access time from address	^tAA		80	ns	
RP# HIGH to output valid delay	^tRWH		1,000	ns	
OE# or CE# HIGH to output in High-Z	^tOD		30	ns	
Output hold time from OE#, CE# or address change	^tOH	0		ns	
RP# LOW pulse width	^tRP	60		ns	

NOTE: 1. OE# may be delayed by ^tACE minus ^tAOE after CE# falls before ^tACE is affected.

AC TEST CONDITION

Input pulse levels	0.4V to 2.4V
Input rise and fall times	<10ns
Input timing reference level	0.8V and 2V
Output timing reference level	0.8V and 2V
Output load	1 TTL gate and C_L = 100pF

WORD-WIDE READ CYCLE [1]



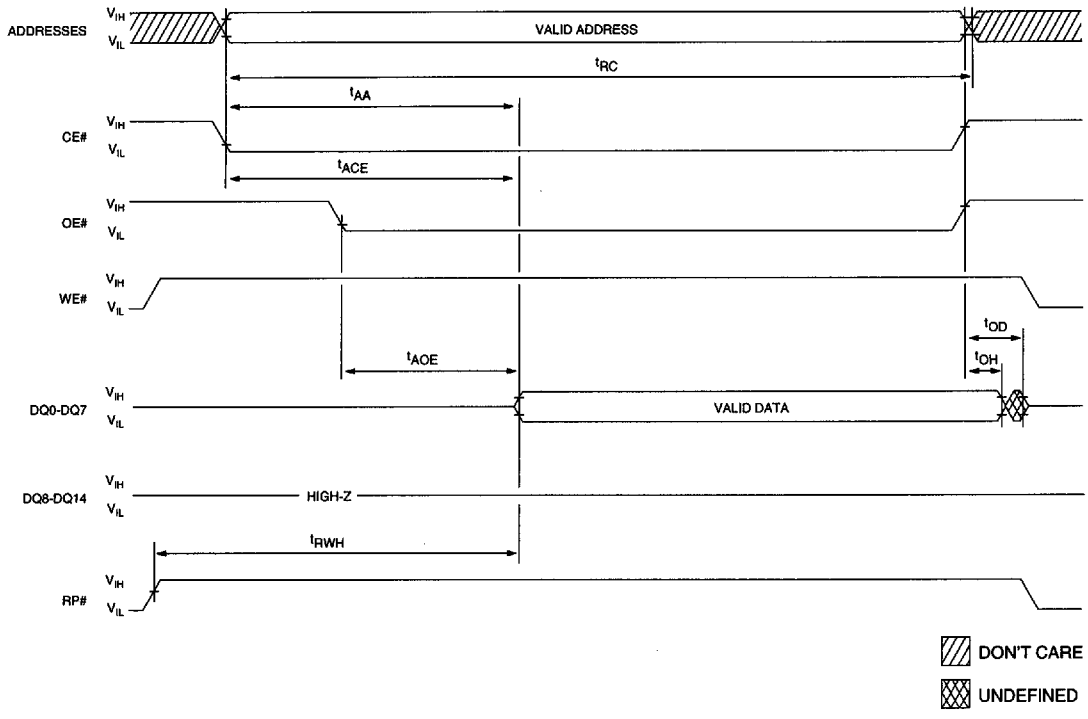
READ TIMING PARAMETERS

SYMBOL	-8 MIN	-8 MAX	UNITS
t_{RC}	80		ns
t_{ACE}		80	ns
t_{AOE}		40	ns
t_{AA}		80	ns

SYMBOL	-8 MIN	-8 MAX	UNITS
t_{RWH}		1,000	ns
t_{OD}		30	ns
t_{OH}	0		ns

NOTE: 1. BYTE# = HIGH.

BYTE-WIDE READ CYCLE [1]



READ TIMING PARAMETERS

SYMBOL	-8 MIN	-8 MAX	UNITS
tRC	80		ns
tACE		80	ns
tAOE		40	ns
tAA		80	ns

SYMBOL	-8 MIN	-8 MAX	UNITS
tRWH		1,000	ns
tOD		30	ns
tOH	0		ns

NOTE: 1. BYTE# = LOW.

RECOMMENDED DC WRITE/ERASE CONDITIONS

($-40°C \le T_A \le +85°C$; $V_{CC} = +5V \pm 10\%$)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
V_{PP} WRITE/ERASE lockout voltage	V_{PPLK}		1.5	V	1
V_{PP} voltage during WRITE/ERASE operation	V_{PPH1}	4.5	5.5	V	
V_{PP} voltage during WRITE/ERASE operation	V_{PPH2}	11.4	12.6	V	
Boot block unlock voltage	V_{HH}	11.4	12.6	V	
V_{CC} WRITE/ERASE lockout voltage	V_{LKO}	2		V	

WRITE/ERASE CURRENT DRAIN

($-40°C \le T_A \le +85°C$; $V_{CC} = +5V \pm 10\%$)

PARAMETER/CONDITION	SYMBOL	5V V_{PP} MAX	12V V_{PP} MAX	UNITS	NOTES
WORD WRITE CURRENT: V_{CC} SUPPLY	I_{CC9}	35	45	mA	
WORD WRITE CURRENT: V_{PP} SUPPLY	I_{PP4}	55	25	mA	
BYTE WRITE CURRENT: V_{CC} SUPPLY	I_{CC10}	25	45	mA	
BYTE WRITE CURRENT: V_{PP} SUPPLY	I_{PP5}	55	25	mA	
ERASE CURRENT: V_{CC} SUPPLY	I_{CC11}	25	40	mA	
ERASE CURRENT: V_{PP} SUPPLY	I_{PP6}	55	20	mA	
ERASE SUSPEND CURRENT: V_{CC} SUPPLY (ERASE suspended)	I_{CC12}	12	12	mA	2
ERASE SUSPEND CURRENT: V_{PP} SUPPLY (ERASE suspended)	I_{PP7}	200	200	µA	

NOTE: 1. Absolute WRITE/ERASE protection when $V_{PP} \le V_{PPLK}$.
2. Parameter is specified when device is not accessed. Actual current draw will be I_{CC12} plus READ current if a READ is executed while in erase suspend mode.

WRITE/ERASE AC TIMING CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS: WE#-CONTROLLED WRITEs

(-40°C ≤ T_A ≤ +85°C; Vcc = +5V ±10%)

AC CHARACTERISTICS		-8			
PARAMETER	**SYMBOL**	**MIN**	**MAX**	**UNITS**	**NOTES**
WRITE cycle time	^tWC	80		ns	
WE# HIGH pulse width	^tWPH	30		ns	
CE# HIGH pulse width	^tCPH	30		ns	
CE# pulse width	^tCP	50		ns	
WE# pulse width	^tWP	50		ns	
Address setup time to WE# HIGH	^tAS	60		ns	
Address hold time from WE# HIGH	^tAH	10		ns	
Data setup time to WE# HIGH	^tDS	60		ns	
Data hold time from WE# HIGH	^tDH	0		ns	
CE# setup time to WE# LOW	^tCS	0		ns	
CE# hold time from WE# HIGH	^tCH	0		ns	
V_{PP} setup time to WE# HIGH	$^tVPS1$	200		ns	1, 2
V_{PP} setup time to WE# HIGH	$^tVPS2$	100		ns	1, 3
RP# HIGH to WE# LOW delay	^tRS	1,000		ns	
RP# at V_{HH} or WP# HIGH setup time to WE# HIGH	^tRHS	100		ns	4
WRITE duration (WORD or BYTE WRITE)	$^tWED1$	6		µs	1
Boot BLOCK ERASE duration	$^tWED2$	300		ms	1, 4
Parameter BLOCK ERASE duration	$^tWED3$	300		ms	1
Main BLOCK ERASE duration	$^tWED4$	600		ms	1
WE# HIGH to busy status (SR7 = 0)	^tWB	200		ns	5
V_{PP} hold time from Status Data valid	^tVPH	0		ns	1
RP# at V_{HH} or WP# HIGH hold time from Status Data valid	^tRHH	0		ns	4
Boot block relock delay time	^tREL		100	ns	6

NOTE:
1. WRITE/ERASE times are measured to valid status register data (SR7 = 1).
2. Measured with V_{PP} = V_{PPH1} = 5V.
3. Measured with V_{PP} = V_{PPH2} = 12V.
4. RP# should be held at V_{HH} or WP# held HIGH until boot block WRITE or ERASE is complete.
5. Polling status register before ^tWB is met may falsely indicate WRITE or ERASE completion.
6. ^tREL is required to relock boot block after WRITE or ERASE to boot block.

WRITE/ERASE AC TIMING CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS: CE#-CONTROLLED WRITEs

(-40°C ≤ T_A ≤ +85°C; Vcc = +5V ±10%)

AC CHARACTERISTICS		-8			
PARAMETER	**SYMBOL**	**MIN**	**MAX**	**UNITS**	**NOTES**
WRITE cycle time	^tWC	80		ns	
WE# HIGH pulse width	^tWPH	30		ns	
CE# HIGH pulse width	^tCPH	30		ns	
CE# pulse width	^tCP	50		ns	
WE# pulse width	^tWP	50		ns	
Address setup time to CE# HIGH	^tAS	60		ns	
Address hold time from CE# HIGH	^tAH	10		ns	
Data setup time to CE# HIGH	^tDS	60		ns	
Data hold time from CE# HIGH	^tDH	0		ns	
WE# setup time to CE# LOW	^tWS	0		ns	
WE# hold time from CE# HIGH	^tWH	0		ns	
V_{PP} setup time to CE# HIGH	$^tVPS1$	200		ns	1, 2
V_{PP} setup time to CE# HIGH	$^tVPS2$	100		ns	1, 3
RP# HIGH to CE# LOW delay	^tRS	1,000		ns	
RP# at V_{HH} or WP# HIGH setup time to CE# HIGH	^tRHS	100		ns	4
WRITE duration (WORD or BYTE WRITE)	$^tWED1$	6		µs	1
Boot BLOCK ERASE duration	$^tWED2$	300		ms	1, 4
Parameter BLOCK ERASE duration	$^tWED3$	300		ms	1
Main BLOCK ERASE duration	$^tWED4$	600		ms	1
CE# HIGH to busy status (SR7 = 0)	^tWB	200		ns	5
V_{PP} hold time from Status Data valid	^tVPH	0		ns	1
RP# at V_{HH} or WP# HIGH hold time from Status Data valid	^tRHH	0		ns	4
Boot block relock delay time	^tREL		100	ns	6

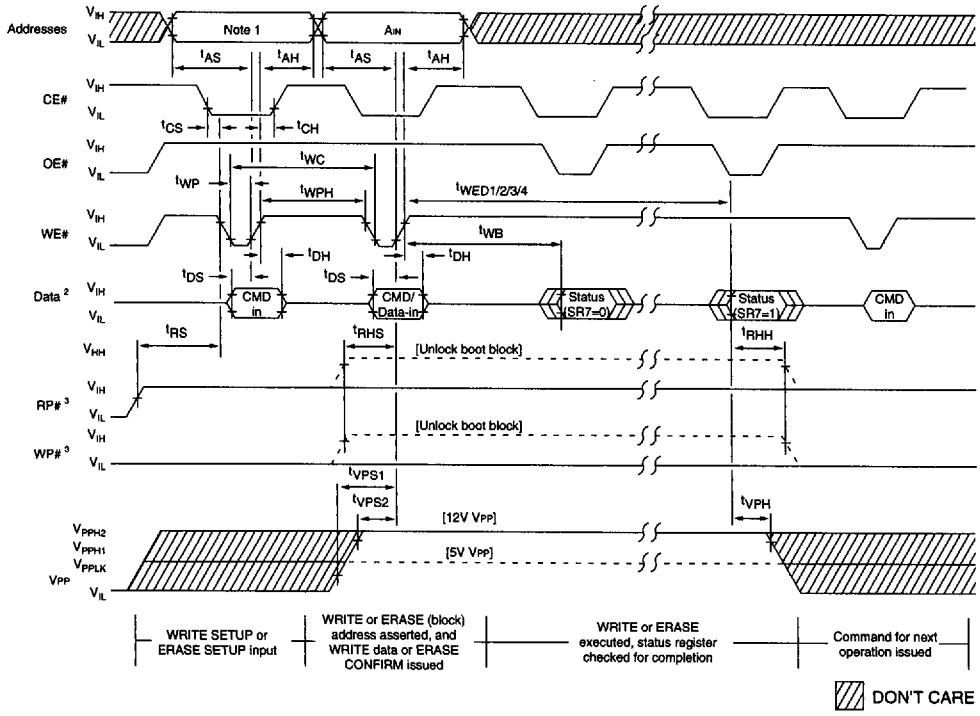
NOTE:
1. WRITE/ERASE times are measured to valid status register data (SR7 = 1).
2. Measured with V_{PP} = V_{PPH1} = 5V.
3. Measured with V_{PP} = V_{PPH2} = 12V.
4. RP# should be held at V_{HH} or WP# held HIGH until boot block WRITE or ERASE is complete.
5. Polling status register before ^tWB is met may falsely indicate WRITE or ERASE completion.
6. ^tREL is required to relock boot block after WRITE or ERASE to boot block.

WORD/BYTE WRITE AND ERASE DURATION CHARACTERISTICS

PARAMETER	5V V_{PP}		12V V_{PP}		UNITS	NOTES
	TYP	MAX	TYP	MAX		
Boot/parameter BLOCK ERASE time	0.8	7	0.5	7	s	1
Main BLOCK ERASE time	2	14	1.1	14	s	1
Main BLOCK WRITE time (BYTE mode)	1.8		1		s	1, 2, 3
Main BLOCK WRITE time (WORD mode)	1.1		0.6		s	1, 2, 3

NOTE: 1. Typical values measured at T_A = +25°C.
2. Assumes no system overhead.
3. Typical WRITE times tested with checkerboard data pattern.

WRITE/ERASE CYCLE
WE#-CONTROLLED WRITE/ERASE



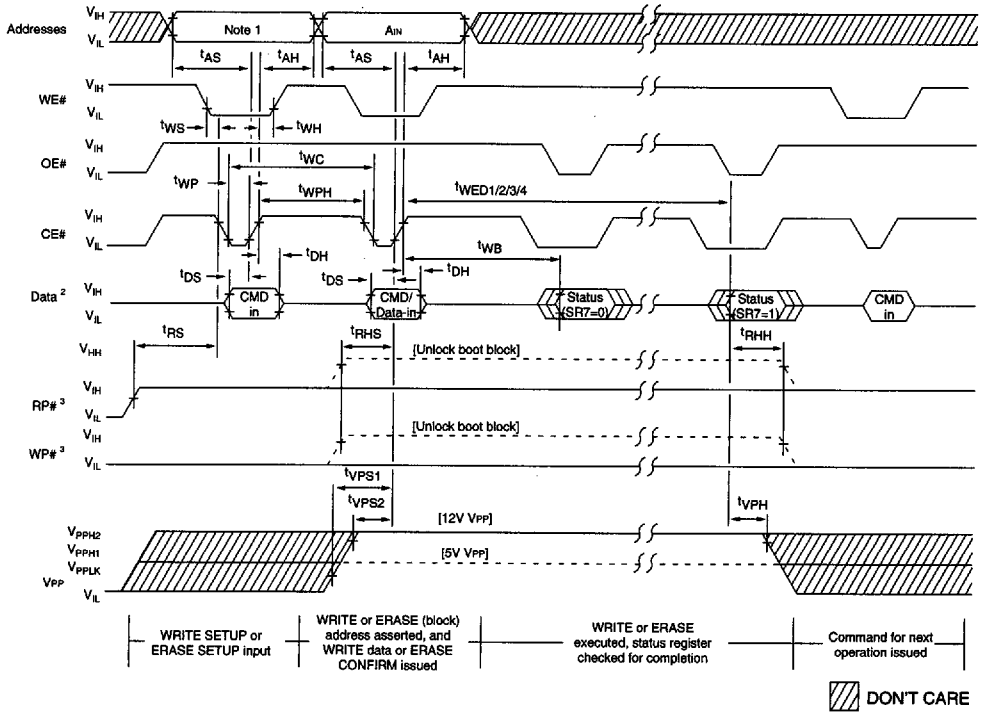
WRITE/ERASE TIMING PARAMETERS

SYMBOL	-8 MIN	-8 MAX	UNITS
tWC	80		ns
tWPH	30		ns
tWP	50		ns
tAS	60		ns
tAH	10		ns
tDS	60		ns
tDH	0		ns
tCS	0		ns
tCH	0		ns
tVPS1	200		ns

SYMBOL	-8 MIN	-8 MAX	UNITS
tVPS2	100		ns
tRS	1,000		ns
tRHS	100		ns
tWED1	6		µs
tWED2	300		ms
tWED3	300		ms
tWED4	600		ms
tWB	200		ns
tVPH	0		ns
tRHH	0		ns

NOTE: 1. Address inputs are "don't care" but must be held stable.
2. If BYTE# is LOW, DATA and COMMAND are 8-bit. If BYTE# is HIGH, DATA is 16-bit and COMMAND is 8-bit.
3. Either RP# at VHH or WP# HIGH unlocks the boot block.

WRITE/ERASE CYCLE
CE#-CONTROLLED WRITE/ERASE



WRITE/ERASE TIMING PARAMETERS

SYMBOL	-8 MIN	-8 MAX	UNITS
tWC	80		ns
tCPH	30		ns
tCP	50		ns
tAS	60		ns
tAH	10		ns
tDS	60		ns
tDH	0		ns
tWS	0		ns
tWH	0		ns
tVPS1	200		ns

SYMBOL	-8 MIN	-8 MAX	UNITS
tVPS2	100		ns
tRS	1,000		ns
tRHS	100		ns
tWED1	6		µs
tWED2	300		ms
tWED3	300		ms
tWED4	600		ms
tWB	200		ns
tVPH	0		ns
tRHH	0		ns

NOTE: 1. Address inputs are "don't care" but must be held stable.
2. If BYTE# is LOW, DATA and COMMAND are 8-bit. If BYTE# is HIGH, DATA is 16-bit and COMMAND is 8-bit.
3. Either RP# at VHH or WP# HIGH unlocks the boot block.